



## **Invitation**

You are invited to attend

### **IHP's 6<sup>th</sup> Workshop**

**High-Performance SiGe:C BiCMOS for Wireless  
and Broadband Communication:**  
Technology, IC Design, and Applications  
(Sept. 10, 2007, 9:30-16:30)

and the

### **Tutorial**

**IHP Design Kits:**  
Installation, Design Flow & Special Features  
(Sept. 11, 9:00 –Sept. 12, 14:00, 2007)



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## Workshop Agenda:

9:30 Welcome W. Mehr

### Technologies

9:40 IHP Technology Roadmap Update and Future Research Topics B. Tillack

10:00 0.13  $\mu\text{m}$  BiCMOS Development H. Rucker

10:20 New LDMOS Module for 0.25  $\mu\text{m}$  SiGe:C BiCMOS Technologies R. Sorge

### Coffee Break

### Design Kits & Prototyping

11:20 Overview IHP Design Kits and Modeling U. Biswurm

11:40 MPW and Prototyping Service R. Scholz

12:10 RFIC Design Solutions Overview & Future Roadmap  
Agilent EEs of EDA  
(Agilent Technologies GmbH & Co. KG) I. Nickeleit /  
G. Berger

12:30 Virtuoso IC 6.1, New Paradigm for Full Custom Design  
(Cadence Design Systems GmbH) P. Köhler

13:00 RF/Mixed-Signal Structured ASIC  
(advICo microelectronics GmbH) H. Safdary

### Light Lunch

### Integrated Circuits

14:20 Integrated Circuits for 77-81 GHz Short-Range  
Automotive Radar  
(University of Ulm) B. Schleicher

14:40 A 60 GHz SiGe-HBT Power Amplifier with 18 dB Gain  
and 20% PAE  
(TU Berlin) V. Subramanian

15:00 High frequency MMICs in SG25H1 up to 120GHz  
(Silicon Radar GmbH) W. Winkler

15:20 Single-Chip Fractional-N Synthesizer for Space  
Applications in SGB25VD F. Herzel

15:40 Design of High Speed Data Converter Components  
in SG25H1 S. Halder



**The Tutorial will help to save time in using IHP's design kits and to make use of their full potential. Topics include:**

- ASIC Design Flow
- Design Entry and Simulation with Spectre
- Layout creation using LayoutXL/DRD
- Verification with Diva or Assura
- Filler Generation
- Parasitic Extraction and Postlayoutsimulation
- Additional Tools (LENa, onGrid, shrinkLib, UpdateCDF, Calculator ext.)
- Installation Requirements (OS and Cadence versions), Installation and Version Management
- Interface to ADS (standalone ADS and RFDE)
- Discussion of open questions.

***The tutorial will be given by advlCo.***



# Organisation

## Registration

Please fill out the attached registration form. After receipt of your registration we will send you a confirmation and an invoice for the attendance fee (€ 80 for the workshop and € 500 for the tutorial).

## Contact and Requests

Dr. Wolfgang Kissinger

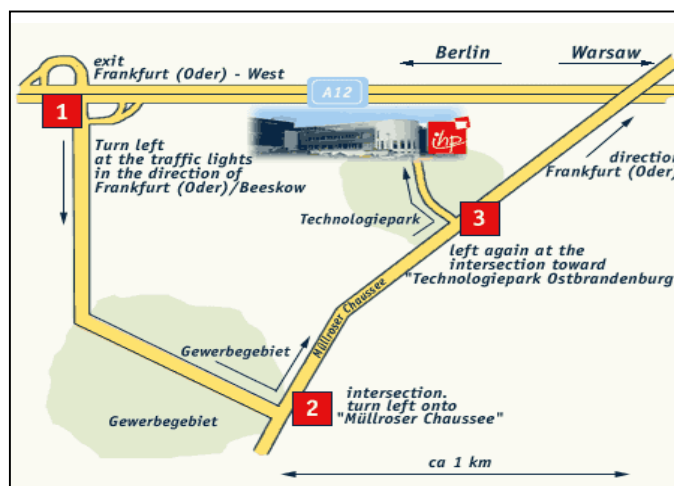
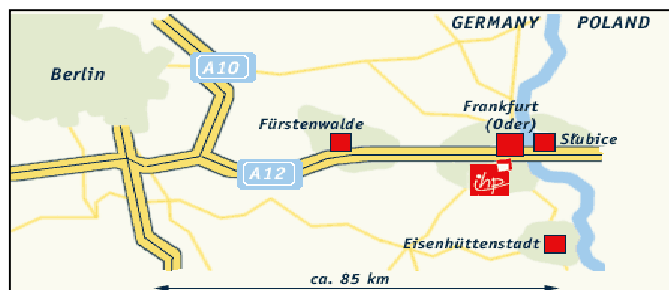
[kissinger@ihp-microelectronics.com](mailto:kissinger@ihp-microelectronics.com)

Fax: +49 335 5625 222

Phone: +49 335 5625 410

## Location

The workshop will take place at the IHP  
Im Technologiepark 25  
D-15236 Frankfurt (Oder)  
Germany





## Registration Form

I will attend the IHP workshop at September 10, 2007  
I will attend the IHP tutorial at September 11-12, 2007

Yes	No
<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	<input type="checkbox"/>

Family Name.....

First Name.....

Titel.....

Organisation.....

Address.....

City.....

Zip Code.....

Country.....

Email.....

Phone.....

Fax.....

The attendance fee is € 80 for the workshop and € 500 for the tutorial (25% tutorial-discount for Europractice members). It includes documentations, light lunch and refreshments. It will be invoiced with the confirmation of your registration.

***Please fax or mail the registration form to***

Dr. Wolfgang Kissinger, Im Technologiepark 25

D-15236 Frankfurt (Oder), Germany

Email: [kissinger@ihp-microelectronics.com](mailto:kissinger@ihp-microelectronics.com)

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