

# Press Release



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## Project GALAXY will push GALS design flow for chip integration

### *European Commission acknowledges successful start of the project*

**Frankfurt (Oder), July 2008:** The project "GALS Interface for Complex Digital System Integration" (GALAXY) funded under the The Seventh Framework Programme (2007-2013), Objective ICT-2007.3.3: Embedded System Design has started recently and will take 2.5 years more to complete. The European Commission has acknowledged a successful start of the project and expressed satisfaction with the first results. This EUR 4 million project is being carried out by a consortium, led by IHP GmbH (Germany). EUR 2.9 million is funded by the European Commission and the rest by the project partners including University of Manchester (UK), University of Bologna (Italy), EPFL (Switzerland), Silistix (UK), and Infineon Technologies (Germany).

The goal of the project is to provide an integrated Globally Asynchronous, Locally Synchronous (GALS) design flow, together with novel Network-on-Chip (NoC) capabilities. The project will evaluate the ability of the GALS approach to solve system integration issues. The results will be demonstrated by implementing a complex wireless communication system.

The increased complexity, performance requirements, and the need for power and electromagnetic interference (EMI) reduction are a big challenge for designers of complex chips. Furthermore, the continued technology improvement towards nanoscale dimensions brings additional challenges for embedded system design. For that reason, Chipset designers and system engineers have recognized the necessity to deal with these issues; one very promising option is the use of a GALS design methodology.

Most of the today's designs are synchronous, i.e. there is a common clock signal driving all blocks in the design. However, it is possible that system blocks internally operate synchronously and communicate asynchronously. In this case, there is no need for a common clock that should synchronize all blocks. Such system is usually referred to as a GALS system.

In the framework of the project it is intended to prove that the GALS methodology offers powerful solutions for modern system integration. The goal is to promote the development of GALS system design by providing an interoperability framework between the existing open or commercial CAD tools. It is planned to explore and evaluate the ability of GALS to solve system integration issues as well as building on its reduced EMI and low-power properties. A promising target platform can be seen in the area of NoCs. In this project, different approaches of implementing GALS-enabled NoC platforms will be investigated and compared with fully synchronous implementations. We integrate the NoC design flow into the GALS design flow.

"The project reinforces European competitiveness by extending the existing expertise in synchronous and asynchronous design methodologies in the direction of heterogeneous design methods. The GALS technique will play a major role as the integration technique for future complex embedded systems", explains project coordinator Milos Krstic from IHP.

More information on this project is available at: [www.galaxy-project.org](http://www.galaxy-project.org)

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**About IHP:**

The IHP ([www.ihp-microelectronics.com](http://www.ihp-microelectronics.com)) is a publicly funded R&D institution. The IHP's core competencies include process technology, circuit design, and communication systems design, with emphasis on wireless and broadband. The IHP consists of approximately 200 R&D experienced professionals working in a recently completed facility, including a state-of-the-art 200-mm pilot line housed in a 1,000-square-meter class-1 cleanroom. It is located at Im Technologiepark 25, 15236 Frankfurt (Oder), Germany.