to be published in Analog Integrated Circuits and Signal Processing
DOI 10.1007/s10470-010-9454-z final version available at: www.springerlink.com

An Integrated 8-12 GHz Fractional-N Frequency Synthesizer in SiGe BiCMOS for Satellite Communications

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Received: Nov.17, 2009 / Accepted: Jan.06, 2010

Abstract We present an integrated fractional-N low-noise frequency synthesizer for satellite applications. By using two integrated VCOs and combining digital and analog tuning techniques, a PLL lock range from 8 to 12 GHz is achieved. Due to a small VCO fine tuning gain and optimized charge pump output biasing, the phase noise is low and almost constant over the tuning range. All 16 sub-bands show a tuning range above 900 MHz each, allowing temperature compensation without sub-band switching. This makes the synthesizer robust against variations of the device parameters with process, supply voltage, temperature and aging. The measured phase noise is -87 dBc/Hz and -106 dBc/Hz at 10 kHz and 1 MHz offset, respectively. In integer-N mode, phase noise values down to -98 dBc/Hz at 10 kHz and -111 dBc/Hz at 1 MHz offset, respectively, were measured.

Keywords Phase-locked loop · satellite communication · phase noise · SiGe · BiCMOS · PVT tolerance

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1 Introduction

Telecommunication satellites have to be more flexible in the future to cover new applications in Ku-band and Ka-band. Examples are HDTV and internet-via-satellite services such as DVB-RCS [1]. The local oscillator (LO) frequency should be reconfigurable in orbit by a ground tele-command to achieve flexibility during the 15 years satellite lifetime. For our application, a tuning range from 8.5 GHz to 11.5 GHz is required [2]. In order to achieve low cost and high flexibility, highly integrated silicon-based solutions are desirable. Integer-N phase-locked loops (PLL) in SiGe BiCMOS at 18 GHz and above have been reported recently [3]-[5]. However, since in integer-N PLLs the channel spacing cannot be smaller than the comparison frequency in the phase detector, they are not very flexible. Fractional-N synthesizers can overcome this difficulty by providing synthesis of fractional multiples of the reference frequency [6]. Fractional-N PLLs above 10 GHz have been reported in both CMOS [7], [8] and SiGe BiCMOS technology [2], [9]. In all these PLLs, the tuning range is below 10 percent, limiting their flexibility in the context of satellite payloads.

Silicon-Germanium (SiGe) HBTs compare favorably with CMOS and GaAs HBT technologies in radiation hardness [10] and flicker noise performance [11]. The high speed of emitter-coupled logic (ECL) dividers allows a high comparison frequency at the phase-frequency detector (PFD) input to be used, resulting in a low close-in phase noise. The combination of SiGe HBTs with CMOS logic within a SiGe BiCMOS technology allows a single-chip integration of the low-noise RF circuitry and high speed ECL logic with the complex logic functions required for channel selection and $\Sigma\Delta$ modulation.

This paper extents the tuning range of an integrated frequency synthesizer to 40 percent of the center frequency, maintaining a robust low-phase-noise performance over the whole tuning range. This has been achieved by using an array of two voltage-controlled oscillators (VCO) in conjunction with digital varactor switching [12] and a modern analog tuning principle [9] in a single chip for the first time. The digital tuning employs differential varactors in the VCO controlled by digital signals, thereby avoiding noisy MOSFET switches in the VCO tank. For analog tuning, relative wide bands with large overlaps between them are used in order to avoid band switching during operation. Charge-pump-induced phase noise is minimized by employing a slow coarse tuning loop in parallel to a fast fine tuning loop for VCO noise suppression. High robustness of loop bandwidth and phase noise spectrum is achieved by DC output biasing of the charge pump for fine tuning.

2 PLL Architecture

Integrated PLLs have to cope with variations in the device parameters with process and temperature, resulting in frequency variations of the VCO. Therefore, the tuning range must be relatively large in order to cover the desired band and the VCO frequency variations. This translates into a high VCO gain, increasing the sensitivity of the PLL with respect to the noise in the control line. As a result, undesired frequency components (reference spurs) are generated. This effect becomes yet more troublesome with technology scaling, since the supply voltage needs to be reduced, which increases the required VCO gain. A VCO with two or more control ports is useful in this context [13], [12]. One way to reduce the VCO gain maintaining a moderate tuning range is to digitally switch between different capacitances in the resonance circuit [14], [15]. Such a switched-capacitor tuning loop requires an array of capacitances which need to be controlled digitally. This extends the possible tuning range beyond the possibilities of the available varactors. One disadvantage of this approach is the small tuning range of the sub-bands. Digital sub-band switching during operation is complex and not allowed in the application discussed in this paper. As a result, analog tuning over a wide range of typically five percent is mandatory for compensation of temperature and aging effects. A single-loop PLL having such a large tuning range is too noisy due to the large VCO gain. PLLs using dual-path active loop filters have been presented in [16] and [17]. They lend themselves to full integration, but the active circuitry adds noise to the PLL. Another way to achieve both a wide tuning range and a low noise is to employ a VCO with two analog tuning inputs driven by two parallel charge pumps [18]. Fig. 1

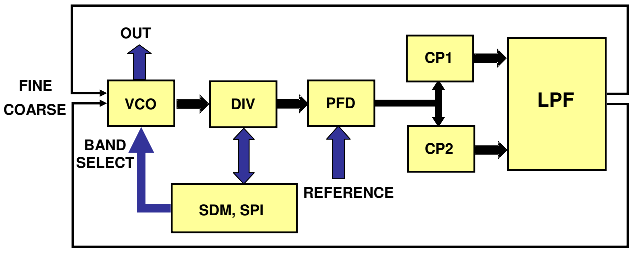

Fig. 1 Schematic of dual-loop frequency synthesizer

shows the general dual-loop PLL architecture using two parallel charge pumps. The VCO is followed by a prescaler and a programmable divider interacting with the digital CMOS block of the chip. The latter is composed of an integrated $\Sigma - \Delta$ modulator (SDM) and a serial processor interface (SPI). The divider output is connected to a PFD, which is followed by a high-current charge pump CP1 and a low-current charge pump CP2. The two charge pumps are connected to a low-pass filter (LPF), the two outputs of which control the oscillation frequency of the VCO. An advantage of this architecture is that the coarse tuning loop can be damped with a large capacitor avoiding a resistor in this loop. This reduces phase noise and spurs significantly. For applications with fast switching between channels, e.g. frequency hopping, the slewing of the coarse tuning voltage might not be acceptable, if the required frequency range exceeds the fine tuning range of the PLL. However, for applications at a constant frequency, as in satellite systems, the PLL dynamics in the steady state will not be affected by the slow coarse tuning loop. Two problems with the architecture in [18] are obvious. First, the variation of the VCO gain over the tuning range results in a high susceptibility of the phase noise spectrum to parameter variations. Second, if the charge pump output voltage approaches ground or the supply voltage, the phase noise may increase significantly. In order to improve this situation, some biasing of the fine tuning VCO input is helpful to keep the fine tuning voltage in a region, where the phase noise is low. This has been done using both ring oscillators [19] and LC-VCOs [20] by employing active integrators. In order to avoid phase noise contributions from active circuitry in the loop filter, we use the architecture of [18], but with an important modification: The charge pump for fine tuning is biased at the output by a resistive voltage divider. The dual-loop filter is depicted in Fig. 2. The fine tuning filter is a standard fourth-order

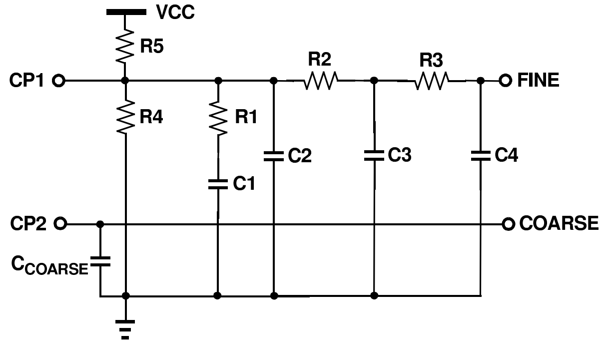

Fig. 2 Schematic of loop filter for biased dual-loop PLL topology

PLL filter supplemented with the two bias resistors R4 and R5. This voltage divider is connected to a quiet supply VCC (3.3 V) and to the board ground (0 V). It keeps the fine tuning voltage at a value where the VCO gain is fairly constant, resulting in a low phase noise. The filter in the coarse tuning loop is nothing but a large external capacitor (100 nF) in parallel with a 5 pF integrated metal-insulator-metal (MIM) capacitor. The loop dynamics in the steady state is not affected by the coarse tuning loop, if the capacitor C_{COARSE} is large enough [18]. Recently, this architecture was applied to an 18 GHz fractional-N PLL for satellite communications [9]. Bandwidth and phase noise spectrum were shown to be almost independent of the PLL output frequency.

In this paper, analog dual-loop tuning is supplemented with digital sub-band switching, as indicated in Fig. 1. In the context of satellite communication, this will allow parameter variations owing to the IC fabrication process to be compensated by proper selection of the sub-band in an initialization procedure before launching the satellite. The remaining tuning range provided by the analog dual-loop tuning can exclusively be exploited for compensating temperature variations and aging during the operation of the satellite.

3 PLL Building Blocks

3.1 Digital CMOS Block

We use a multi-stage noise shaping (MASH) type SDM in our design. The number of SDM stages is switchable from one to four by using the SPI. The number of stages will influence the slope of the phase noise spectrum at frequency offsets above 10 MHz. All SDM accumulators are 40 bit wide. This allows very fine frequency steps in the mHz range to be programmed. All SPI registers have been tripled to achieve better radiation hardness. This design principle is called triple-mode redundancy. More details about the digital circuitry used here are given in [2].

3.2 Voltage-Controlled Oscillator

In order to obtain 4 GHz tuning range, we combine two integrated VCOs selectable by a digital command as shown in Fig. 3. Each VCO has eight sub-bands controlled

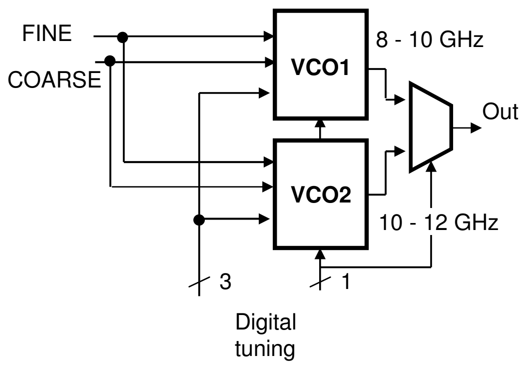

Fig. 3 Schematic of VCO array

by three bits. The schematic of one of the VCOs is shown in Fig. 4. The VCO core is based on a modified Colpitts principle in a differential configuration, since the Colpitts oscillator was reported to have an advantage over cross-coupled oscillators with respect to phase noise [21]. According to more recent works [22], [23], however, a cross-coupled pair oscillator might be a good alternative for low-noise applications.

Commonly, digital tuning is achieved by a bank of capacitors or inductors reconfigured via MOSFET switches. With this approach, the resistance and parasitic capacitances of the switches degrade the quality factor of the tank. Therefore, we avoid MOSFET switches in the resonator and use the varactors in a digital manner [12]. For digital tuning the switchable varactors are biased either in full depletion or in full accumulation, where the capacitance is relatively constant with the control voltage. The varactors are MOS-structures with a measured quality factor above 12 over the whole tuning range. Analog tuning is performed with two symmetric varactors. The VCOs have a separate supply. They can be operated from VCC=3.3 V as the rest of the chip, but a supply voltage of 5 V is also possible for phase noise minimization.

3.3 Frequency Divider

The VCO array is followed by a static divide-by-two circuit (DTC) realized as two latches in a negative feedback loop. This prescaler is followed by a programmable divider, the core of which is a divide-by-4/5 circuit. This dual-modulus divider is controlled by a 7-bit program counter and a 4-bit swallow counter. In order to ensure a safe operation of the programmable divider up to 6 GHz, the program and swallow counter as well as the divide-by-4/5 counter have been designed in ECL. The design is fully synchronous and uses only differential signal wires. The behavior of all counters was described in VHDL at Register Transfer Level (RTL). Unfortunately, the state-of-the-art synthesis tools do not support differential signals. So we propose a two-step

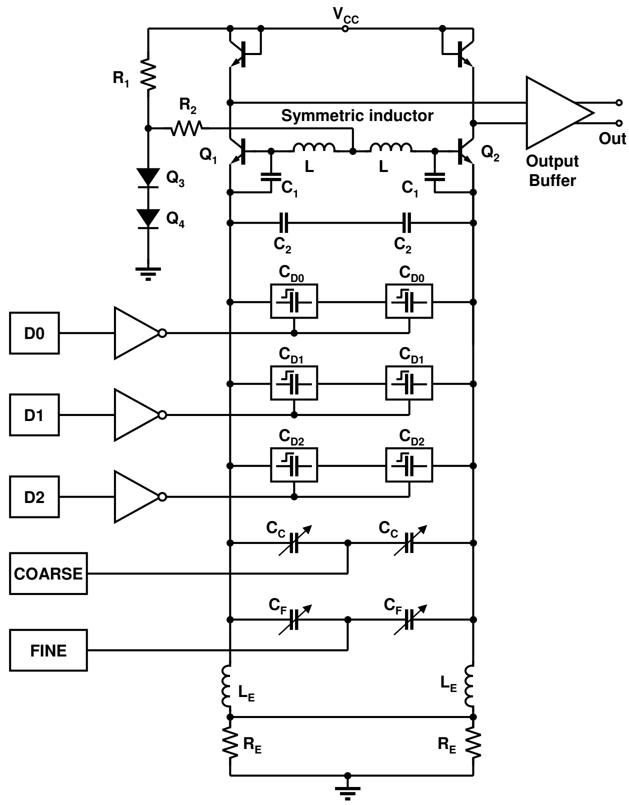

Fig. 4 Schematic of VCO with three control bits and two analog inputs

synthesis design flow to generate an ECL netlist from the RTL description. In a first step, a non-differential design was synthesized using single-ended signals, comparable to the standard CMOS design flow. In a second step, a converter, first described in [24], changes all signal wires to differential ones and automatically connects them to differential ECL gates in consideration of the proper polarity. A digital simulation ensures the proper operation of both the ECL and the CMOS parts before layouting [25].

Using a 0.25 μm SiGe BiCMOS process [26], the ECL gates and the digital CMOS parts were realized on the same chip, which increases the speed of CMOS-only designs tremendously. The BiCMOS design was proven by a common digital ECL and CMOS timing simulation at gate level to verify the functionality of the whole digital design. Furthermore, by using analog simulation, VCO and 1:2 prescaler were simulated together with the VHDL-based ECL design to verify the interface between the prescaler and the programmable divider.

3.4 Phase-Frequency Detector and Charge Pump

The PFD is taken from [27]. It consists of dynamic logic gates and a NOR gate in the feedback loop. The delay of the NOR gate was adjusted such that both UP pulse and DOWN pulse of the charge pump are briefly activated if the phase error is zero. This eliminates the dead zone of the PFD/CP, reducing the resulting jitter. The charge pump is essentially the same as in [28], but with five switchable binary weighted charge pumps in parallel. The current can be controlled digitally from 250 μA to 7750 μA in steps of 250 μA.

3.5 Reference Input Buffer

In wide-bandwidth PLLs having a large divider modulus N, the noise of the reference buffer is a major contributor to the output phase noise. We use a CMOS inverter chain as input buffer. The main problem here is the conversion of the crystal oscillator signal into a rectangular signal on the chip. Once this has been achieved, the additional phase noise contributions are small due to the large slope of the signal, which makes the signal phase robust against additive noise voltages. Assuming a sinusoidal reference signal, the phase noise contribution of the squaring CMOS inverter is given by

$$S_\phi^{\mathrm{BUF}} = \frac{S_V^{\mathrm{BUF}}}{V_0^2}\,, \tag{1}$$

where V_0 is the input amplitude, and S_V^{BUF} is the noise voltage power spectral density referred to the input. As has been shown in [9], the transconductance of the MOSFETs ($\propto W/L$) must be large enough to make this noise negligible. For an input power of 0 dBm, gate widths of at least 10 μm are recommended in the first CMOS inverter.

3.6 Loop Filter

The schematic of the loop filter was shown in Fig. 2. Two differences to a standard filter are obvious. First, a large capacitor C_{COARSE} is connected between the coarse tuning VCO input and ground. Second, two biasing resistors R4 and R5 are connected to the output of the high-current charge pump CP1, which is used for VCO fine tuning. The voltage divider R4/R5 deserves some special explanations. Without this DC biasing of the charge pump CP1 as in [18], there is an infinite number of control voltage combinations ($V_{\mathrm{FINE}}, V_{\mathrm{COARSE}}$) for a given PLL output frequency. This makes V_{FINE} and the resulting loop bandwidth unpredictable and dependent on device parameter variations. Our improved PLL topology including the voltage divider keeps the DC voltage of CP1 output close to VCC$\times$R4/(R4+R5), resulting in a constant phase noise spectrum over a wide range of output frequencies, as experimentally verified in Section 5. A minor drawback of the voltage divider is the fact that the fine tuning range $(\Delta f)_{\mathrm{FINE}}$ does not contribute to the useful tuning range of the PLL, which is defined by the coarse tuning range $(\Delta f)_{\mathrm{COARSE}}$ in this topology. If the PLL frequency is increased, then V_{COARSE} moves toward VDD, while V_{FINE} remains roughly constant. If the frequency is increased even more, then V_{FINE} is pulled up and the PFD starts to work against the voltage divider, raising phase noise and spurs. This drawback can by minimized by using a large ratio $(\Delta f)_{\mathrm{COARSE}}/(\Delta f)_{\mathrm{FINE}}$. For a value of 10, for example, the total useful tuning range is as large as $10\times(\Delta f)_{\mathrm{FINE}}$. The charge-pump-induced phase noise, however, remains small, since the low fine tuning gain of the VCO minimizes phase noise and spurs resulting from CP1. Phase noise and spur contributions resulting from the coarse tuning charge pump CP2 are negligible due to the large value of C_{COARSE} as verified in [9]. The sizing of C_{COARSE} entails a trade-off between settling time and noise performance as discussed in [18]. If settling is not critical as in our case, a large external capacitor of, e.g., 100 nF in parallel with an integrated MIM capacitor for suppression of high-frequency noise is a good choice. For a good biasing, R4 and R5 should be small, since the charge pump output resistance also affects the DC bias point and pulls the fine tuning voltage away from the noise optimum. However, if R4 is too small, its thermal noise current will be large, and the voltage divider will affect the loop dynamics increasing the phase noise floor and 1/f noise.

4 Modeling Results

We use the analytical linear fourth-order PLL model presented in [29] to optimize the loop filter. For the voltage divider we assume R5=R4. Fig. 5 shows the phase noise spectrum for different values of R4. As evident from the figure, the effect of the voltage

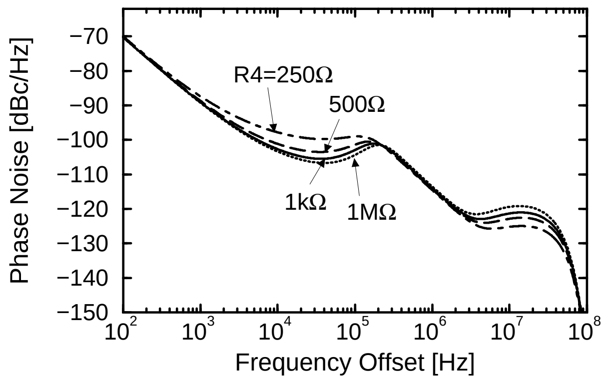

Fig. 5 Analytically calculated phase noise spectrum for different values of the bias resistor R4

divider on the phase noise is small, if R4 is larger than 1 kΩ. If the bias resistance R4 becomes lower than 1 kΩ, the phase noise floor will increase. This trade-off results in an optimum value for the bias resistance with respect to the integrated phase error. The RMS phase error is depicted in Fig. 6. It was determined from the phase noise spectrum $S_\phi = 10^{\pounds/10}$ according to

$$\sigma_\phi = \frac{180^\circ}{\pi}\sqrt{\int_0^\infty 2\,S_\phi(f)\,\mathrm{d}f}\,. \tag{2}$$

The influence of the bias resistors R4 on the open-loop transfer function is shown in Fig. 7. Obviously, the phase margin is not affected by the bias resistors, if R4 is not smaller than 1 kΩ.

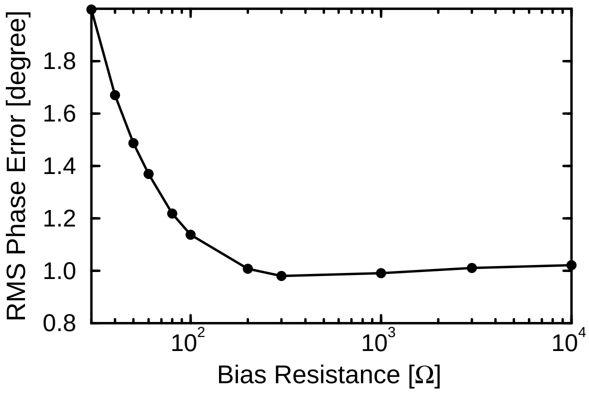

Fig. 6 RMS phase error as a function of the bias resistance R4

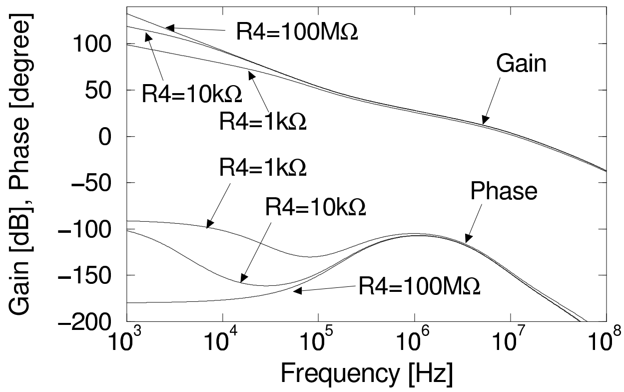

Fig. 7 Bode plot for three values of R4

5 Measurement Results

The synthesizer was fabricated in a low-cost SiGe BiCMOS technology [26] and occupies a die area of 1.2×6.0 mm^2 including pads. Fig. 8 shows a chip photo. A narrow and

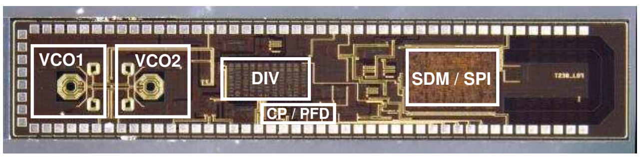

Fig. 8 Chip photo of the synthesizer

long layout was chosen in order to spatially separate the noisy digital circuitry from the charge pumps and the VCO array to minimize substrate noise coupling. The CMOS circuitry was surrounded by a guard ring with a dedicated ground pad to create a low-impedance path to ground for the substrate noise generated in the SDM. The analog circuitry was protected by vertical guard bands only in order to impede the substrate noise from propagating in horizontal direction, i.e., from right to left. Closed guard rings would create a low-impedance path in horizontal direction, reducing the effect of spatial separation of the circuit blocks.

The VCO array can be operated from a 5.0 V supply for a low phase noise, or from VCC=3.3 V as the rest of the chip. Several bandgap reference circuits were used to derive stable voltages of VDD=2.5 V for the ECL and CMOS logic. Fig. 9 shows

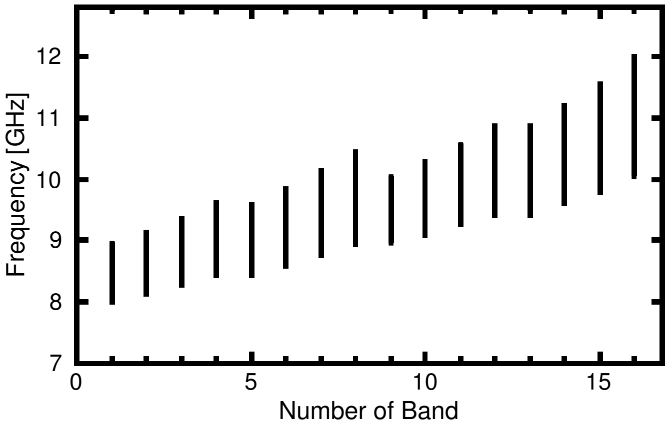

Fig. 9 Measured tuning ranges of the 16 sub-bands

the measured tuning ranges for the 16 sub-bands. Due to the large overlap, there are up to eight possible sub-bands for a given frequency. This allows the best band with respect to phase noise and margin to be selected by an initial calibration procedure. If applied individually to each chip, this also offers the opportunity of compensating parameter variations with the process. The analog sub-band tuning range of 1-2 GHz can then exclusively be used for compensation of temperature and aging effects. In order to determine the contribution of the input reference buffer, a test pad was used after this buffer. An input signal generated by an R&S SMA 100A signal generator was applied to the reference input. The buffer output was then analyzed by an R&S FSUP signal source analyzer. Fig. 10 shows the phase noise of the reference buffer using a 100 MHz reference of -5 dBm power. The measured phase noise at the output of the reference buffer is as low as -144 dBc/Hz at 10 kHz and -151 dBc/Hz at 100 kHz offset. Assuming an amplification of $20\times \log(12\text{ GHz}/100\text{ MHz})=41.6$ dB, this corresponds to an in-band phase noise contribution below -102 dBc/Hz at 10 kHz.

Fig. 11 shows a typical phase noise plot at 9.6 GHz in integer-N mode for three different charge pump currents. Here, we used the following filter parameters according to Fig. 2: R1=680 Ω, C1=4.7 nF, C2=18 pF, R2=2 kΩ, C3=10 pF, R3=2 kΩ, C4=10 pF, R4=1.5 kΩ, R5=1 kΩ, and C_{COARSE}=100 nF. A large charge pump current may reduce the in-band phase noise, since the noise power spectral density of the charge pump is proportional to I_{CP}, whereas the noise transfer function is proportional to $1/I_{\mathrm{CP}}^2$ [4]. The phase noise is as low as -95 to -98 dBc/Hz at 10 kHz, depending on the charge pump current. At 1 MHz, phase noise is as low as -111 dBc/Hz for

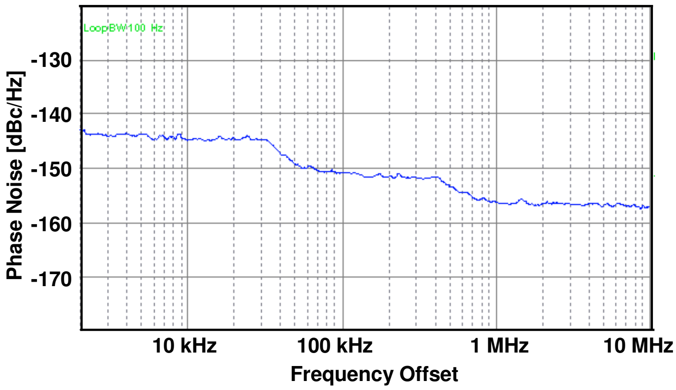

Fig. 10 Measured phase noise spectrum of input buffer

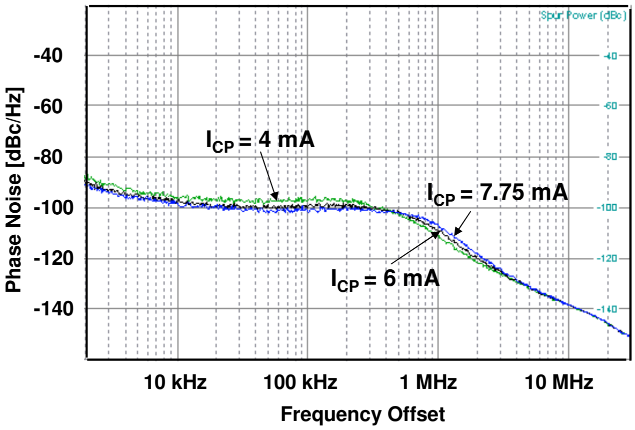

Fig. 11 Measured phase noise spectrum at 9.6 GHz in integer-N mode

I_{CP}=4 mA. A typical phase noise plot for three different frequencies within one sub-band in fractional mode is shown in Fig. 12. Note that the three spectra are very similar despite the large frequency range of 800 MHz. This is the result of biasing the fine tuning voltage in our dual-loop PLL. Phase noise is below -87 dBc/Hz at 10 kHz offset and below -106 dBc/Hz at 1 MHz. The measured in-band phase noise in fractional mode is significantly higher than in integer mode shown in Fig. 11. The following three improvements are planned for the future in order to reduce the phase noise in fractional-N mode: First, following the basic idea of [30], we will add DC offset currents $I_{\mathrm{OS1}} = \alpha_{\mathrm{CP}} I_{\mathrm{CP1}}$ and $I_{\mathrm{OS2}} = \alpha_{\mathrm{CP}} I_{\mathrm{CP2}}$ to the charge pump output currents I_{CP1} and I_{CP2} of CP1 and CP2, respectively. Here, α_{CP} is the CP duty cycle, the optimum value of which is typically 5-15 percent in fractional-N mode. This will improve the linearity of the phase detector (PD), which is composed of PFD and CP. As a result, noise generated by the SDM and folded down to small frequency offsets in the nonlinear PD is reduced, as described in [31]-[35]. Second, the PD linearity will be further improved by reducing turn-on and turn-off time of CP1 in the fine tuning loop. Third, the stan-

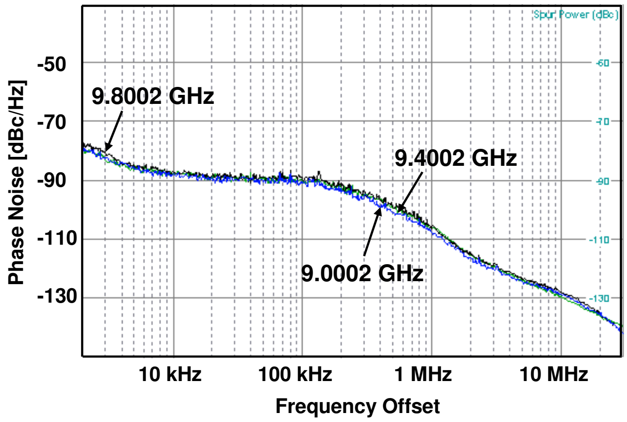

Fig. 12 Measured phase noise spectrum at three different frequencies in fractional mode

dard deviation of the steady-state phase error in fractional-N mode will be reduced by replacing the MASH type SDM with a single-loop SDM. According to [31], this will reduce SDM noise and its in-band noise contribution resulting from noise folding.

A typical output spectrum is shown in Fig. 13, where an 80 MHz crystal reference was used. The spurs at ±80 MHz offset are 64 dB below the carrier. A further reduction

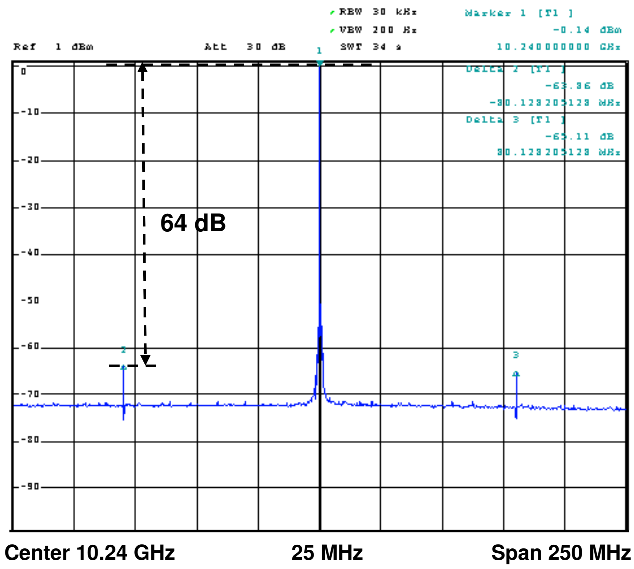

Fig. 13 Output spectrum at 10.24 GHz

of these spurs is possible by increasing the capacitors C2, C3 or C4. However, this might increase the phase noise. According to (2), the two spurs of -64 dBc power correspond

Table 1 Tuning range and phase noise of fractional-N PLLs

Ref.	f_C [GHz]	Tuning [percent]	$\pounds$(10 kHz) [dBc/Hz]	$\pounds$(1 MHz) [dBc/Hz]
[2]	18	8	-85	-108
[7]	13	8	-97	-103
[8]	40	6.2	-60	-90
[9]	18	8	-75	-110
This work	10	40	-87	-106

Table 2 Performance summary

	Measured value
Technology	0.25 μm SiGe BiCMOS
Chip area	7.2 mm^2
Supply voltage	3.3 V (5 V also possible for VCO array)
Current consumption	296 mA at 3.3 V supply
Center frequency	10 GHz
Tuning range	4 GHz (=40 percent)
Frequency at PFD input	80 MHz
Loop bandwidth	$\approx$ 200 kHz
Reference spur level	-64 dBc
Phase noise in integer-N mode	-98 dBc/Hz at 10 kHz; -111 dBc/Hz at 1 MHz
Phase noise in fractional-N mode	-87 dBc/Hz at 10 kHz; -106 dBc/Hz at 1 MHz

to a phase error of 0.05 degree. This value is negligible compared to the total phase error shown in Fig. 6.

Table 1 shows tuning range and typical phase noise values for published fractional-N synthesizers with carrier frequencies f_C $\geq$10 GHz. The table illustrates that the combination of digital and analog tuning allows the tuning range to be significantly extended keeping the phase noise low. Since the target applications are quite different, we refrain from a detailed performance comparison. The VCO array draws 92 mA from a 5 V supply and 77 mA from 3.3 V. The rest of the chip draws 219 mA from a 3.3 V supply. This relatively large power consumption was necessary in order to achieve the high comparison frequency at the PFD input, resulting in power-hungry frequency dividers. According to the application, emphasis was placed on a low phase noise, flexibility and robustness rather than on low power consumption. Table 2 shows a performance summary of the chip.

6 Other Applications

This synthesizer was mainly developed for Ka-band application, where a 8-12 GHz PLL is used for down-conversion from 30 GHz to 20 GHz. Other satellite applications with flexible payloads require frequencies between 1.25 GHz and 3.3 GHz [36]. In the field of wireless communication, cognitive radio multi-mobiles terminals are an interesting topic. Such terminals are to perform an efficient environment spectrum scanning in order to switch accordingly to an appropriate communication standard [37]. They require frequency synthesizers from 880 MHz up to 5.8 GHz.

Fig. 14 shows a multi-octave synthesizer architecture using the 8-12 GHz PLL in conjunction with a dual-modulus prescaler and a cascade of 1:2 dividers. It allows all

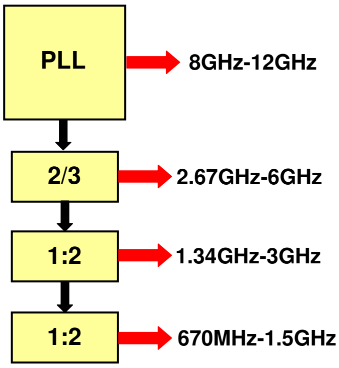

Fig. 14 Schematic of multi-octave synthesizer

frequencies below 6 GHz to be generated by frequency division. Quadrature signals are easily obtained and phase noise reduction by 6 dB per 1:2 division can be expected, since bipolar frequency dividers add only little phase noise in this frequency range [38].

7 Conclusions

We have presented a fractional-N synthesizer for satellite applications. Digital selection between two integrated VCOs was combined with digital and analog VCO tuning for extending the total PLL tuning range to 4 GHz. Only one of the two charge pumps contributes to the overall phase noise and is DC biased at optimum output voltage. This reduces charge pump mismatch over the whole tuning range. Moreover, loop bandwidth and phase noise spectrum are almost independent of the PLL output frequency. This makes the synthesizer performance robust against device parameter variations with process, temperature and aging. For the programmable divider a new ECL synthesis design flow was employed, generating highly reliable, fully synchronous and fully differential ECL designs using VHDL descriptions. The combination of low-noise RF circuitry, high-speed ECL dividers and a digital CMOS block on the same chip allows complex fractional-N PLLs to be designed, where a high comparison frequency at the PFD input is used. As a result, a low close-in phase noise and low reference spurs were achieved.

Acknowledgements This work was supported by the European Space Agency (ESA) and the German DLR (Deutsches Zentrum für Luft- und Raumfahrt). The authors thank the IHP technology team for the fabrication of the test chips.

References

1. Vaucher, C. S., Apeldoorn, O., Apostolidou, M., Dekkers, J., Farrugia, A., Gul, H., Kramer, N., Praamsma, L. (2005). "Silicon-germanium ICs for satellite microwave front-ends," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM 2005)*, Santa Barbara, USA, 196-203.

2. Follmann, R., Köther, D., Kohl, T., Engels, M., Podrebersek, T., Heyer, V., Schmalz, K., Herzel, F., Winkler, W., Osmany, S., Jagdhold, U. (2008). "A single SiGe chip fractional-N 275 MHz...20 GHz PLL with integrated 20 GHz VCO," *IEEE MTT-S International Microwave Symposium*, Atlanta, 355-358.
3. Reynolds, S. K., Floyd, B. A., Pfeiffer, U. R., Beukema, T., Grzyb, J., Haymes, C., Gaucher, B., Soyuer, M. (2006). "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE Journal of Solid-State Circuits*, 41(12), 2820-2831.
4. Osmany, S. A., Herzel, F., Scheytt, J. C., Schmalz, K., Winkler, W. (2007). "An integrated 19-GHz low-phase-noise frequency synthesizer in SiGe BiCMOS technology," in *Proceedings of the 2007 IEEE Compound Semiconductor IC Symposium (CSIC 2007)*, Portland, USA, 191-194.
5. Herzel, F., Glisic, S., Osmany, S. A., Scheytt, J. C., Schmalz, K., Winkler, W., Engels, M. (2008). "A fully integrated 48-GHz low-noise PLL with a constant loop bandwidth," in *Proceedings of the 2008 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Circuits (SiRFIC 2008)*, Orlando, USA, 82-85.
6. Perrot, M. H., Tewksbury III, T. L., Sodini, C. G. (1997). "A 27 -mW fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation,"*IEEE Journal of Solid-State Circuits*, 44(12), 2048-2059.
7. Tiebout, M., Sandner, C., Wohlmuth, H.-D., Da Dalt, N., Thaller, E. (2004). "A fully integrated 13 GHz $\Delta\Sigma$ fractional-N PLL in 0.13 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, 386-387.
8. Pellerano, S., Mukhopadhyay, R., Ravi, A., Laskar, J., Palaskas, Y. (2008). "A 39.1-to-41.6GHz $\Delta\Sigma$ fractional-N frequency synthesizer in 90nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, 484-485.
9. Herzel, F., Osmany, S. A., Schmalz, K., Winkler, W., Scheytt, J. C., Podrebersek, T., Follmann, R., Heyer, H.-V. (2009). "An integrated 18 GHz fractional-N PLL in SiGe BiCMOS technology for satellite communications," in *Proc. of 2009 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2009)*, Boston, USA, 329-332.
10. Cressler, J. D. (1998). "SiGe HBT technology: a new contender for Si-based RF and microwave circuit applications," *IEEE Transactions on Microwave Theory and Techniques*, 46(5), 572-589.
11. Niu, G. (2005). "Noise in SiGe HBT RF technology: physics, modeling, and circuit implementations," *Proceedings of the IEEE*, 93(9), 1583-1597.
12. Osmany, S. A., Herzel, F., Scheytt, J. C., Schmalz, K., Winkler, W. (2009). "An integrated 22-GHz low-phase-noise VCO with digital tuning in SiGe BiCMOS technology," *Electronics Letters*, 45(1), 39-40.
13. Kral, A., Behbahani, F., Abidi, A. A. (1998). "RF-CMOS oscillators with switched tuning," in *Proc. of 1998 Custom Integrated Circuits Conference (CICC'98)*, Santa Clara, USA, 555-558.
14. Lin, T.-H., Kaiser, W. J. (2000). "A 900MHz, 2.5mA CMOS frequency synthesizer with an automatic SC tuning loop," in *Proc. of 2000 Custom Integrated Circuits Conference (CICC'00)*, Orlando, USA, 375-378.
15. Lo, C.-W., Luong, H. C. (2002). "A 1.5-V 900-MHz monolithic CMOS fast-switching frequency synthesizer for wireless applications," *IEEE Journal of Solid-State Circuits*, 37(4), 459-470.
16. Craninckx, J., Steyaert, M. S. J. (1998). "A fully integrated CMOS DCS-1800 frequency synthesizer," *IEEE Journal of Solid-State Circuits*, 33(12), 2054-2065.
17. Koo, Y., Huh, H., Cho, Y., Lee, J., Park, J., Lee, K., Jeong, D.-K., Kim, W. (2002). "A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems," *IEEE J. Solid-State Circuits*, 37(5), 536-542.
18. Herzel, F., Fischer, G., Gustat, H. (2003). "An integrated CMOS RF synthesizer for 802.11a wireless LAN," *IEEE Journal of Solid-State Circuits*, 38(10), 1767-1770.
19. Williams, S., Thompson, H., Hufford, M., Naviasky, E. (2004). "An improved CMOS ring oscillator PLL with less than 4ps RMS accumulated jitter," in *Proc. of 2004 Custom Integrated Circuits Conference (CICC'04)*, San Jose, USA, 151-154.
20. Wu, T., Hanumolu, P. K., Mayaram, K., Moon, U.-K. (2007). "A 4.2 GHz PLL frequency synthesizer with an adaptively tuned coarse loop," in *Proc. of 2007 Custom Integrated Circuits Conference (CICC'07)*, San Jose, USA, 547-550.
21. Aparicio, R., Hajimiri, A. (2002). "A noise-shifting differential Colpitts VCO," *IEEE Journal of Solid-State Circuits*, 37(12), 1728-1736.

22. Fard, A., Andreani, P. (2007). "An analysis of $1/f^2$ phase noise in bipolar Colpitts oscillators (with a digression on bipolar differential-pair LC oscillators)," *IEEE Journal of Solid-State Circuits*, 42(2), 374-384.
23. Mazzanti, A., Andreani, P. (2008). "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE Journal of Solid-State Circuits*, 43(12), 2716-2729.
24. Winkler, F., Heyer, H.-V., Herzel, F., Folio, B.-M., Glass, B., Miquel, C. (2008). "First time common synthesis and simulation of ECL and CMOS parts at a BiCMOS chips based on the IHP SGB25V library," in *Proceedings of the Second International Workshop on Analog and Mixed Signal Integrated Circuits for Space Applications (AMICSA 2008)*, Cascais, Portugal.
25. Gustat, H., Jagdhold, U., Winkler, F., Appel, M., Kell, G. (2008). "Differential ECL/CML synthesis for SiGe BiCMOS," in *Proceedings of the 2008 IEEE Compound Semiconductor IC Symposium (CSIC 2008)*, Monterey, USA, 1-4.
26. Knoll, D., Heinemann, B., Barth, R., Blum, K., Borngräber, J., Drews, J., Ehwald, K.-E., Fischer, G., Fox, A., Grabolla, T., Haak, U., Höppner, W., Korndörfer, F., Kuck, B., Marschmeyer, S., Richter, H., Rücker, H., Schley, P., Schmidt, D., Scholz, R., Senapati, B., Tillak, B., Winkler, W., Wolanski, D., Wolf, C., Wulf, H.-E., Yamamoto, Y., Zaumseil, P. (2004). "A modular, low-cost SiGe:C BiCMOS process featuring high-fT and high-BV CEO transistors," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Montreal, Canada, 241-244.
27. Kim, S., Lee, K., Moon, Y., Jeong, D.-K., Choi, Y., Lim, H.-K. (1997). "A 960-Mb/s/pin interface for skew-tolerant bus using low jitter PLL," *IEEE Journal of Solid-State Circuits*, 32(5), 691-700.
28. Lam, C., Razavi, B. (2000). "A 2.6-GHz/5.2-GHz frequency synthesizer in 0.4-μm CMOS technology," *IEEE Journal of Solid-State Circuits*, 35(5), 788-794.
29. Osmany, S. A., Herzel, F., Schmalz, K., Winkler, W. (2007). "Phase noise and jitter modeling for fractional-N PLLs," *Advances in Radio Science*, vol. 5.
30. Chien, H.-M., Lin, T.-H., Ibrahim, B., Zhang, L., Rofougaran, M., Rofougaran, A., Kaiser, W. J. (2004). "A 4GHz fractional-N synthesizer for IEEE 802.11a," *2004 Symposium on VLSI Circuits Digest of Technical Papers*, Honolulu, USA, 46-49.
31. De Muer, B., Steyaert, M. S. J. (2003). "On the analysis of $\Delta\Sigma$ fractional-N frequency synthesizers," *IEEE Transactions on Circuits and Systems II: Analog Digit. Signal Processing*, 50(11), 784-793.
32. Riley, T. A. D., Filiol, N. M., Du,Q., Kostamovaara, J. (2003) "Techniques for in-band phase noise reduction in $\Delta\Sigma$ synthesizers," *IEEE Transactions on Circuits and Systems II: Analog Digit. Signal Processing*, 50(11), 794-803.
33. Pamarti, S., Jansson, L., Galton, I. (2004) "A wideband 2.4-GHz delta-sigma fractional-N PLL with 1-Mb/s in-loop modulation," *IEEE Journal of Solid-State Circuits*, 39(1), 49-62.
34. Arora, H., Klemmer, N., Morizio, J. C., Wolf, P. D. (2005). "Enhanced phase noise modeling of fractional-N frequency synthesizers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(2), 379-395.
35. Hedayati, H., Bakkaloglu, B., Khalil, W. (2006). "Closed-loop nonlinear modeling of wideband $\Sigma\Delta$ fractional-N frequency synthesizers," *IEEE Trans. Microw. Theory Tech.*, 54(10), 3654-3663.
36. Thornber, M., Thomas, G., Leineweber, T. (2008). "Integrated SiGe PLL synthesizer for space applications," in *Proc. of ESA Workshop on Advanced Flexible Telecom Payloads*, Noordwijk, The Netherlands, 333-340.
37. Valenta, V., Baudoin, G., Villegas, M. (2008). "Phase noise analysis of PLL based frequency synthesizers for multi-radio mobile terminals," in *Proc. of 3rd International Conference on Cognitive Radio Oriented Wireless Networks and Communications*, Singapore, 1-4.
38. Herzel, F., Winkler, W. (2005). "A 2.5-GHz eight-phase VCO in SiGe BiCMOS technology," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, 52(3), 140-144.

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