

A Fully Integrated 48-GHz Low-Noise PLL with a Constant Loop Bandwidth

Frank Herzel¹, Srdjan Glisic¹, Sabbir A. Osmany¹, J. Christoph Scheytt¹, Klaus Schmalz¹,
Wolfgang Winkler¹, and Michael Engels²

¹IHP, Im Technologiepark 25, D-15236 Frankfurt (Oder), Germany

²IMST GmbH, Carl-Friedrich-Gauß-Str. 2, D-47475 Kamp-Lintfort, Germany

in *Proc. of the 2008 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF 2008)*, Orlando, USA, Jan. 2008, pp. 82-85.

Abstract — We present a dual-loop PLL architecture for low-noise frequency synthesizers. The approach is experimentally verified for a 48 GHz PLL in 0.25 μm SiGe BiCMOS technology intended for a 60 GHz wireless transceiver. The design employs two parallel charge pumps one of which dominates the loop dynamics and is biased at optimum output voltage. This equalizes the loop bandwidth and reduces charge pump mismatch.

Index Terms — BiCMOS, Dual-loop PLL, Frequency Synthesizer, Silicon-Germanium, 60 GHz.

I. INTRODUCTION

The 60 GHz band is perfectly suited for wireless short-range communications at high data rates for its huge amount of license-free bandwidth. Silicon-based solutions are especially interesting here for low-cost implementations [1]-[4]. In order to convert the baseband signal to RF and vice versa, stable frequency sources are required, which are usually generated by a phase-locked loop (PLL) controlled by a crystal oscillator. The PLL phase noise is critically here, especially in OFDM systems [5]. A first PLL for a 60 GHz system was presented in [6], where a VCO oscillating at the fundamental frequency of 56 GHz was employed. Using a sliding-IF architecture similar to [7], the required PLL frequency can be reduced to 80 percent of the RF, that is, to 48 GHz. This reduces power consumption, complexity, facilitates image rejection and eliminates LO pulling in transmitters. A first 48 GHz silicon-based PLL was presented in [8]. The performance requirements imply several conflicting demands such as a wide tuning range, low phase noise, low spur level, low power consumption, predictable settling behavior, and low complexity.

The goal of our paper is to present a simple PLL architecture, where a wide tuning range and a good noise performance can be achieved simultaneously, and which

has a constant loop bandwidth over the whole tuning range. This eliminates the need for digital bandwidth control. The performance of the critical charge pump is improved by optimum output biasing, which may reduce the in-band phase noise.

II. PLL ARCHITECTURE

Integrated PLLs in the mm-wave range must typically have a tuning range of a few GHz to compensate variations of the device parameters with process and temperature. This causes a high phase noise of the voltage-controlled oscillator (VCO), the charge pump (CP) and the low-pass filter (LPF). This problem is exacerbated in fully integrated PLLs by the limited size of integrated capacitors. In order to reduce the noise of CP and LPF and the spur level, a dual-loop PLL was proposed in [9], where a high-current charge pump controls a fine tuning VCO input, while a coarse tuning VCO input is controlled by a low-current charge pump. The disadvantage of this approach is that for one PLL output frequency an infinite number of control voltage combinations V_{COARSE} , V_{FINE} exists to generate the desired frequency. Since in integrated PLLs, the VCO gain strongly depends on the control voltages, this ambiguity results in an unpredictable loop bandwidth. One possibility to equalize the loop bandwidth is a digitally controlled charge pump current, which requires a large design effort. The control voltages of the PLL in [9] may approach the rail voltages V_{DD} and V_{SS} , resulting in a poor charge pump performance, increasing phase noise and spur level. In a modified dual-loop design [10] the two VCO control inputs have been connected through a large resistor. This eliminates the ambiguity for V_{COARSE} and V_{FINE} . But still the fine loop control voltage will vary over frequency resulting in a frequency dependent loop bandwidth. Fig. 1 shows a

schematic view of the proposed PLL. The fine tuning input is controlled by a high-current CP connected to a second-order low-pass filter, while the coarse tuning input is controlled by a low-current CP loaded with a large capacitor to ground.

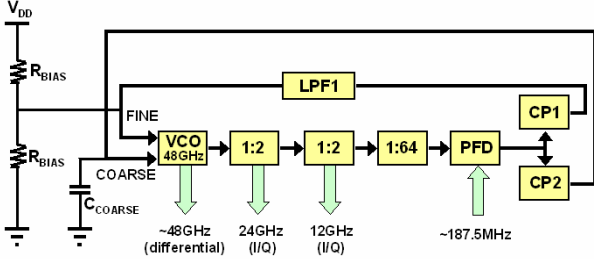


Fig. 1. Schematic view of dual-loop PLL including fine tuning biasing.

The two parallel tuning loops share the frequency divider and the phase-frequency detector (PFD) in order to save power. Our approach architecture is similar to that in [9], but entails an important improvement. Two large resistors of size R_{BIAS} connect the fine tuning VCO input to a supply and the ground. It is advisable to use a separate supply V_{DD} for the voltage divider or to derive it from the VCO supply to avoid noise coupling from other circuitry, especially digital, into the VCO. The average fine tuning voltage is $V_{DD} / 2$, resulting in an optimum output voltage bias of the high-current charge pump CP1, regardless of the PLL output frequency. As a result, CP mismatch can be reduced. Since the fine loop tuning voltage is always given by the bias resistors, the charge pump does not have to be optimized for flat current over output voltage. This significantly reduces the required size of the charge pump, because short-gate-length transistors with high channel-length modulation can be used. Additionally, a lower CP mismatch will reduce spurs and in-band phase noise, especially in fractional-N PLLs [11]. The output voltage of the second charge pump CP2 for coarse tuning is of coarse not constant. This charge pump will, therefore, suffer from mismatch as the PLL output frequency moves toward the boundaries of the tuning range. But, since the current of CP2 is small and the output is loaded by a large capacitor only, the effect on phase noise and spurs is small [9]. Another advantage of our approach compared to [9] and [10] is the fact that the PLL loop bandwidth is independent of the output frequency, provided that the effect of the coarse tuning loop on the settling behavior is negligible.

Beside these advantages, our topology entails three potential disadvantages. First, the total tuning range is limited to the coarse tuning range. For a tuning range ratio of 10:1 as used here, this might reduce the PLL tuning range by about nine percent, which is, however, still as large as ten times the fine tuning range. Therefore, we consider this a minor drawback. The second potential disadvantage is the fact that the settling behavior might be affected by the two biasing resistors. Third, the biasing resistors add thermal noise enhancing the phase noise.

In section III we will show that with proper sizing of R_{BIAS} , neither the frequency settling nor the phase noise are significantly affected.

III. SIMULATION RESULTS

Fig. 2 shows the simulated phase noise for two values of R_{BIAS} and for the case without biasing resistors. Obviously, for $R_{BIAS} > 500 \text{ k}\Omega$ the effect of the biasing resistors on the loop dynamics is negligible. The same holds for the thermal noise of these resistors, which also affects the total phase noise spectrum.

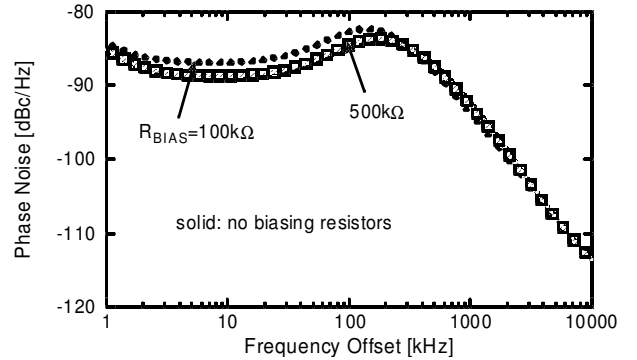


Fig. 2. PLL phase noise for $R_{BIAS} = 100 \text{ k}\Omega$ (circles), $500 \text{ k}\Omega$ (squares) and without biasing resistors (solid line).

In order to investigate the effect of the biasing resistors in the time domain, we performed a behavioral simulation for $R_{BIAS} = 500 \text{ k}\Omega$ and for the case without biasing resistors. The constant fine tuning gain is $K_1 = 100 \text{ MHz/V}$, and the coarse tuning gain is $K_2 = 1 \text{ GHz/V}$. Beside the tuning voltages V_{FINE} and V_{COARSE} , we monitor the effective tuning voltage $V_{EFF} = [K_1 / (K_1 + K_2)] V_{FINE} + [K_2 / (K_1 + K_2)] V_{COARSE}$ representing the sum of the two control voltages weighted with the corresponding VCO gain. This quantity is suited for investigating the frequency settling, since the momentary VCO frequency is a linear function of V_{EFF} . Fig. 3 shows the settling behavior for the two cases. Obviously, in the case of biasing the fine tuning

voltage approaches the value $V_{DD} / 2 = 1.25$ V. Interestingly, the effective voltage settles much faster than the fine and coarse voltages. After the settling of V_{EFF} , the fine and coarse tuning voltages drift to their final values in opposite direction with slew rates in proportion to the corresponding inverse VCO gain.

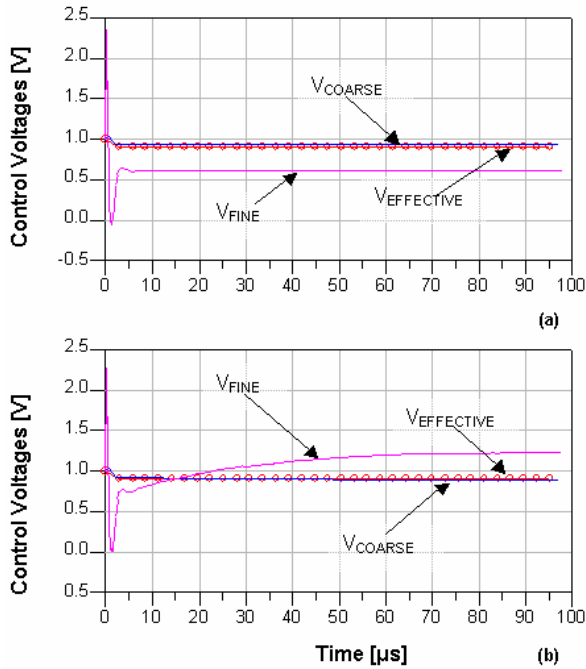


Fig. 3. Coarse, fine and effective tuning voltage versus time for the case without biasing resistors (a) and with resistors (b).

During this time, the effective voltage and the PLL output frequency have already settled. Fig. 4 shows the effective control voltages with and without CP biasing

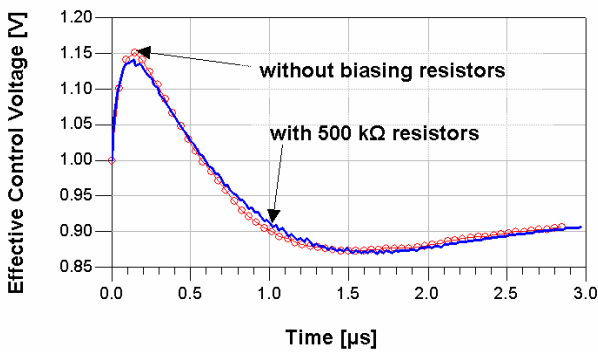


Fig. 4. Effective tuning voltage versus time for the case without biasing resistors and with resistors.

As evident from this figure, the small-signal frequency settling behavior is hardly affected by the biasing resistors.

IV. MEASUREMENTS

We have fabricated two versions of the synthesizer in a $0.25 \mu\text{m}$ SiGe BiCMOS process with three thin and two thick metal layers [12]. The first version has no biasing resistors and has been described in [8]. Measured phase noise at 1 MHz offset was below -98 dBc/Hz over a tuning range from 47.2 to 49.6 GHz. In the second version, the biasing resistors are added at the fine tuning VCO input according to Fig. 1. The targeted bandwidth was increased to 150 kHz for phase noise minimization. Fig. 5 shows the chip photo of the PLL including biasing resistors.

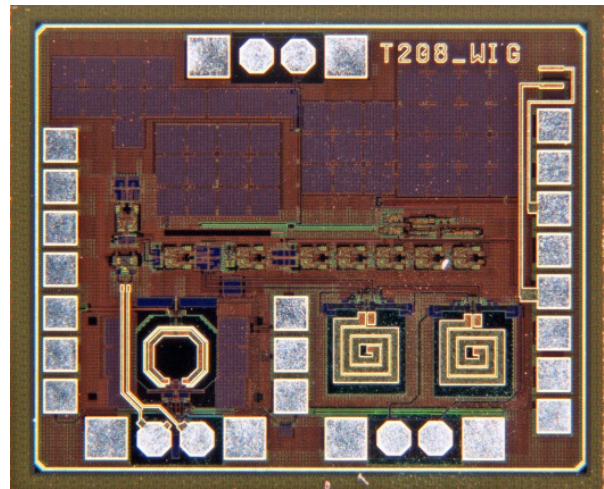


Fig. 5. Chip photo of the PLL with biasing resistors.

The bandwidth was measured for both versions by phase modulating the input frequency and monitoring the level of sidebands in the PLL output spectrum by using a spectrum analyzer. Fig. 6 shows the result for a low modulation frequency of 20 kHz.

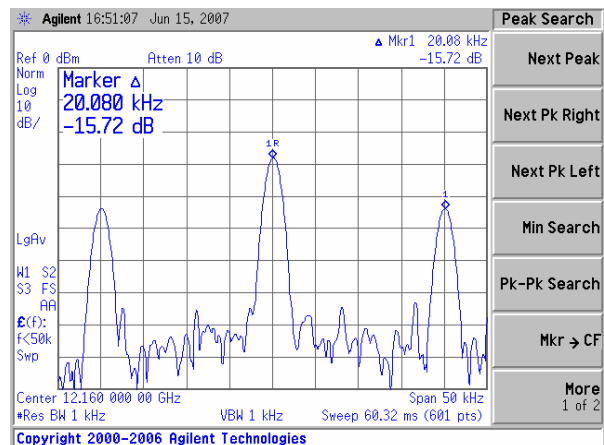


Fig. 6. PLL output spectrum at 12 GHz with a 20 kHz phase modulated reference signal.

For a modulation frequency of 150 kHz the sidebands are 3dB lower than in Fig. 6. The bandwidth at a PLL output frequency of $4 \times 12.16 \text{ GHz} = 48.64 \text{ GHz}$ is, therefore, 150 kHz. Repeating this measurement over the whole PLL tuning range for the two PLL versions we obtain the loop bandwidth as a function of the output frequency depicted in Fig. 7.

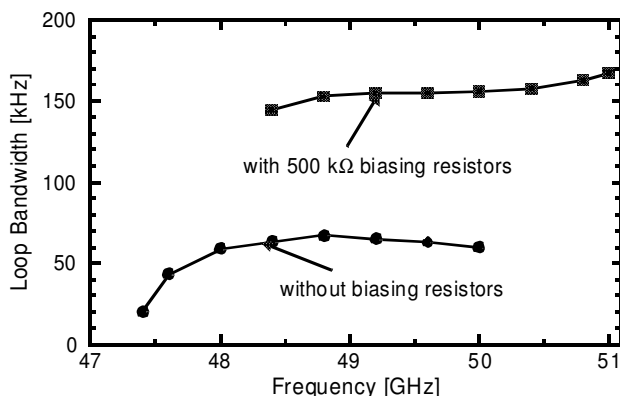


Fig. 7. Measured loop bandwidth as a function of output frequency for the PLL with and without biasing resistors.

In the version without CP output biasing the loop bandwidth strongly depends on the PLL output frequency and is proportional to the VCO gain. In the version including the biasing resistors the loop bandwidth is flat. The loop bandwidth variation is as low as ± 7 percent of the mean value over the tuning range of 2.6 GHz, compared to a factor of three over the same range in the case without biasing resistors. This verifies our simple approach for loop bandwidth equalization, which eliminates the need for digital bandwidth control. Using our architecture, the dominating charge pump CP1 can be optimized for a given bias, e.g., $V_{DD} / 2$. This will minimize the charge pump mismatch for all PLL output frequencies.

V. CONCLUSION

We have presented a 48 GHz PLL consisting of two parallel tuning loops sharing frequency divider and phase-frequency detector. The coarse tuning loop is designed such that its influence on the PLL dynamics is small. The fine tuning VCO input is controlled by a charge pump, the output of which is biased by large resistors at optimum voltage. As a result, charge pump mismatch will be reduced over the whole tuning range. This is expected to be especially useful in fractional-N PLLs. In addition,

significant size reduction of the charge pump is possible. With proper sizing of the loop parameters, the loop bandwidth is almost independent of the PLL output frequency. This allows the settling behavior of the PLL to be predicted, also in the presence of device parameter variations with process and temperature. A digital charge pump control for loop bandwidth equalization is, therefore, not required.

REFERENCES

- [1] P. Smulders, "Exploiting the 60 GHz Band for Local Wireless Multimedia Access: Prospects and Future Directions," *IEEE Communications Magazine*, vol. 40, pp. 140-147, Jan. 2002.
- [2] E. Grass, F. Herzel, M. Piz, Y. Sun, and R. Kraemer, "Implementation Aspects of Gbit/s Communication System for 60 GHz Band," in *Proceedings of the 14th Wireless World Research Forum (WWRF 14)*, San Diego, USA, July 2005.
- [3] B. Razavi, "A 60 GHz CMOS Receiver Front-End," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 17-22, Jan. 2006.
- [4] S. K. Reynolds, B. A. Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer "A Silicon 60 GHz Receiver and Transmitter Chipset for Broadband Communications," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2820-2831, Dec. 2006.
- [5] F. Herzel, M. Piz and E. Grass, "Frequency Synthesis for 60 GHz OFDM Systems," in *Proceedings of the 10th International OFDM Workshop (InOWo'05)*, Hamburg, Germany, Aug. 2005, pp. 303-307.
- [6] W. Winkler, J. Borngräber, B. Heinemann, and F. Herzel, "A Fully Integrated BiCMOS PLL for 60 GHz Wireless Applications," *ISSCC Digest of Technical Papers*, San Francisco, Feb. 2005, pp. 406-407.
- [7] M. Zargari, D. K. Su, C. P. Yue, S. Rabii, D. Weber, B. J. Kaczynski, S. S. Mehta, K. Singh, S. Mendis, B. A. Wooley, "A 5 GHz CMOS Transceiver for IEEE 802.11a Wireless LAN Systems," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1688-1694, Dec. 2002.
- [8] F. Herzel, S. Glisic, and W. Winkler, "Integrated Frequency Synthesizer in SiGe BiCMOS Technology for 60 and 24 GHz Wireless Applications," *Electronics Letters*, vol. 43, pp. 154-156, Feb. 2007.
- [9] F. Herzel, G. Fischer, and H. Gustat, "An Integrated CMOS RF Synthesizer for 802.11a Wireless LAN," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1767-1770, Oct. 2003.
- [10] C. Y. Kuo, J. Y. Chang, and S. I. Liu, "A Spur-Reduction Technique for a 5-GHz Frequency Synthesizer," *IEEE Transactions on Circuits and Systems-I*, vol. 53, pp. 526-533, Mar. 2006.
- [11] X. Mao, H. Yang, and H. Wang, "An Analytical Phase Noise Model of Charge Pump Mismatch in Sigma-Delta Frequency Synthesizers," *Analog Integrated Circuits and Signal Processing*, vol. 48, pp. 223-229, Sep. 2006.
- [12] B. Heinemann et al., "Novel Collector Design for High-Speed SiGe:C HBTs," in *Proc. of the IEDM'02*, San Francisco, Dec. 2002, pp. 775-778.