

## **Damascene metal gate technology: A solution to high-k gate stack challenges?**

Since the late 1960s, the normal fabrication method of CMOS transistors is known as the “gate first” approach. As the name indicates, gate dielectric and gate electrode are made first, i.e. prior to the self-aligned formation of the source (S) and drain (D) junctions by ion-implantation. As long as the gate stack has been made out of polycrystalline silicon and silicon dioxide, process integration was not an issue. Both materials are able to withstand high annealing temperatures and are compatible with reactive ion etching. However, after introducing novel gate stack materials, like high-k gate dielectrics and metal gate electrodes, the situation has been changed completely. These new materials are sensitive and degrade during high-temperature processing. In order to circumvent process-induced gate-stack damage, we have developed a “gate last” process flow, in which the self-aligned gate stack is made after S/D junctions. For the first time, fully functional metal gate MOSFETs with crystalline high-k dielectric have been fabricated by means of chemical mechanical polishing (CMP). Electrical results and details of the “gentle” damascene metal gate technology will be presented. To which extent the “gate last” approach is a general solution to the high-k metal gate challenges will be discussed.