An Integrated 19-GHz Low-Phase-Noise Frequency Synthesizer in SiGe BiCMOS Technology

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***Abstract* — We present a fully integrated phase-locked loop tunable from 17.5 GHz to 19.2 GHz fabricated in a 0.25 µm SiGe BiCMOS technology. The measured phase noise is below –110 dBc/Hz at 1 MHz offset over the whole tuning range. Based on an integer–N architecture, the synthesizer consumes 248 mW and occupies a chip area of 2.1 mm^2 including pads. Quadrature outputs at quarter of the oscillator frequency are produced, which are required in a sliding–IF 24 GHz transceiver. Possible applications include wireless LAN as well as satellite communication. The measured phase noise is the lowest among previously published Si-based integrated synthesizers above 12 GHz.**

***Index Terms* — Phase-locked loop, wireless LAN, SiGe, BiCMOS, phase noise, 24 GHz.**

I. Introduction

Frequency synthesizers above 10 GHz are important for many applications such as wireless LAN at 17 and 24 GHz or ultra-wideband vehicular radar between 22 and 29 GHz. Of special interest is the 24 GHz ISM band, which has been opened for wireless point-to-point communications by the Federal Communications Commission (FCC) [1].

The 24-GHz front-end in [2] uses an intermediate frequency (IF) of 5 GHz requiring a 19 GHz frequency synthesizer for the first down-conversion. Another 24 GHz front-end uses a sliding-IF transceiver architecture, where an LO of 19.2 GHz is required [3]. Another field of applications is the satellite communication, where the lower Ka-band (18-20 GHz) will be used for the down-link [4].

Low-cost implementations for the consumer market require a high integration level, which makes CMOS technology an attractive solution. However, the phase noise is limited by the relatively low supply voltage, which prevents large amplitudes in the voltage-controlled oscillator (VCO). Moreover, the large flicker noise of MOSFETs increases the in-band phase noise of the synthesizer. By contrast, in bipolar oscillators the $1/f^3$ noise corner frequency is as low as 10 kHz for modern SiGe HBT technologies [5]. In addition, the speed of frequency dividers is high enough, even in a quarter-micron technology. An integrated phase-locked loop (PLL) employing frequency dividers working at 58 GHz was presented in [6], where a 0.25 µm SiGe BiCMOS technology was used. Therefore, we consider SiGe BiCMOS a good compromise between phase noise performance and cost for several applications around 19 GHz.

The paper is aimed at a fully integrated PLL combining a relatively large tuning range with a low phase noise. The ultimate goal is a low-phase-noise synthesizer that enables low-cost transceivers in the 24 GHz band using highly efficient modulation schemes such as 16-QAM or 64-QAM OFDM.

II. PLL Architecture

Integrated phase-locked loops at 19 GHz must have a tuning range of 1 GHz or more in order to compensate variations of the device parameters with process and temperature. This increases the noise of the low-pass filter (LPF), the phase-frequency detector (PFD) and the charge pump (CP). Moreover, the level of reference spurs is increased due to the high VCO tuning sensitivity. This suggests to split the tuning range in a slow high-gain path and a fast low-gain path in order to alleviate this problem. Fig. 1 shows a schematic view of such a PLL architecture as used in [6]. Two parallel charge pumps are used to form two parallel

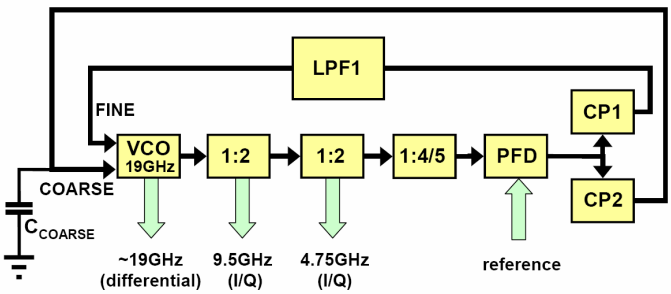

Fig. 1. Schematic view of dual-loop PLL.

control loops. The two loops share the frequency divider and the PFD in order to save power and chip area. The dual-modulus prescaler is preceded with two divide-by-two circuits (DTC). This lowers the input frequency to a moderate value, resulting in low power consumption. Moreover, the quadrature components I and Q of the 5 GHz signal have a low static phase error, since the duty cycle of the 10 GHz signal is very close to 50 percent.

III. Design of Subcircuits

This section briefly describes the different subcircuits of the PLL. Since a BiCMOS technology is employed, we have used both bipolar and CMOS blocks in order to achieve an optimum overall performance. Bipolar transistors were used for the speed-critical blocks (VCO and frequency dividers), while MOSFETs were used for the low-speed blocks (PFD and CP). Fig. 2 shows the schematic of the 19 GHz LC oscillator. The differential VCO in common collector configuration possesses a coarse tuning and a fine tuning input [7].

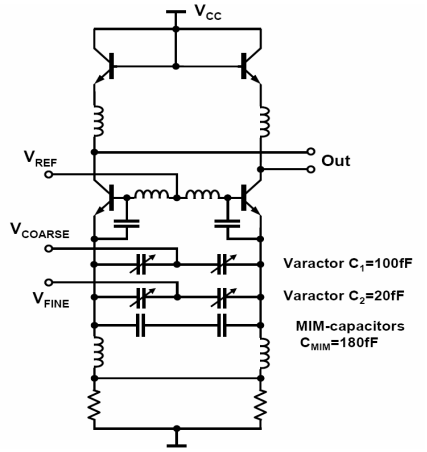

Fig. 2. Schematic view of the voltage-controlled oscillator.

The tank inductor uses the fifth aluminum metal layer with a thickness of 3 µm resulting in a low series resistance and a low parasitic capacitance to the substrate. The separation of the metal from the conductive substrate is as large as 12 µm. Frequency tuning is performed by two symmetric varactors with a capacitance ratio of 1:5. The varactors are MOS-structures with a measured quality factor around 12 over the whole tuning range. Fig. 3 depicts the measured oscillator phase noise spectrum.

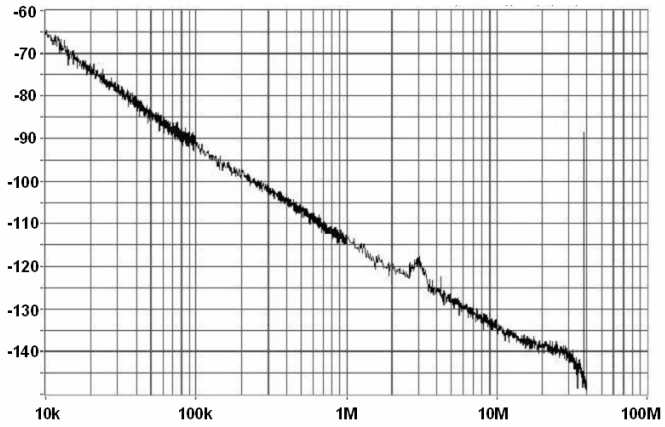

Fig. 3. Measured phase noise of free-running VCO.

The DTC is realized as two latches in a negative feedback loop. Each of the latches is composed of a differential pair and a regenerative pair. The divide-by-four/divide-by-five circuit architecture is taken from [8]. The PFD consists of dynamic logic gates and a NOR gate in the feedback loop. The delay of the NOR gate was adjusted such that both UP pulse and DOWN pulse of the charge pump are briefly activated if the phase error is zero. This eliminates the dead zone of the PFD/CP reducing the resulting jitter. The charge pump is essentially the same as in [9], but with four switchable binary weighted charge pumps in parallel. The current can be digitally controlled from 250 µA to 3750 µA in steps of 250 µA. The second-order low-pass filter is composed of a 75 pF capacitor in series with a 15 kΩ resistor for stability. A 2 pF bypass capacitor is added for spur suppression.

IV. Simulation Results

This section shows the simulated phase noise spectrum and its dependency on charge pump current. In order to estimate the PLL phase noise, we employed a linear third-order PLL model. Fig. 4 shows the simulated two-sided phase noise spectrum and its components.

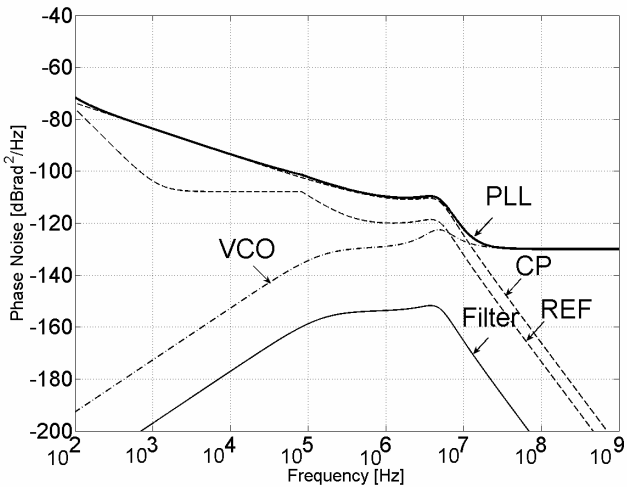

Fig. 4. PLL phase noise spectrum and its components.

As evident from the figure, at very large offsets the phase noise contribution of the VCO dominates. The reference dominates at very low offsets. The in-band phase noise is mainly determined by the charge pump noise. A large charge pump current 3750 µA was used to achieve a large loop bandwidth. Alternatively, a large bandwidth could be produced by a larger loop resistance. From simulations we concluded, however, that this deteriorates the overall phase noise performance. Fig. 5 shows the simulated phase noise for five different charge-pump currents I_{CP}. Obviously, the in-band phase noise is reduced by increasing the current. This is due to the fact that the noise power spectral density of the

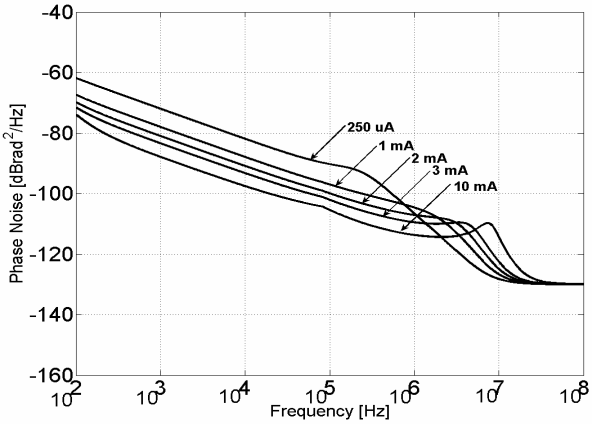

Fig. 5. Simulated phase noise spectrum for different charge-pump currents.

charge pump is proportional to I_{CP}, while the corresponding noise transfer function to the PLL output is proportional to $1/I_{CP}^2$. At very large offsets phase noise is increased with increasing current. However, this part of the spectrum may be irrelevant because it is eliminated after down conversion to baseband and low-pass band filtering.

V. Measurements

The chip was fabricated in a 0.25 µm low-cost SiGe BiCMOS technology using 21 mask steps [14]. The choice of the technology was driven by cost issues and by the available options for low-noise oscillator design. Since the phase noise spectrum of an oscillator is proportional to $1/(V_0^2 Q^2)$, oscillation amplitude V_0 and the quality factor Q of the resonator should be maximized. The bipolar transistors with a high breakdown voltage are, therefore, a useful option for low-phase-noise oscillators, since they allow large amplitudes. Five layers of Al are available, including 2 µm and 3 µm thick upper layers, which allow integrated inductors with a high Q to be designed.

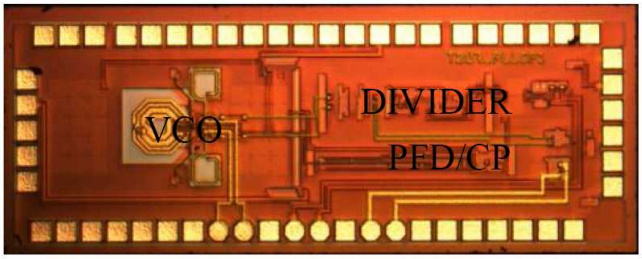

Fig. 6. Chip photograph.

Fig. 6 shows the photograph of the die with an area of 2.4 x 0.85 mm^2 including pads. The RF part (VCO) is on the left side and the digital part (PFD/CP, divider) is on the right side of the die. This reduces the noise coupling from the digital part to the VCO, because the substrate noise is significantly reduced with increasing distance. The measurements were realized after mounting the chip in the cavity of a printed circuit board.

The measured lock range of the synthesizer is 17.45 GHz-19.2 GHz. The output power level is a key issue, since a large and constant LO power is beneficial for the mixer performance in a transceiver. Fig. 7 shows the measured output power with maximum variation of 1 dB within the lock range. The measured output power variation over the temperature is 0.0022 dB / ^{0}C. The synthesizer requires two separate supply voltages, 5 V for the VCO and 2.5 V for the rest. The VCO including buffers draws 30 mA, the PFD/CP draws up to 11 mA, and the whole divider chain draws 28 mA.

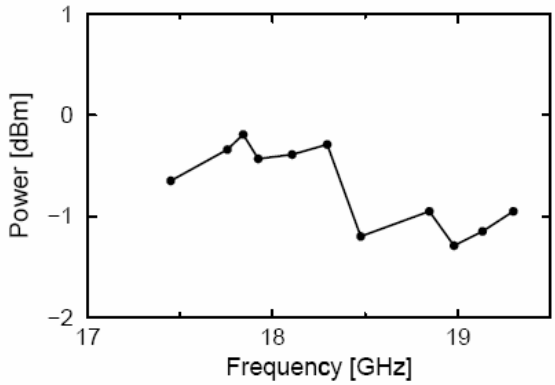

Fig. 7. Measured output power as a function of PLL output frequency.

The phase noise measurement was performed with the AEROFLEX PN9000 system. An Agilent 8257D signal generator was used as the reference. Fig. 8 shows the measured phase noise for two different charge pump currents.

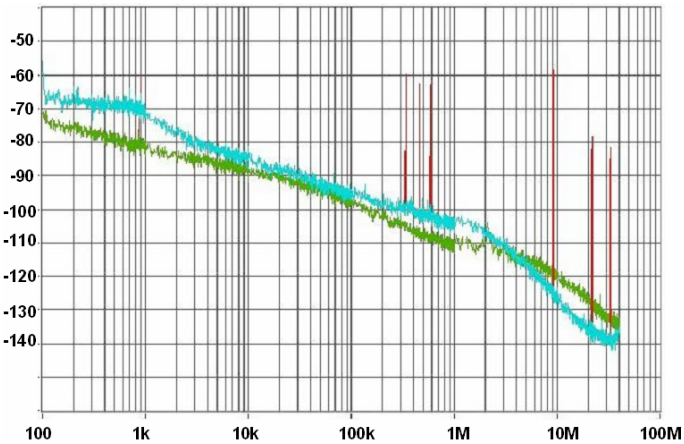

Fig. 8. Measured phase noise spectral density at 19 GHz operation frequency for two different charge pump currents: upper curve 250 µA, lower curve 3750 µA.

With the larger current, the measured phase noise is -99 dBrad^2/Hz at 100 kHz offset and -110 dBrad^2/Hz at 1 MHz offset from the 19 GHz carrier. This matches very well with our predicted values shown in Fig. 4. The measurement shows that the phase noise performance with higher charge pump current degrades at very large offset as discussed in Section IV. However, the phase noise at frequency offsets above 8.5 MHz is not relevant, if an OFDM bandwidth of about B = 17 MHz is assumed, as is used in the IEEE 802.11a standard. The phase noise at two specific offsets is depicted in Fig. 9 as a function of the PLL output frequency.

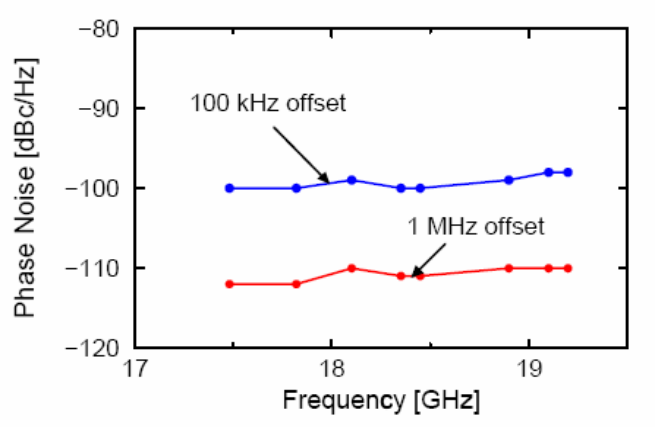

Fig. 9. Measured phase noise spectral versus operation frequency.

In order to compare our phase noise with the state of the art, we have compiled measured values for integrated silicon-based PLLs in Fig. 10. Typically the phase noise at a given

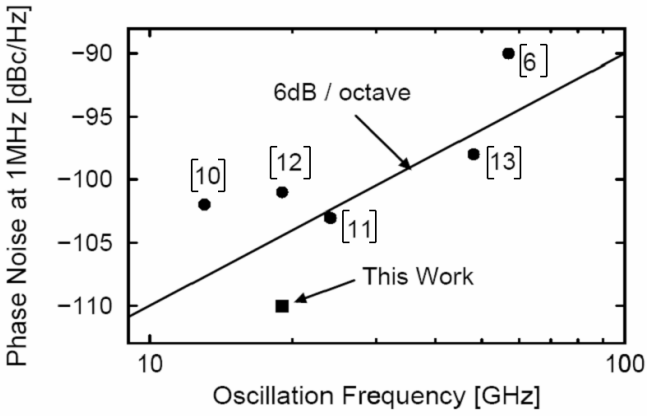

Fig. 10. Measured phase noise at 1 MHz offset.

offset increases roughly in proportion to the squared oscillation frequency. Therefore, we have plotted the phase noise value at 1 MHz as a function of output frequency together with a line having a 6 dB/octave slope shown in Fig. 10. As evident, our phase noise compares favorably with the state of the art.

VI. Conclusion

We have presented an integrated frequency synthesizer fabricated in a 0.25 µm SiGe BiCMOS technology. Based on simulations and measurements, the influence of the charge pump current on phase noise spectrum was discussed. To the best of our knowledge, the measured phase noise at 1 MHz offset normalized to the oscillation frequency is at least 4 dB lower than in all previously published silicon-based integrated frequency synthesizers above 12 GHz.

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