Twinning for Excellence in Reliable Electronics

Annual Newsletter 2025

Year at a Glance

TWIN-RELECT launched in 2024 with a successful kick-off meeting and has made progress through 2025 in advancing Europe's capacity to design reliable electronic systems for critical applications. Key activities include the launch of our first webinar in November on "Bridging EU Innovation in Reliable Electronics Design", the September Business Forum in Volos that brought together academic researchers and European industry partners, and our July scientific workshops on fault modeling and tolerance analysis.

Kick-Off Meeting (2024)

Research Breakthroughs

Tools and methodologies for fault modeling and reliability assessment in advanced semiconductors. Simulation tools for critical applications in space, avionics, and automotive sectors.

Training & Capacity Building

Staff exchanges and joint training between partner institutions. Scientific workshops and research management sessions for early-career researchers.

International Collaboration

Strategic partnerships with European research institutions and industry. Networking events, business forums, and webinars connecting researchers and stakeholders.

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Events

OCT 2024

Kick-Off Meeting

TWIN-RELECT's October 2024 kick-off meeting brought the four-partner consortium together to establish collaboration frameworks, align research objectives, and plan knowledge transfer activities. The meeting set the foundation for joint research initiatives aimed at advancing reliable electronics design across Europe.

Training Week in Montpellier (CNRS)

JAN 2025

The first TWIN-RELECT Training Week (January 06 - 10, 2025) at the University of Montpellier brought together researchers from all partner institutions for knowledge transfer and capacity building in reliable electronics design. Participants engaged in expert lectures, hands-on training sessions, and collaborative research discussions while accessing CNRS's advanced research facilities and tools.

JAN 2025

TWIN-RELECT Attends Research Staff Conference in Manchester

TWIN-RELECT attended the staff conference at the University of Manchester (January 15, 2025), bringing together researchers from all partner institutions to discuss project progress and strengthen collaborative ties. The meeting provided opportunities to explore expanded research initiatives and share best practices across the consortium.

Training Week in Montpellier

Research Staff Conference in Manchester

Events

FEB 2025

TAICHIP Winter School in IHP

The 1st TAICHIP Winter School (February 10 - 12, 2025) hosted 42 researchers from seven countries at IHP Microelectronics in Frankfurt, focusing on reliable AI chip design. TWIN-RELECT participated alongside complementary projects, with participants engaging in lectures, PhD presentations, laboratory tours, and international networking opportunities.

TWIN-RELECT Attends TUZ Workshop

FEB 2025

TWIN-RELECT participated in the 37th TUZ Workshop on Test Methods and Reliability of Circuits and Systems (February 23 - 25, 2025) in Berlin, Europe's leading forum for discussing testing and reliability challenges. The event provided opportunities to share project research outcomes and strengthen connections with the international reliability engineering community.

APR 2025

TWIN-RELECT Presents at COIN-3D Business Forum Volos 2025

TWIN-RELECT presented its research outcomes at the COIN-3D Business Forum Volos 2025 (April 28 - May 02, 2025), showcasing project progress in reliable electronics design. The presentation strengthened TWIN-RELECT's visibility within the European microelectronics research community and fostered valuable networking opportunities.

TAICHIP Winter School in IHP

TUZ Workshop Presentation

Events

MAY 2025

TWIN-RELECT Presents at TAU 2025 Workshop

TWIN-RELECT presented its research at the TAU 2025 Workshop (May 1 - 2, 2025) on Timing Issues in Digital Systems in Seaside, California. The presentation highlighted project advances in reliable electronics design and connected TWIN-RELECT with the international digital systems and timing optimization community.

Training Week in Frankfurt (IHP)

MAY 2025

TWIN-RELECT's 2nd Training School took place at IHP in Frankfurt (May 19 - 21, 2025), combining technical training in reliable electronics with research management and administration workshops. The event brought together researchers and staff from all partner institutions for advanced capacity building and knowledge exchange.

JUL 2025

1st Scientific Workshop: Fault Modeling and Tolerance Analysis in Volos

TWIN-RELECT organized its 1st Scientific Workshop in Volos on fault modeling and fault tolerance techniques for reliable electronics. The event brought together European researchers and industry professionals discussing advanced methodologies for critical applications in space, avionics, and automotive sectors. The workshop strengthened TWIN-RELECT's visibility and fostered collaboration with complementary European research initiatives.

Training Week in IHP

Scientific Workshop in Volos

Events

JUL 2025

2nd Research Management & Administration Workshop

TWIN-RELECT organized its 2nd Research Management & Administration Workshop in Volos, bringing together consortium partners and experts from the European Space Agency, CNRS, University of Montpellier, University of Manchester, and IHP. The three-day event covered leadership, proposal funding, research management best practices, and Horizon Europe proposal development.

TWIN-RELECT Business Forum in Volos

SEP 2025

TWIN-RELECT organized the Business Forum in Volos, bringing together industry leaders, startups, researchers, and professionals from across Europe. The event featured keynote talks from leading companies in circuit design, space applications, and semiconductors, alongside panel discussions and networking sessions exploring collaboration opportunities in reliable electronics innovation.

NOV 2025

1st TWIN-RELECT Webinar: "Bridging EU Innovation in Reliable Electronics Design"

TWIN-RELECT held its first webinar on November 7, 2025, gathering experts from six complementary EU-funded projects—TWIN-RELECT, AIDA4Edge, COIN-3D, RADNEXT, RESIST, and HCCC—to share insights on reliable electronics design and AI at the edge. Presentations covered intelligent error detection, fault tolerance techniques, adaptive systems, and space-grade reliability.

Research Management Workshop in Volos

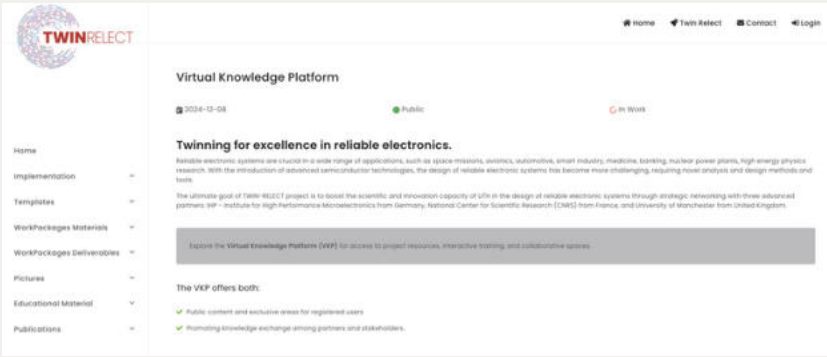
Business Forum in Volos

Milestones

Launch of Project Website and Virtual Knowledge Platform

Launched in October 2024, the TWIN-RELECT website serves as the project's digital hub for news, events, resources, and updates. Hosted by the University of Thessaly, the website is continuously updated throughout the project with new activities, reports, deliverables, publications, upcoming events, and educational opportunities.

The TWIN-RELECT Virtual Knowledge Platform (VKP) was launched under the University of Thessaly's domain at . Acting as both a collaborative workspace and a long-term knowledge repository, the VKP provides partners and stakeholders with easy access to project literature, deliverables, templates, visual materials, educational resources, and publications. The platform is structured for public and private access, supporting interactive training, resource sharing, and secure collaboration, making it a cornerstone for project communication and knowledge exchange in reliable electronics research.



Submitted Deliverables

Deliverable (Number)	Deliverable (Name)	Work package number	Leader	Type	Dissemination Level	Delivery Date	Status
D7.1	Ist Data Management Plan	WP7	UTH	DMP	PU	M6	Submitted
D6.1	Ist Dissemination, Communication and Exploitation Plan	WP6	UTH	R	PU	M4	Submitted
D5.4	Ist Report on Virtual Knowledge Platform	WP5	UTH	R	PU	M4	Submitted
D4.5	Ist Report on Stakeholders Network	WP4	UTH	R	PU	M6	Submitted
D4.1	Networking plan	WP4	MAN	R	PU	M5	Submitted
D3.1	Research Management and Administration Training Plan	WP3	IHP	R	PU	M4	Submitted
D2.1	Scientific Capacity Enhancement Plan	WP2	CNRS	R	PU	M3	Submitted
D1.1	Research Plan	WP1	UTH	R	PU	M6	Submitted

TWIN-RELECT has successfully submitted several key deliverables in the first months of the project, marking important progress in

- planning
- networking, and
- capacity building.

Find a list with our deliverables here!

Scientific Outputs

DATE 2025

Multi-Partner Project: Twinning for Excellence in Reliable Electronics (TWIN-RELECT)

TWIN-RELECT partners published a paper at IEEE during the Design, Automation and Test in Europe Conference (DATE) 2025, titled "Multi-Partner Project: Twinning for Excellence in Reliable Electronics (TWIN-RELECT)" presenting the Horizon Europe Twinning project's overarching vision and scientific objectives. The work introduces TWIN-RELECT as a collaborative initiative aimed at strengthening scientific expertise in designing reliable integrated circuits—a critical capability as semiconductor technology advances and IC complexity increases. Addressing the growing reliability challenges in mission-critical applications such as space missions, avionics, automotive, medicine, banking, automated industry, and wireless communication networks, the paper outlines the project's primary scientific goal: developing a novel and more efficient European Electronic Design Automation (EDA) tool-chain for designing reliable chips. This foundational publication establishes the research directions and collaborative framework guiding TWIN-RELECT's joint research activities across its partner institutions.

ASYNC 2025

Post-Placement Timing Optimisations on Asynchronous Designs

A paper presented under the TWIN-RELECT project at the IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC) introduces the Asynchronous In-Place Optimisation (AIPO) algorithm for enhancing post-placement-and-routing timing in asynchronous control and Bundled-Data circuits. Operating in a closed-loop system with Asynchronous Static Timing Analysis (ASTA), AIPO performs gate resizing and buffer insertion while evaluating timing impact through advanced timing models such as Coupled Capacitance and Switching (CCS) and well-established wire RC representations. The algorithm works in conjunction with a placement legaliser to resolve cell overlaps and achieve timing closure. Demonstrated across 17 benchmark designs spanning three technology libraries—IHP 250nm, IHP 130nm, and GF 22nm—AIPO achieved timing improvements of 33% and 30% for the IHP and GF libraries, respectively, effectively mitigating the adverse effects of cell placement and wire RC interconnect delays while navigating the Area-Delay Pareto trade-off.

Scientific Outputs

SMACD 2025 Publications

Prediction of Single Event Transient Propagation Using Machine Learning Models

"Prediction of Single Event Transient Propagation Using Machine Learning Models" presented under the TWIN-RELECT project analyzes the applicability of machine learning models for predicting Single Event Transient (SET) pulse width variation during propagation through standard combinational cells. Ten regression models were trained on a dataset generated from SPICE simulations conducted for INV, NAND2, and NOR2 gates from IHP's 130 nm standard cell library, with analysis considering input pulse width and polarity, gate size factors, load gate dimensions, supply voltage, and temperature. Results demonstrated that specific models provide optimal prediction accuracy for individual gates, with trained models also capable of predicting SET pulse width changes across combinational paths, though with reduced accuracy compared to single-gate analysis. This work advances the understanding of SET behavior in digital circuits and supports the development of automated machine learning-based tool-flows for comprehensive SET analysis in reliable electronics design

Compact SER Models via Model Order Reduction of Diffusion-Based Charge Collection

Addressing the critical challenge of reliable Soft Error Rate (SER) estimation in contemporary VLSI designs under ionizing radiation, a paper titled "Compact SER Models via Model Order Reduction of Diffusion-Based Charge Collection" proposes a compact SER modeling approach based on Moment Matching combined with Extended Krylov Subspace techniques. The work overcomes computational limitations of traditional physics-based methods by leveraging the inherent linearity of the diffusion equation and employing the Finite Difference Method in three dimensions to construct a discrete representation. Experimental results demonstrate computational speedups of up to 21× while maintaining the accuracy of full numerical models, enabling scalable and efficient SER analysis across various technological nodes and supporting robust design practices for radiation-prone environments.

Fault Injection Attacks Based on Layout-Driven SER Analysis

As CMOS technology continues to downscale, the vulnerability of integrated circuits to reliability threats such as Soft Errors and Hardware Trojans has considerably increased, presenting compounded security challenges. The paper "Fault Injection Attacks Based on Layout-Driven SER Analysis" presents a comprehensive layout-based analysis methodology that identifies the most impactful circuit regions where faults can be intentionally injected, focusing on Single Event Multiple Transients (SEMTs) generation and propagation through circuits by leveraging detailed layout information to pinpoint critical vulnerability areas. Experimental results on ISCAS '89 benchmarks demonstrate a significant average increase of approximately 32% in Soft Error Rate when targeted fault injection is applied, underscoring the critical need for more robust system design strategies to combat reliability-based threats in modern integrated circuits.

Scientific Outputs

DFTS 2025 Publications

Special Session Paper: Simulation Methodologies and Experiments for Reliability Analysis of Devices in Radiation Harsh Environment

TWIN-RELECT recently presented the joint paper "Simulation Methodologies and Experiments for Reliability Analysis of Devices in Radiation Harsh Environments" in a special session at the 38th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS 2025). The publication, a collaboration between students from the University of Thessaly and University of Montpellier/CNRS, focuses on the growing challenge of ensuring reliable operation of electronic systems deployed in radiation-prone sectors like aerospace, automotive, and remote sensing. The paper details a novel simulation framework for evaluating Single Event Transients in clock networks using the integrated PREDICSEE and UPSET SET analysis tools, investigates the fault resilience of Dynamic Neural Networks (DyNNs) in edge AI accelerators, and reports experimental findings from neutron irradiation tests on a hardened RISC-V SoC implemented in SRAM-based FPGA—comparing its vulnerability to flash-based technologies.

Compact SER Models for Line-Source-Induced Charge Collection Using Model Order Reduction

The TWIN-RELECT team, in partnership with COIN-3D, presented the paper "Compact SER Models for Line-Source-Induced Charge Collection Using Model Order Reduction" at 38th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS 2025). As soft errors from cosmic rays and particle strikes pose increasing reliability challenges for modern electronics, especially in aerospace, automotive, and high-performance computing, this work introduces an efficient modeling strategy to address SER estimation's computational demands at advanced technology nodes. The approach leverages model order reduction by discretizing the physical diffusion-collection mechanism of charge in 3D space and applying Extended Krylov Subspace and Moment Matching techniques. This enables the analysis of particle-induced charge collection dynamics with significant computational speedup and preserved accuracy, supporting robust and reliable system design for radiation-prone environments.

DFTS Presentations

Exchange Visits

Exchange in University of Thessaly

In October 2025, a Post-doctoral Research Associate from the University of Manchester's Advanced Processing Technologies Group conducted a week-long visit to the University of Thessaly to advance training and collaborative research in asynchronous communication for neuromorphic computing. The visit focused on training UTH's team in synthesizing asynchronous bundled-data networks-on-chip (NoCs) using mainstream CAD tools, with emphasis on the TaBuLA architecture and its application to neural accelerators like NVDLA and NeoCorAI. A key research milestone was achieved through joint development of synthesis scripts for a new TaBuLA variant compatible with Design-for-Test methodologies. The exchange included hands-on supervision of UTH students, enabling the local team to independently design and conduct reliability analysis on emerging AI devices. This collaboration addresses critical gaps in testing and fault tolerance for asynchronous neuromorphic systems, particularly spike routing faults that have been significantly underexplored.

Exchange in IHP

A PhD student from the University of Thessaly visiting IHP engaged in practical, hands-on training focused on fault characterization at the circuit level and the development of fault-tolerant design methodologies. The visit spanned from 7th of October to 15th of December. The training program covered electrical characterization of transient and permanent fault effects in standard cells through SPICE simulations, fault injection in digital designs and Neural Networks using open-source logic fault injectors, and application of AI-driven prediction and classification methods for assessing SET generation and propagation. Moreover, the program included Reliability Analysis of Neural Networks as well as studying and mitigating the aging effects on circuits. The student gained expertise in assessing the reliability of a circuit, designing fault tolerant standard cells, implementing selective fault tolerance based on analytical assessment, and developing on-chip fault detection sensors with reliability evaluation.

Exchange in University of Monpellier/CNRS

Since October 2025, a PhD student from the University of Thessaly has been stationed at University of Montpellier/CNRS to collaborate on irradiation test campaigns and radiation effect simulations. The sudent will prepare detailed test plans and strategies to conduct Single Event Effect (SEE) and Total Ionizing Dose (TID) irradiation tests on both commercial off-the-shelf (COTS) and custom-designed chips. The training also includes design of specialized hardware setups for TID, and SEE experiments, equipping the student with comprehensive knowledge of the challenges of experimental validation under harsh radiation environments and how to mitigate them. Finally, the visit emphasizes on simulating radiation effects in scaled technologies (sub-30 nm CMOS) using in-house tools PredicSEE and ECORCE, along with data analysis techniques for extracting reliability insights from simulation results. The student is engaging into technical discussions, with the developers of these tools, to construct a detailed technical plan on the tools interface with the Cross-Layer EDA Tool Flow for reliability analysis.

Upcoming Events

2026

3rd Training School

University of Manchester

4th Research Management Workshop

University of Thessaly

2nd Scientific Workshop

University of Thessaly

3rd Research Management Workshop

University of Manchester

2nd Business Forum

University of Thessaly

2nd Webinar

University of Thessaly

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