

Press Release

2024-23-02



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Scale4Edge enters second project phase Fault-tolerant system with RISC-V cores presented at the kick-off meeting

Kaiserslautern. Future-proof specialised processors for technology sovereignty in Germany were on the agenda of the joint event of the KI-Mobil, KI-Power and Scale4Edge projects funded by the Federal Ministry of Education and Research (BMBF). In two phases, development platforms for future-proof special processors (ZuSE) are being developed with a focus on hardware for edge applications and AI processors for the automotive sector. The kick-off event in Kaiserslautern in mid-February heralded the start of the second project phase. At the beginning, the role of processors in European/German efforts to achieve semiconductor sovereignty was discussed. The 30 partners involved also showcased the results of the first phase. Here, IHP - Leibniz Institute for High Performance Microelectronics from Frankfurt (Oder) presented the TETRIS Soc demonstrator for an adaptive and fault-tolerant multi-core system. The chip developed on this basis has four open-source RISC-V cores and is optimised for use in reliability-critical environments such as those prevailing in aviation or spaceflights.



Dr Markus Ulbricht presented the IHP results of the first project phase of Scale4Edge at the kick-off meeting in Kaiserslautern.

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The approximately 30 partners in the BMBF-ZuSE projects cover a wide range of specialised fields and work on problems in the automotive and space sectors, amongst others. All these applications share innovative solutions that fulfil the high requirements for powerful electronics, processors und computing power. At the same time all solutions have to concern energy efficiency, reliability, robustness, and security. As a result, a lively panel discussion took place at the kick-off meeting, including with Mario Brandenburg, Parliamentary State Secretary of the BMBF, and the three project coordinators, as well as among the participants. During the subsequent exchange, IHP project manager Dr Markus Ulbricht answered questions about the TETRIS SoC demonstrator.

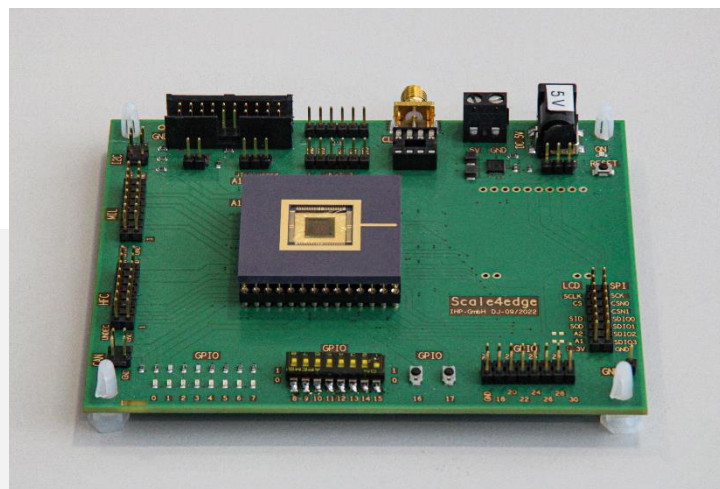


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"In the first phase of the Scale4Edge project, we focussed primarily on the design of the fault-tolerant system with RISC-V cores. The resulting test chip, which is also used in the demonstrator shown, has three sensors that check the temperature, the ageing process and the radiation exposure. On this basis, the system can adapt in real time to these parameters, which are very critical for reliability and can vary greatly in some instances. The cores can adaptively redistribute their power load among each other and thus avoid excessive heat development, which prevents damage to the system. In the event of increased radiation or strong ageing effects, they work redundantly so that a reliable result is always available via a majority decision," explains Dr Markus Ulbricht. "With our first test version, we primarily learnt how to design the system and where potential weaknesses lie. It was also used to characterise the power consumption and maximum clock frequency," he adds.



The TETRISC SoC demonstrator presented in Kaiserslautern with the developed test chip in the centre.

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In the second phase, the developed chip is further optimised and, as a final step, subjected to an irradiation test. Additionally, the IHP team not only wants to rely more heavily on open source system blocks, but also implement the design as far as possible with open source tools and make the entire fault-tolerant system available. The second phase of the Scale4Edge project will run until the end of December 2025.



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About Open Source:

Open source refers freely accessible software, hardware and methodologies. The sources can be freely viewed, used, modified and distributed. The community defines standards and formats for further development. One well-known example is the open source operating system Linux, which has been an alternative to Windows and MacOS since the 1990s and is used in high-performance, professional applications. Without licence fees and dependencies, open source also provides universities and their students, as well as SMEs, with low-threshold access to these technical solutions. IHP designs and develops open source solutions in the field of microelectronics. Via the GitHub repository, IHP provides access to an open-source PDK for the institute's SG13G2 BiCMOS technology, which can be used to create designs for production in the IHP clean room. For microelectronic systems, the open source approach is an important component for realising trustworthy electronics and ensuring the technological sovereignty of Germany and Europe. IHP and its research contribute significantly to this.

More on Scale4Edge:

<https://www.edacentrum.de/scale4edge/en>

More on the BMBF-ZuSE projects at:

<https://www.elektronikforschung.de/projekte/ki-mobil>

<https://www.elektronikforschung.de/projekte/ki-power>

<https://www.elektronikforschung.de/projekte/zuse-scale4edge>

More on the IHP open source PDK:

www.ihp-microelectronics.com/services/research-and-prototyping-service/fast-design-enablement/open-source-pdk

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About IHP:

The IHP is an institute of the Leibniz Association and conducts research and development of silicon-based systems and ultrahigh frequency circuits and technologies including new materials. It develops innovative solutions for application areas such as wireless and broadband communication, security, medical technology, industry 4.0, automotive industry, and aerospace. The IHP employs approximately 365 people. It operates a pilot line for technological developments and the preparation of high-speed circuits with 0.13/0.25 μm SiGe BiCMOS technologies, located in a 1500 m² DIN EN ISO 14644-1 3 certified clean room.

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