Press Release

IHP Partner in EU Chips Design Platform
Consortium to facilitate access to design infrastructure, training, and capital for European fabless semiconductor startups, small and medium enterprises and research organizations

Frankfurt (Oder). A consortium of 12 European partners, coordinated by imec, has been selected in the framework of the European Chips Act to develop the EU Chips Design Platform. Funded by Chips JU, the platform will facilitate access to advanced semiconductor design infrastructure, training, and capital for fabless semiconductor startups, small and medium enterprises and research organizations. By providing the necessary resources, the initiative aims to democratize and foster semiconductor innovation across Europe, specifically for chip design.

The semiconductor industry is the backbone of modern technology, powering everything from smartphones to advanced medical devices. With the EU Chips Act, Europe is dedicated to increasing its global semiconductor market share. Next to the launch of European pilot lines that aim to develop key technologies for semiconductor innovation, the EU Chips Act has proposed the EU Chips Design Platform as a vehicle to support the growth of fabless chip companies in Europe.

The EU Chips Design Platform will enable fabless companies to access the resources they need quickly and efficiently via a cloud-based virtual environment, offering chip design resources, training, and capital. Coordinated by imec, twelve key European research players in the semiconductor ecosystem have joined forces in a consortium to create this design platform.

As part of the platform coordination team, IHP is leading the effort to integrate and promote open-source EDA tools to support innovation and lower barriers to entry in the chip design market. This includes selecting and qualifying open-source EDA tools for different stages of the design flow, identifying areas for improvement, and ensuring accessibility via a central cloud infrastructure. The initiative will also provide open-source-compatible PDKs, IP libraries, and comprehensive training programs. A dedicated test environment will support experimentation and validation for new users. Collaboration with industry and international partners will further enhance the availability and quality of open design resources. "Our goal is to make open-source EDA tools and design flows intuitive, accessible, and production-ready, enabling innovators across Europe to explore ideas, prototype ASICs, and bring them to fabrication," says René Scholz, project coordinator at IHP side.

The Platform Coordination Team of the EU Chips Design Platform consists of imec (Belgium), the French Alternative Energies and Atomic Energy Commission (CEA, France), Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e. V. (Germany), Leibniz Institute for High Performance Microelectronics (IHP, Germany), Silicon Austria Labs (Austria), Fondazione Chips-IT (Italy), Spanish National Research Council (CSIC, Spain), International Iberian Nanotechnology Laboratory (Portugal), Eindhoven University of Technology (The Netherlands), Tampere University (Finland), CVUT (Czech Republic) and AGH University of Krakow (Poland).

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The grant agreement with the Chips JU, through the European Union's Digital Europe program, is ongoing and will be signed later this year. The project will run from 2025 until the end of 2028.

Follow the European Chips Design Platform LinkedIn page for more updates.

Representatives of the twelve consortium members gathered at the International Iberian Nanotechnology Laboratory in Braga, Portugal.

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About IHP:
The IHP is an institute of the Leibniz Association and conducts research and development of silicon-based systems and ultrahigh frequency circuits and technologies including new materials. It develops innovative solutions for application areas such as wireless and broadband communication, security, medical technology, industry 4.0, automotive industry, and aerospace. The IHP employs approximately 365 people. It operates a pilot line for technological developments and the preparation of high-speed circuits with 0.13/0.25 µm SiGe BiCMOS technologies, located in a 1500 m² DIN EN ISO 14644-1 3 certified clean room.

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