

Successful simple power analysis of GALS ECC design

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Side channel analysis attacks are significant threat for implementing cryptographic algorithms. A lot of countermeasures based on the randomization of the secret (private) key [1], inputs [1], steps of algorithms [2] or influence of the circuit [3] are published. In [4] the implementation of ECC (Elliptic Curve Cryptography) design as a GALS (Global Asynchronous Locally Synchronous) design was introduced as a possible countermeasure against side channel analysis (SCA) attacks.

We performed a simple power analysis (SPA) attack against the original synchronous IHP ECC design and against its GALS-ified version. In this work we analysed simulated power traces of both ECC designs. To ensure a fair comparison exactly the same manufacturer library of elements, the same inputs, private key and simulation tools were used for obtaining the power traces of both hardware implementations. The private key can be extracted successfully for both designs. This shows clearly that a straight forward GALS-ification of a synchronous ECC design that is vulnerable to SPA is also vulnerable to SPA. Also we explain here why the GALS design is even more vulnerable to other SCA attacks for example to differential power analysis than a synchronous ECC design.

Acknowledgement

The authors would like to thank the Dr. Milos Krstic from System department of IHP for providing the GALS-ified version of IHP ECC design.

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