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Impact of the Incremental Programming Algorithm on the Filament Conduction in HfO₂-Based RRAM Arrays

EDUARDO PÉREZ¹, ALESSANDRO GROSSI², CRISTIAN ZABELLI², PIERO OLIVO², AND CHRISTIAN WENGER¹

¹ IHP GmbH/Leibniz-Institut für innovative Mikroelektronik, 15236 Frankfurt, Germany

² Dip. di Ingegneria, Università degli Studi di Ferrara, 44122 Ferrara, Italy

CORRESPONDING AUTHOR: E. PÉREZ (e-mail: perez@ihp-microelectronics.com)

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ABSTRACT In this paper, the set operation of HfO₂ based 1T-1R arrays is studied by applying incremental step pulse with verify algorithm. To evaluate the impact of the voltage step increment on the conduction mechanism of filaments, the voltage increments between consecutive pulses are varied between 0.05 and 0.4 V. The extracted leakage values after the set operation were discussed in the framework of the quantum point contact model. In the so called low resistive state, the conductive filaments demonstrate a defined signature of conductance quantization.

INDEX TERMS RRAM, HfO₂, QPC model, programming algorithm.

I. INTRODUCTION

Resistive Random Access Memories (RRAM) based on HfO₂ is one of the most promising technology candidates for replacing Flash memories [1], [2]. This technology has shown fast low-power switching operations, high-integration density [3], [4], and compatibility with CMOS processes [5]. However, an intensive research activity has still to be performed on this innovative technology in order to increase RRAM reliability and performance. After the concept validation on single cells [6], [7], the characterization of array structures is mandatory to bring such technology to a maturity level [8]–[10].

RRAM behavior is based on the electrical modification of the conductance of a Metal-Insulator-Metal (MIM) stack: the Set operation moves the cell into a Low Resistive State (LRS), whereas Reset operation brings the cell back to a High Resistive State (HRS) [8], [11]. In order to control the formation and rupture of the conductive filament (CF), the Incremental Step Pulse with Verify Algorithm (ISPVA) [12]–[14] is applied instead of a simple DC voltage sweep [15]. The drawback of ISPVA guided Set and Reset operations is the increased power consumption per writing cycle. One way to minimize the consumption is to enlarge the incremental voltage steps. For this purpose, a complete study of the voltage increment variation

between consecutive pulses on array RRAM devices was performed. The extracted experimental results were analyzed in the framework of the quantum point contact (QPC) model [16].

II. SAMPLES CHARACTERISTICS

The measurements were performed over 4 kbits memory devices organized in 64 pages (rows) each consisting of 64 cells (bits), as Fig. 1 shows including also the peripheral circuitry. Each cell is a 1T-1R RRAM single device constituted by a select NMOS transistor manufactured in 0.25 μm BiCMOS technology: W = 1.14 μm and L = 0.24 μm. Such a transistor also sets the current compliance, whose drain is in series to a variable resistor connected to the bitline (BL). The variable resistor is a Metal-Insulator-Metal (MIM) device integrated on the metal line 2 of the CMOS process. The schematic and cross-sectional SEM image of the integrated RRAM cell including the metal lines and the W based Via-connections are shown in Fig. 2. The MIM resistor is a TiN/HfO₂/Ti/TiN stack of 150 nm TiN layers deposited by magnetron sputtering, a 7 nm Ti layer (under TiN top electrode), and a 8 nm HfO₂ layer grown by Chemical Vapor Deposition (CVD), which results in amorphous films (determined by

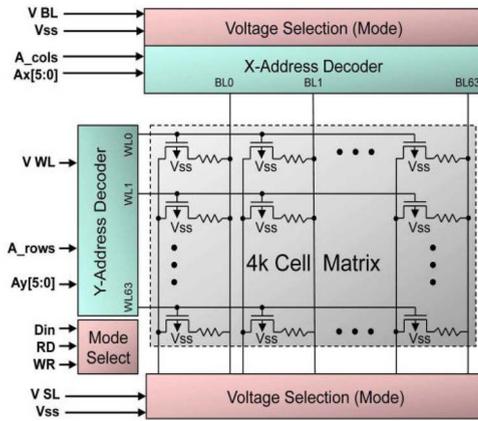


FIGURE 1. Simplified block diagram of the 4 kbits memory device.

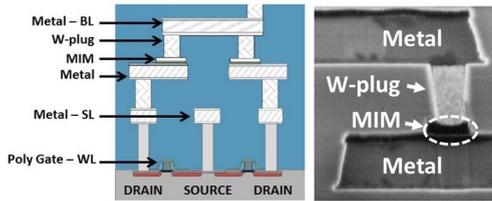


FIGURE 2. Schematic and cross-sectional SEM image of the integrated RRAM cell.

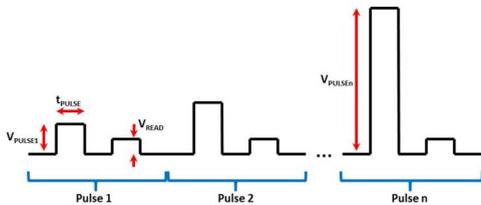


FIGURE 3. Schematic illustration of the Incremental Step Pulse with Verify Algorithm (ISPVA).

X-Ray Diffraction measurements). The resistor area is equal to $0.4 \mu\text{m}^2$.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The electrical characteristics were obtained by means of a set-up based on the RIFLE SE test system working together with the Cascade PA200 semi-automatic probe system. In order to ensure a reliable accuracy for statistical calculations 128 1T-1R cells (two 64-bits pages) were characterized at each voltage step.

The ISPVA technique consists of a sequence of increasing voltage pulses (Fig. 3) on the BL during Set operation, whereas this sequence is applied on the source line (SL) during Reset operation: $V_{pulse} = 0.2 - 3.5 \text{ V}$, $t_{pulse} = 10 \mu\text{s}$, $t_{fall/rise} = 1 \mu\text{s}$. In order to analyze its effect over the RRAM cells behavior, several measurements were done using different voltage step values between consecutive pulses (V_{step}): 0.05, 0.1, 0.2 and 0.4 V. The applied transistor gate voltage values through the wordline (WL) were 2.7 V for Reset and 1.4 V for Set. After every pulse a Read-verify

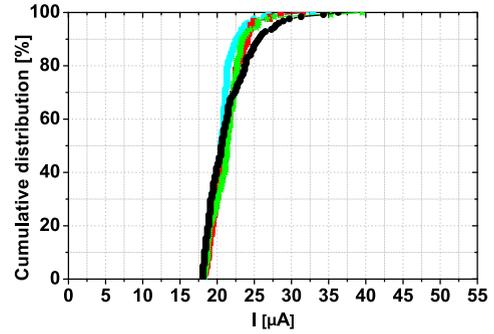


FIGURE 4. Cumulative distribution of the read currents after Forming operation in the 4 subsections of the 4 kbit memory array.

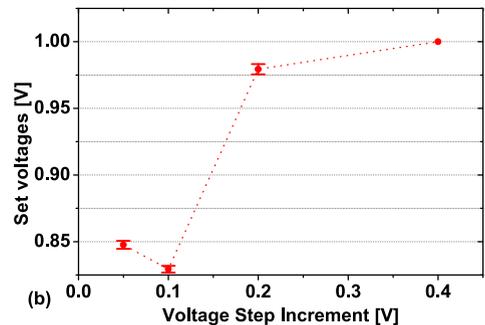
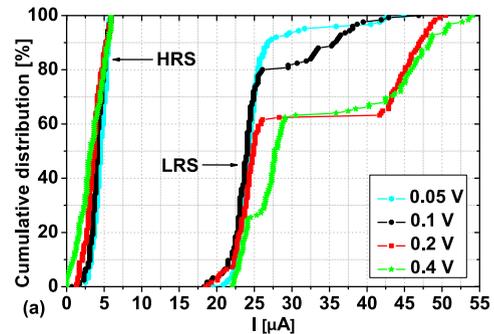


FIGURE 5. Cumulative distribution of read currents (a) and average and dispersion of Set voltages (b) as function of voltage step increment.

operation is performed with $V_{WL} = 1.4 \text{ V}$, $V_{read} = 0.2 \text{ V}$ (applied over the Drain) for $10 \mu\text{s}$. When the Read current reaches the target value of $18 \mu\text{A}$ the Set operation is stopped, whereas the Reset operation is stopped when the target value of $6 \mu\text{A}$ is achieved.

To activate the resistive switching behavior, the RRAM cells require a preliminary Forming operation [4]–[7]. This initial operation plays a fundamental role in determining the subsequent devices performance [17]. Therefore, the ISPVA procedure is also used for the Forming operation with the same parameters for each subsection (128 cells) of the 4 kbit array: $V_{pulse} = 2 - 5 \text{ V}$, $t_{pulse} = 10 \mu\text{s}$, $t_{fall/rise} = 1 \mu\text{s}$, $V_{step} = 0.01 \text{ V}$ and $V_{WL} = 1.4 \text{ V}$. The cumulative distributions of the currents after forming are within the variability limit of the RRAM process technology as shown in Fig. 4. Therefore, the starting point for the following Reset/Set operations is similar for every subsection.

First of all, the impact of the ISPVA procedure on the filamentary conduction mechanism after the first Reset and Set operation was evaluated. As shown in Fig. 5(a), the first Reset operation is not affected by the variation of voltage steps. The currents in the High Resistive State (HRS) are quite similar within the limit of process variability. In contrast to the Reset operation, the currents in the Low Resistive State (LRS) are strongly affected by the increase of voltage increment. At small step increments, 80-90 % of cells are set to the same LRS current values as after the Forming procedure. The remaining 10-20 % cells tend to be set to higher current values. This trend is strongly pronounced at larger incremental voltage steps. Now, 40 % of the cells show a second contribution of LRS currents with much higher values. As illustrated in Fig. 5(b), the Set operations with small voltage increments happen at voltages around 0.85 V. Caused by the increase of the voltage increment to 0.2 and 0.4 V the cells are forced to Set around 1 V.

In order to illustrate the distribution of LRS currents in a better way, the Set currents are plotted separately as function voltage step increment in Fig. 6. As shown in Fig. 6(b) and (c), a second peak occurs at about 48 μA . The first peak at about 24 μA is strongly reduced. It is obvious, that a kind of quantization of the conduction mechanism occurs at larger voltage step increments.

The observation of conductance quantization in oxide-based resistive memory cells was reported by Zhu *et al.* [18]. The conductance quantization behavior was attributed to the creation and annihilation of atomic scaled CF in the oxide layer. Later on Lian *et al.* [19] linked the conduction quantization with the quantum point contact model. Regarding the HfO₂-based RRAM cells, a CF is constructed by the Forming operation and its behavior can be explained by the QPC model. Focusing on the LRS, the current raises linear with applied voltage and can be expressed as [20]:

$$I = NG_0V / (1 + NG_0R) \quad (1)$$

where $G_0 = 2e^2/h$ is the quantum conductance unit, N is the number of CF and R is a series resistance external to the constriction of the filament.

In order to evaluate the number of CF, additional DC measurements were performed, by using the same voltage values as in the ISPVA mode. Fig. 7 illustrates the experimental LRS I-V characteristics. The obtained I-V curve can be explained by the QPC model: the continuous line illustrates the fitting curve for LRS by using (1). The series resistance R is mainly generated by the select transistor and is determined by a separate simulation. The theoretical curve agrees with the experimental data, indicating that the QPC model is able to explain the conduction mechanism. According to the model, one CF is formed ($N = 1.01$) by applying the adopted ISPVA voltage values.

By using the quantum conductance value of 12.9 k Ω at the readout voltage of 0.2 V, the calculated current per filament is about 15 μA , without taking into account external resistances. Although at small incremental steps the first peak

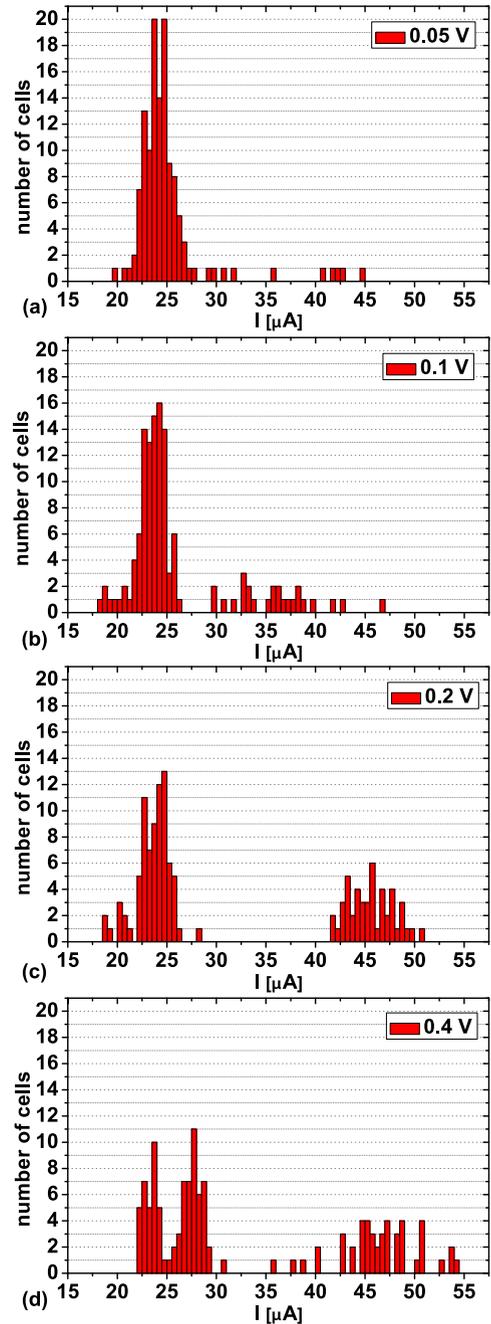


FIGURE 6. Distribution of currents after Set operation as function of voltage step increment: 0.05 V (a), 0.1 V (b), 0.2 V (c) and 0.4 V (d).

appears at about 24 μA , we can assume that just one filament is formed by the Set process at 0.85 V (Fig. 8(a)). According to Grossi *et al.* [21] G_0 value correspond to the bottom limit of the filament conduction: narrower filament implies the creation of a constriction and higher conduction values are caused by enlarged filaments. Since at large incremental steps the second peak appears at about 48 μA , we can conclude that the Set operation at 1.0 V results in the formation of two filaments, as illustrated in Fig. 8(b). It has to be mentioned, that the formation of two filaments is

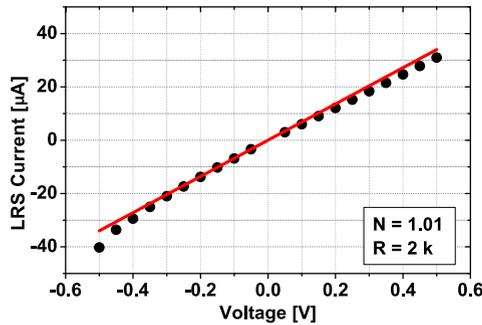


FIGURE 7. Experimental (black solid circles) and theoretical I-V characteristics for the LRS in DC mode. The QPC model was used for the theoretical curve (red solid line).

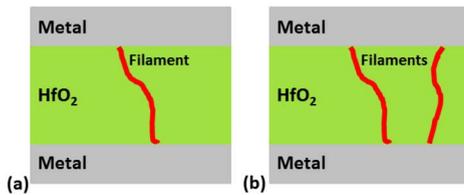


FIGURE 8. Schematic illustration of the conduction quantization in LRS: (a) one CF with a mean current of about 24 μA and (b) two CF with mean currents of about 48 μA .

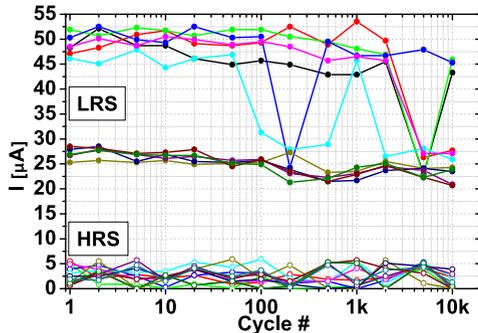


FIGURE 9. Stability of the two LRS states and the HRS during endurance cycling procedure over 11 of the considered devices.

enabled by the saturation current of the select transistor of about 100 μA at the used gate voltage of 1.4 V during the Set process.

Finally, the stability of both LRS states and the HRS are examined by endurance cycling of 10^4 times using ISPVA. In Fig. 9 are shown the results for 11 of the considered devices. The LRS state consisting just on one CF is stable, while the cells consisting on two CFs demonstrate partially unstable switching behavior, because one or alternative two filaments are involved in the switching process. The conduction through either one or two filaments after Set operations depends on random phenomena as [22] claims. In contradiction to the widely acknowledged picture of filament growth from the active electrode toward the inert electrode, an additional filament growth mode with opposite direction is reported by Dirkmann *et al.* [22]. HRS current values

remains below the threshold value of 6 μA emphasizing the presence of a constriction in the conduction path in the HRS state, as predicted by the QPC model [21].

IV. CONCLUSION

The conduction properties of resistive switching filaments have been studied in HfO₂ based memory arrays. By applying the Incremental Step Pulse with Verify Algorithm with varied incremental voltage steps, a quantization of the LRS state is observed in the Set operation regime. The quantization of two LRS conductance states is explained by the QPC model. The endurance study of both conductance states reveals that the conduction path consisting of just one filament is stable, while the one consisting of two filaments is partially unstable.

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EDUARDO PÉREZ received the M.Sc. and Ph.D. degrees in information and communications technologies from the University of Valladolid, Valladolid, Spain, in 2010 and 2014, respectively. He has been with the Innovations for High Performance Microelectronics since 2015, where he researches in the field of electrical characterization of resistive switching devices.



ALESSANDRO GROSSI received the M.Sc. degree in electronic and telecommunications engineering from the Università degli Studi di Ferrara, Ferrara, Italy, in 2013, where he is currently pursuing the Ph.D. degree in engineering science with the Department of Engineering.



CRISTIAN ZABELLI received the M.Sc. and Ph.D. (Hons.) degrees in electronic engineering from the University of Ferrara, Ferrara, Italy, in 2008 and 2012, respectively, where he has been an Assistant Professor since 2015. His current research interests include the electrical characterization, physics, and reliability modeling of different nonvolatile memories such as NAND/NOR flash, phase change memories, nano-MEMS memories, resistive RAM, and magnetic RAM. He is also interested in the evaluation of the solid state drives reliability/performance tradeoffs exposed by the integrated memory technology.



PIERO OLIVO received the Ph.D. degree in electronic engineering from the University of Bologna, Bologna, Italy, in 1987. He has been a Full Professor of Electronics with the University of Ferrara, Ferrara, Italy, since 1994. He has co-authored the first paper describing and analyzing stress induced leakage current in thin oxides, presented at IRPS'87. His research interests include the physics, the reliability and the experimental characterization of innovative non-volatile memory cells and architectures.



CHRISTIAN WENGER received the Diploma degree in physics from the University of Konstanz in 1995, and the Ph.D. and Post-Doctoral degrees from the Technical University of Dresden, in 2000 and 2009, respectively. Since 2002, he has been with the Innovations for High Performance Microelectronics, where he works in the field of functional devices for medical and space applications. He has authored and co-authored over 150 papers and holds 6 patents.