

Placement of Gates in ECC Designs

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In Heyszl (2013) a localized Electromagnetic Analysis (EMA) attack against an FPGA implementation of an Elliptic Curve (EC) point multiplication was introduced. The attacked design is an implementation of the Montgomery kP algorithm using projective López-Dahab coordinates for the NIST EC $B-163$. The Montgomery kP algorithm is a bitwise processing of the scalar k , whereby the activity of registers depends on the processed bit value of the scalar k . Thus, the scalar k can be revealed due to the physical placement of the registers in a hardware implementation. To prevent this kind of attacks a randomized placement of flip flops of all registers was proposed in Heyszl (2013). This randomization leads to an equal distribution of flip flops in the chip area and can increase the vulnerability of designs against other side channel analysis attacks. Isolated placed flip flops can be attacked more precisely using optical fault injection attacks. Furthermore interconnects of isolated placed flip flops can be significant longer than interconnects of flip flops placed close to each other. These interconnects can be a strong leakage source that increases the success of EMA attacks, for example horizontal bus and address bit DEMA attacks.

Thus, the designer needs a methodology for an intelligent placement of gates. This work describes our first experiments for the development of an intelligent placement of logic gates and register flip flops in the layout.

References

- JOHANN HEYSZL (2013). *Impact of Localized Electromagnetic Field Measurements on Implementations of Asymmetric Cryptography*. Ph.D. thesis, Technische Universität München.