Wideband 240-GHz Transmitter and Receiver in BiCMOS Technology With 25-Gbit/s Data Rate

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Abstract—In this paper, a fully integrated wideband 240-GHz transceiver front-end, supporting BPSK modulation scheme, with on-chip antenna is demonstrated in SiGe:C BiCMOS technology with $f_t/f_{\text{max}} = 300/500 \text{ GHz}$ and local backside etching option. Within the transmitter, the upconversion is provided by fundamental mixing using a modified Gilbert cell mixer driven by a multiplier-by-eight local oscillator (LO) chain. The transmitter achieves a 3-dB RF bandwidth of 35 GHz with a saturated output power of $-0.8 \text{ dBm}$. The down converter is equipped with a mixer first architecture. The mixer is designed utilizing a transimpedance amplifier as load for enhanced noise and bandwidth performance. For dc-coupled receiver, two dc offset cancellation loops are implemented within the receiver chain. It achieves a 3-dB RF bandwidth of 55 GHz, minimum single-sideband noise figure (SSB NF) of 13.4 dB, and a gain of 32 dB with 25-dB gain control. A wideband on-chip double-folded dipole antenna and an on-board optical lens are utilized to demonstrate a wireless link achieving 20- and 25-Gb/s data rates at bit error rates (BERs) of $6 \times 10^{-6}$ and $2.2 \times 10^{-4}$, respectively, across a distance of 15 cm. The transmitter and receiver consume 375 and 575 mW, respectively, which correspond to power efficiencies of 15 pJ/bit for the transmitter and 23 pJ/bit for the receiver. They occupy a silicon area of 4.3 and 4.5 mm$^2$, respectively.

Index Terms—Broadband circuits, broadband communication, ultra wideband communication.

I. INTRODUCTION

The wide and available bandwidths above 200 GHz open a lot of opportunities for very high data rate communication solutions. Such frequency range might be optimal for applications that require very high data rates for short ranges such as chip to chip, board to board or rack communication in data centers. At these frequencies, the wavelength is in the millimeter range. Hence, on-chip antenna is one of the efficient solutions to deliver the power out of the chip, alleviating the need for expensive off-chip alternatives and packaging techniques. With the continuous technological options such as local back side etching (LBE) and system techniques to maximize RF bandwidth, system efficiency. While implementing systems at sub-terahertz frequencies, different challenges rise on the system and circuit levels. The degraded maximum available gain (MAG) at such frequencies results in low-power efficiency transmitters and frequency generation circuits. Top of that, the relatively high minimum noise figure (NF) (NF$_{\text{min}}$) allows only for receivers with limited sensitivity. These factors, together with the high path loss, result in a very challenging link budget analysis. In order to overcome these challenges, circuits and system techniques need to be implemented to enable efficient solutions.

To achieve high system dynamic range, receiver NF is to be minimized while maximizing the transmitter output power and maximizing the receiver gain to cover such dynamic range. This can be reached by cascading more stages at the RF side [low noise amplifiers (LNA)+Mixer], which limits the achievable bandwidth, or by implementing high gain baseband chains, which is challenging in direct conversion receivers because of the dc coupling of the different stages. In some embodiments, this has been solved by decoupling the stages with bulky series capacitors. Although being a simple solution, it adds a tradeoff between the area consumption and the achievable low-cutoff frequency of the receiver.

Several transmitter and receiver architectures and building blocks at such high frequencies have been presented in the literature and some presented data transmission experiments, implementing either non-coherent detection for ON–OFF keying (OOK) modulation scheme [1], [2] or coherent detection for phase-shift keying (PSK) and quadrature-amplitude modulation (QAM) schemes [3]–[8].

In this paper, a fully integrated receiver and transmitter chipset with on-chip antennas are presented, implementing circuits and system techniques to maximize RF bandwidth, system dynamic range, and power efficiency. Fig. 1 shows the block diagrams of the direct conversion transmitter and receiver chips, supporting BPSK modulation scheme. DC-offset cancellation loops (dc OCLs) are used within the receiver to guarantee consistent performance across process variations and achieve low-cutoff frequency. The complete system is characterized by wireless data transmission. The paper is organized...
as follows: the system aspects considered for choosing the local oscillator (LO) frequency are presented in Section II. The transmitter and receiver design details and measurements are discussed in Section III and Section IV, respectively. Section V provides a summary of the antenna design. The measurement results of the wireless link demonstrator are then presented in Section VI and Section VII concludes the paper.

II. LO FREQUENCY GENERATION

A frequency multiplying chain is utilized to generate the on-chip sub-terahertz carrier frequency LO_N, centered at 240 GHz. Although low-frequency signals are easier to generate and route on board with low losses. The choice of the input frequency LO_in and the multiplication factor N is crucial in communication systems, as it defines the frequency spacing between the desired signal and any other spurious signal. To visualize the effect of the LO spurs and the spacing between them on the system specifications, Fig. 2 shows how the spurious tones of the LO signal, LO_N-1 and LO_N+1, attenuated by a ratio of LO_rej from the fundamental signal LO_N, create undesired spurious versions of the data. Hence, LO_in should be at least equal to twice the targeted baseband bandwidth to guarantee minimum interference on top of the desired signal from parasitic up and down conversions. This will guarantee that this parasitic harmonics will not degrade the signal quality. It is worth mentioning that lower LO_in is still possibly utilized, but in cost of more stringent requirements on the spurious harmonics rejection. For the system presented here, a baseband signal bandwidth of 15 GHz is targeted, so an LO frequency of 30 GHz is multiplied by eight through a multiplication chain.

In the transmitter chip, as shown in Fig. 1(a), a single-ended 30-GHz input LO signal is converted to a differential one through an edge-coupled spiral Marchand balun. The balun drives a Gilbert cell-based quadrupler, optimized to maximize the fourth harmonic at its output. The resulting 120-GHz signal is then amplified by a three-stage cascode amplifier, which acts also as a filtering stage to cancel out the unwanted harmonics. The signal is then multiplied by two through a push–push frequency doubler. As the output of such frequency doubler is single ended, a 240-GHz Marchand balun is utilized to feed the mixer’s LO port differentially [9], [10]. In the receiver chip, the doubler was implemented differentially using a Gilbert cell-based frequency doubler, as shown in Fig. 1(b), followed by a broadband amplifier to drive the mixer. The LO multiplication chain is presented in detail in [11].

III. WIDEBAND 240-GHZ TRANSMITTER

The transmitter chip is shown in Fig. 1(a). The baseband signal is amplified by a resistively loaded common emitter amplifier. The differential input is resistively matched through a 100-Ω resistor. The baseband signal is then upconverted through a fundamental mixer. The broadband amplifier presented in [11] is used as power amplifier following the mixer to increase the output power radiated through a double-folded dipole on-chip antenna.

In conventional Gilbert cell mixers, as shown in Fig. 3(a), the LO signal drives the switching quad transistors (Q1–Q4), while the baseband signal is fed into the transconductance (g_m) stage (Q5–Q8). In this paper, as shown in Fig. 3(b), this configuration was modified in order to maximize the mixer conversion gain and bandwidth [12]. Because of the limited
power at 240 GHz, the LO signal was fed into the $g_{m}$ stage instead of the switching quad. As now the LO driver is loaded by half the number of transistors, the input impedance in this case is typically doubled compared to the conventional connection. This allows for lower loss matching networks and higher voltage swing at the LO port and so better switching. To validate this analysis, both topologies have been simulated in the same matching conditions. Transistors are equally sized in order to keep all of them in the optimum $f_T$ biasing conditions. Simulation results showed the input impedance at the LO port for topology (a) is $8.6-j*12$ while that for topology (b) is $18-j*15$. As shown in Fig. 4(a), the conversion gain of the modified topology [topology (b)] is higher than the conventional topology [topology (a)] till a certain level of LO power after which the LO power is high enough to perform better switching. Moreover, because of the higher input impedance in topology (b), the impedance matching ratio is lower, which leads to less lossy matching networks. Another advantage of topology (b) is the higher RF output impedance, being nearer to the 100-Ω differential impedance, which promises for wider RF bandwidth.

The conversion gain and RF return loss of both mixer topologies are simulated for LO power of $-5$ dBm; this LO power level was chosen to account for future in-phase and quadrature-phase mixer implementation, where the LO signal will be equally divided and experiences the losses of the

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Fig. 7. Transmitter conversion gain and LO-to-RF leakage across LO frequency (RF = 241 GHz).

Fig. 8. Transmitter conversion gain and output power across input power.

the baseband frequency is swept. With respect to the SHM based measurement, the conversion gain in linear operation, plotted in Fig. 6, shows better agreement with its simulated values. Then, the baseband input power was swept. As shown in Fig. 8, a −2.3-dBm saturated output power along with an output 1-dB compression point (OP1dB) of −3 dBm and a conversion gain of 9 dB were measured. Considering the output pad losses of 1.5 dB, the saturated output power in the transmitter version with on-chip antenna is expected to be −0.8 dBm. The transmitter consumes a total power of 375 mW.

IV. WIDEBAND 240-GHZ RECEIVER

As the operation frequency increases approaching the transistor $f_T$ frequency, the transistor $NF_{min}$ increases significantly, while the MAG decreases. In Fig. 9, $NF_{min}$, MAG, and stability factor of a single-stage cascode amplifier, widely adopted configuration for amplifier designs at such frequency ranges [13], with transistor-emitter area of $4 \times 0.12 \times 0.9 \mu m^2$ are plotted across the transistor collector bias current. In the schematic level, a MAG of 15 dB and a $NF_{min}$ of 10 dB were simulated in stable conditions. Obviously, the MAG and the $NF_{min}$ performances will be even worse after electromagnetic simulations of amplifier core and matching networks.

To elaborate more on the frequency dependence of the NF, the expression of the HBT’s shot noise is reported in (1) and (2) [14], where $q$ is the charge, $B$ the bandwidth of interest, $V_T$ thermal voltage, $I_C$ the transistor bias current, $Z_S$ the source impedance, and $\beta(\omega)$ the transistor frequency-dependent current gain. The term $N_{CE}$ considers the shot noise added by the collector-emitter junction while the term $N_{BE}$ corresponds to the one injected by the base-emitter junction. The base contact resistance is neglected here

$$V_{in}^2 = 2Bq(N_{BE} + N_{CE})$$

$$N_{BE} = \frac{V_T^2}{I_C}, \quad N_{CE} = \frac{Z_S^2 I_C}{\beta(\omega)}.$$ (2)

It is clear that as the frequency increases, the current gain $\beta(\omega)$ decreases and so the input referred noise increases. The relatively high NF achievable by LNA at such frequency ranges makes its benefit for the link budget analysis marginal. This motivates the idea of omitting the LNA and go for a mixer-first architecture, if the mixer design can be optimized to achieve NF comparable to the LNA NF. This will also promise for better linearity and larger bandwidth because of reducing the number of cascaded stages in the chain. In this paper, a mixer-first architecture is proposed as shown in Fig. 1(b).

A. Downconversion Mixer With first dc Offset Cancellation Loop

In a conventional Gilbert cell mixer design at such sub-millimeter-wave frequencies, the $g_m$ stage is the first noise contributor followed by the switching quad transistors. At the same time, the $g_m$ stage acts as an amplification stage prior to the switching quad stage, reducing its noise contribution. Nevertheless, due to the reduced achievable MAG, at this high frequency, this benefit is limited. Hence, it was found, as shown in Fig. 10 and further explained in [10], that by omitting the $g_m$ stage lower mixer NF can be achieved. While the RF signal is fed directly to the emitters of the switching quad transistors ($Q_1$–$Q_4$). Another advantage of feeding the RF
signal into the emitters rather than the base is the lower input impedance, being nearer to the 100 Ω differential impedance, which leads to lower loss matching structures. As the size of (Q1–Q4) decreases, their capacitive loading decreases, but their base resistance (rbb) increases, boosting the Johnson noise contribution of the switching quad transistors. Hence, the quad sizing is driven by a compromise between capacitive loading, driving capability, and noise contribution.

Although omitting the gm stage enhances the NF, it limits the conversion gain. Increasing the conversion gain through increasing the load resistance in conventional Gilbert cell mixer compromises the achievable bandwidth. Hence, to further enhance the mixer conversion gain without sacrificing the bandwidth, a transimpedance amplifier (TIA) is implemented at the mixer load to translate the switching quad output current signal into a voltage signal. Normally, the drawback of such implementation is the need for high-voltage headroom and so high supply voltage. In this paper, as shown in Fig. 10, a dc bias servo loop is proposed where a pair of pMOS devices (Pn–Pp) is used as dc current source to bias the switching quad. The pMOS devices are controlled by two operational amplifiers (OPAMPs) sensing the switching quad collectors’ dc voltage and comparing it to an on-chip reference voltage (Vref). This setup ensures that only the ac signal flows across the resistor RF and not the dc current, not requiring any higher supply voltage. In such case, the sizing of the RF and the TIA parameters are irrelevant to the mixer bias, adding a lot of flexibility to the design and avoiding sub-optimal realizations. The bias servo loop also acts as a dc OCL compensating for any dc offsets arising from the LO leakage of mixer’s devices mismatches. In order to further enhance the achieved bandwidth, a slight inductive peaking is implemented between the mixer and the TIA (TLind1) to compensate for the switching quad parasitic capacitance and the TIA input capacitance, taking care of the group delay variations across the targeted bandwidth [15].

**B. Cascaded VGAs With Second DC-Offset Cancellation Loop**

To achieve sufficient output swing, for bit error rate (BER) measurements, cascaded variable gain amplifiers (VGA) are used after the mixer. The current steering VGA topology, shown in Fig. 11, was implemented with capacitive peaking at the emitter. An output buffer is utilized to drive the 100-Ω differential output. The second dc OCL is implemented in a series–shunt feedback topology where the differential output dc voltages (Voutp, Voutn) are sensed and compared within a differential-to-single-ended OPAMP. The output of the OPAMP is then compared to an internally generated reference voltage (Vref) through a current steering nMOS differential pair (N1, N2) delivering the current difference to the resistive load of the first VGA as shown in Fig. 11. Such a dc OCL is crucial in dc-coupled cascaded amplification stages since it avoids any gain drop across process variations due to the saturation of the different stages.

**C. Receiver Performance**

In order to test the performance of the baseband chain including first and second dc OCLs, a test cell, whose die photo is shown in Fig. 12, was manufactured. On-wafer differential S-parameter measurements show a transimpedance gain of 68 dB Ω in maximum gain setting across a 3-dB bandwidth of 46 GHz with maximum group delay variation of ±5 psec as shown in Fig. 13(a). The baseband chain achieves a low-cutoff frequency 3-dB bandwidth of 8 MHz which can be reduced further by simply adding off-chip capacitors, this does not affect the RF performance unlike the usage of dc
blocking capacitors within the signal path. The operation of the two dc OCLs was tested by inserting a differential dc current at the input ($I_p, I_n$), to mimic the mismatches generated from the LO leakage or due to devices mismatches, while monitoring the output dc voltage ($V_{outp}, V_{outn}$). As shown in Fig. 13(b), the two dc OCLs operate across an input dc current of $\pm 5.5$ mA with only 6-mV output dc offset voltage in maximum gain. In order to characterize the full receiver including the mixer and the LO multiplication chain, the test structure shown in Fig. 14 was manufactured and measured on wafer. The RF frequency was swept at a constant LO frequency of 240 GHz as shown in Fig. 15. A maximum conversion gain of 32 dB was measured with gain tuning range of 25 dB across a RF 3-dB bandwidth of 55 GHz in linear operation. An input return loss better than $-7$ dB was measured across the 3-dB bandwidth (without the input pad, the input return loss was simulated to be better than $-10$ dB). Noise measurements have been conducted using the gain method. The single-sideband (SSB) NF was calculated in maximum gain to be 16.5 dB averaged across the band with a minimum value of 13.4 dB at 230 GHz. The enhanced RF matching, the higher LO power and the higher TIA gain are the reasons why the presented receiver shows lower SSB NF compared to the one presented in [10]. In addition, better results are expected without the input RF pad. As discussed earlier, the LO multiplication chain generates not only the desired LO signal of $8 \times 30$ GHz = 240 GHz but also undesired seventh and ninth harmonics at 210 and 270 GHz, respectively. In order to quantify the distortion caused by these spurious emissions, the resulting down-converted signals at $210 - f_{RF}$ and $270$-GHz-$f_{RF}$ were measured. The rejection for two LO frequencies of 235 and 240 GHz are plotted in Fig. 16, showing a worst case rejection of 30 dBc at RF frequency of 230 GHz.

To characterize the receiver linearity, the RF input power was swept at a constant LO frequency of 240 GHz and RF frequency of 250 GHz (IF = 10 GHz) for three different gain states. The input power sweep, shown in Fig. 17, shows an input 1-dB compression point (IP1dB) of $-28.5$ dBm for a gain of 30.5 dB in maximum gain setting at 240 GHz.
The close proximity between the measured data and the simulated ones results from the full electromagnetic simulation of the high-frequency components and passives together with the RC extraction of the broadband circuit ones.

V. BROADBAND ON-CHIP ANTENNA AND LENS

The IHP LBE technology allows for high antenna efficiency by removing the high-loss silicon substrate beneath the antenna radiator. The double-folded dipole antenna presented here and shown in Fig. 18 is an optimized version of the antenna presented in [16] for larger RF bandwidth. The radiator is manufactured on the uppermost metal layer (TM2) with the board below the chip serving as reflector in the final implementation. The silicon substrate height is thinned to 200 μm. The simulated antenna gain is 7.5 dBi with ±25° beamwidth as shown in Fig. 19 and a 1-dB bandwidth of 33 GHz from 225 to 258 GHz as shown in Fig. 20(a), with a maximum simulated efficiency of 70%. These simulation results do not include the input pad structure. The antenna test structure shown in Fig. 18 was measured on wafer, using the metal chuck of the probe station as reflector. Then, the antenna test structure was diced and glued on the ground plane of a printed circuit board (PCB) in order to compare the performance. The measured results of eight antennas measured on wafer and two antennas measured on PCB together with
the simulated input return loss including the pad can be observed in Fig. 20(b). The difference between the simulated and measured data might originates from the tolerance of the LBE process or the thinning process, for the glued version the height of the glue also play a role, over and above at such frequencies the probe tip over travel shows variations in the return losses. To further improve the radiated power, a 40 mm × 40 mm lens made of high-density polyethylene with a relative permittivity of 2.32 is utilized. The lens has a plano-convex type with two refracting surfaces and a focal length of 25 mm. The gain of the lens combined with the effective gain of the on-chip antenna depends on the link distance as presented in [17].

VI. WIRELESS DATA LINK EXPERIMENTAL RESULTS

Die photos of the transmitter and receiver chips with on-chip antennas are shown in Fig. 21. The chips were thinned to 200 μm based on the optimization of the antenna design with the LBE option. The receiver and transmitter chips have been bonded as a die-on-board with the optical lens fixed at a distance of 2 cm from the PCB surface, as shown in Fig. 22. The radiation occurs from the top side of the chip while the board metallization behaves as reflector. A Rogers3003 material is used on top of an FR4 layer for the board production to route with low losses the LO signal while maintaining robust board handling. The dc connections have been routed at the backside of the PCB to avoid unwanted coupling between the transmitter and the receiver. The measurement setup depicted in Fig. 23 shows that the same frequency source, with a specified phase noise of $-145$ dBc/Hz at 10-MHz offset which dominates the noise performance of the 240 GHz frequency source, have been used to drive the LO of both boards to guarantee frequency and phase synchronization as
TABLE I

PERFORMANCE COMPARISON OF WIRELESS LINKS AT SUB-MILLIMETER-WAVE FREQUENCIES

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[1]</th>
<th>[4]</th>
<th>[18]</th>
<th>[2]</th>
<th>[3][5]</th>
<th>[7]</th>
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<tr>
<td>Technology</td>
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<td>130 nm SiGe</td>
<td>130 nm SiGe</td>
<td>40 nm CMOS</td>
<td>65 nm CMOS</td>
<td>130 nm SiGe</td>
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<tr>
<td>fT /fMAX (GHz)</td>
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<td>240</td>
<td>240 - 240</td>
<td>240</td>
<td>240</td>
<td>240</td>
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<td>Frequency (GHz)</td>
<td></td>
<td></td>
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<tr>
<td>Receiver Integration Level</td>
<td>OEK demod.</td>
<td>LNA, IQ mixer</td>
<td>LNA, IQ mixer</td>
<td>LNA, IQ mixer</td>
<td>LNA, IQ mixer</td>
<td>LNA, IQ mixer</td>
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<tr>
<td>RF Rx 3dB Linear B/W (GHz)</td>
<td>15</td>
<td>24</td>
<td>35</td>
<td>35</td>
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<td>35</td>
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<tr>
<td>RF Tx 3dB Linear B/W (GHz)</td>
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<tr>
<td>TRX 6-dB Saturated RF B/W (GHz)</td>
<td>26</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>40</td>
<td>35</td>
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<tr>
<td>TRX 6-dB Linear RF B/W (GHz)</td>
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<tr>
<td>Transmission type</td>
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<td>QPSK/BPSK</td>
<td>QPSK/BPSK</td>
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<td>QPSK/BPSK</td>
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<tr>
<td>LO architecture</td>
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<td>coherent</td>
<td>non-coherent</td>
<td>coherent</td>
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<tr>
<td>RF bandwidth</td>
<td>60 GHz VCOs+3</td>
<td>x16</td>
<td>x16</td>
<td>x16</td>
<td>x16</td>
<td>x8</td>
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<tr>
<td>BER (dBi)</td>
<td>+5</td>
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<td>21</td>
<td>25 - 27</td>
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<tr>
<td>T2 Gain (dB)</td>
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<td>NEXP (dB)</td>
<td>19</td>
<td>15</td>
<td>9.6</td>
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<td>15</td>
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<td>Range (cm)</td>
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<td>70</td>
<td>100</td>
<td>100</td>
<td>1</td>
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<td>Symbol rate (GHz)</td>
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<td>12.5</td>
<td>35</td>
<td>10.7</td>
<td>5.8</td>
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<tr>
<td>BER at data rate (Gbps)</td>
<td>10 OEK</td>
<td>25 QPSK</td>
<td>55 BPSK</td>
<td>55 BPSK</td>
<td>10 OEK</td>
<td>50 BPSK</td>
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<td>Demonstration data rate (Gbps)</td>
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<td>BER (%)</td>
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<td>EIRP (dBi)</td>
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<tr>
<td>B/MS (mW)</td>
<td></td>
<td></td>
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<tr>
<td>Transmitter efficiency (pA/µm²)</td>
<td>68.8</td>
<td>41</td>
<td>14.7</td>
<td>23.14</td>
<td>0.64%</td>
<td>18.75, 15</td>
</tr>
<tr>
<td>Receiver efficiency (pA/µm²)</td>
<td>48.5</td>
<td>34.6</td>
<td>15.3</td>
<td>26.16</td>
<td>2.44%</td>
<td>28.75, 23</td>
</tr>
<tr>
<td>BER (%)</td>
<td></td>
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</table>

1 In saturated conditions; 2 Including antenna and lens gain; 3 Maximum gain setting; 4 Compensated for output pad.

* Minimum single side band noise figure. * Average single side band noise figure.

a LNA noise figure. b Probed baseband input and output. c with no LO generation circuitry. d With real time scope post processing including adaptive channel equalizer and amplitude limiting.

coherent detection is approached. A broadband hybrid balun is utilized as a power splitter to drive the transmitter and the receiver. An analog phase shifter is also connected in the path of the transmitter LO to further tune the phase shift if needed to approach the maximum signal to noise ratio.

In order to quantify the wireless link bandwidth including all cascaded blocks till the board connector level, single-tone measurements were conducted. The input baseband signal frequency was swept at a constant LO frequency while the output signal was monitored using a spectrum analyzer. This sweep was performed for different LO frequencies to evaluate its effect on the performance. As shown in Fig. 24(a), a 6-dB bandwidth of 35 GHz was measured at LO of 240 GHz when the transmitter is in saturation, while in 8-dB back-off conditions a 20-GHz RF bandwidth was measured, as shown in Fig. 24(b). To test the wireless link capabilities, data transmission was tested using a bit pattern generator to create a broadband BPSK signal at the transmitter input and a sampling scope at the receiver output for analyzing the received data. For BPSK modulation scheme, no back-off power is required and the transmitter operates in saturation. Eye diagrams for different data rates of 8, 16, 20, and 25 Gb/s with a 32-bit long pseudorandom binary sequence (PRBS31) and no post processing are shown in Fig. 25. In order to quantify the link performance further, a BER tester was connected in place of the sampling scope. The bathtub curves depicted in Fig. 26 show that 20 and 25 Gb/s data rates are achieved with BERs of $6.3 \times 10^{-9}$ and $2.2 \times 10^{-4}$, respectively, which allows to perform forward error correction algorithms. A link range of 15 cm was kept in this experiment because of the setup physical limitations arising from sharing the LO signal. The effective isotropic radiated power (EIRP) was calculated from the on-wafer transmitter saturated output power of $-0.8$ dBm and the measured combined antenna and optical lens gain of 14 dBi to be 13.2 dBm.

Various communication links have been presented in the literature. Table I summaries the main performance parameters of the mostly related works. The integration level and the packaging level strongly affect the performance parameters. In this paper, the modified mixer architecture and optimized design allows the current paper to achieve the largest receiver bandwidth of 55 GHz with high gain enabling the BER measurements with no external amplifiers or post processing. The presented symbol rate and system bandwidth outperform the previously published work at carrier frequencies above 200 GHz, except of [18] which utilizes signal post-processing, doing adaptive channel equalization and amplitude limiting, and [7] which operates at a carrier frequency of 190 GHz.
bandwidth among the state of the art for fully integrated solutions above 200 GHz, demonstrating very high symbol and data rates with no post-processing and long bit streams of 32.

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REFERENCES


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