Electrical study of radiation hard designed HfO_2-based 1T-1R RRAM devices

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ABSTRACT

In this work the electrical performance of a radiation hard designed 1T-1R resistive random access memory (RRAM) device is investigated in DC (voltage sweep) and AC (pulsed voltage) modes. This new device is based on the combination of an Enclosed Layout Transistor (ELT) used as selector device and a TiN/ HfO_2/ Ti/TiN RRAM stack used as resistive device. The high cell to cell variability in the DC mode makes it difficult to define an electrical gap between the High Resistive State (HRS) and the Low Resistive State (LRS). The strong reduction of the variability by the use of Incremental Step Pulse with Verify Algorithm (ISPVA) makes the later a mandatory programming approach. The Quantum Point Contact (QPC) model defines an energy barrier located in the rupture point of the filament in HRS. The compensation between the width and height variations of this barrier during cycling could explain the stability of HRS and LRS. The good performance of the proposed device using the ISPVA programming approach makes it a good candidate for Rad-Hard Non Volatile Memories integration.

INTRODUCTION

Semiconductor memories, both volatile and non-volatile, are mostly integrated using standard processes and standard architectures. This means that the standard silicon memory devices, such as flash memories, are Rad-tolerant but not Rad-Hard. Therefore, for applications in radiation environments a new approach is required to avoid radiation-related failures.

Resistive Random Access Memories (RRAM) are intrinsically radiation tolerant [1], thus a proper candidate to achieve the mentioned target. Nowadays, RRAM based on HfO_2 is one of the most promising technology candidates due to its full compatibility with CMOS processes. Its behavior is based on the electrical modification of the conductance of a Metal-Insulator-Metal (MIM) stack: the set operation moves the cell into a Low Resistive State (LRS), whereas reset operation brings the cell back to a High Resistive State (HRS). The switching effect of the RRAM devices is determined by the formation and modification of conductive filaments composed of oxygen vacancies, which are controlled through the motion of such vacancies by an applied electric field [2-4].

Nevertheless, the 1T-1R structure of the memory array consists of NMOS access transistors, which are sensitive to radiation [5]. In advanced CMOS technologies with thin gate oxides, the leakage paths along the shallow trench edges become the major contributor to the total ionizing dose (TID) effect of NMOS. A suitable approach to eliminate the leakage path in NMOS transistors is to adopt a gate-enclosed layout [6]. Therefore, we present a 1T-1R cell based on the combination of an Enclosed Layout Transistor (ELT) and a TiN/HfO_2/Ti/TiN based resistor.

In order to study the electrical performance of the rad-hard RRAM cells a complete characterization was performed in AC mode, through the Incremental Step Pulse with Verify

Algorithm (ISPVA) [7-9], and in DC mode, providing in addition data for the filament constriction modeling using the Quantum-Point Contact (QPC) model [10-12].

EXPERIMENT

The 1T-1R memory samples are composed of a select ELT transistor manufactured in a 250 nm CMOS technology, which also sets the current compliance, whose drain is in series to a Metal-Insulator- Metal (MIM) stack. The MIM cell integrated on the metal line 2 of the CMOS process is a TiN/HfO_2/Ti/TiN stack of 150 nm TiN layers deposited by magnetron sputtering, a 7 nm Ti layer, and a 9 nm HfO_2 layer grown by Chemical Vapor Deposition (CVD). The MIM cells area is 700 x 700 nm^2. The TEM cross view of the Rad Hard designed 1T-1R cell and the circuit schematics are illustrated in Figure 1.

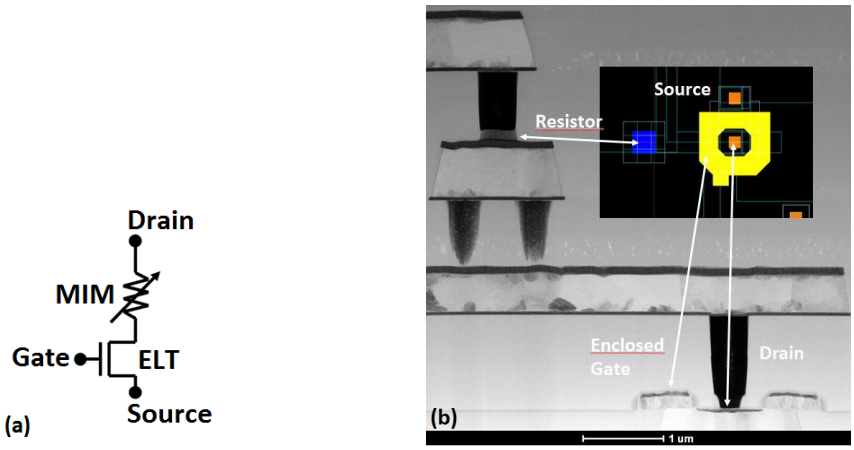

Figure 1. Circuit schematics (a) and TEM cross-sectional image of 1T-1R architecture with an ELT transistor and a 0.7 x 0.7 μm^2 MIM cell (b).

In the DC measurement mode, double voltage sweeps were applied on the cell Source/Drain terminals (Figure 1(a)), corresponding to reset/set and forming operation respectively, while recording the I-V curves. The first sweep starts at 0 V and stops at 5 V with step heights of 0.05 V, whereas the second one follows the opposite voltage trail recording the current value at 0.2 V defining the HRS/LRS currents, respectively. The applied transistor gate voltage values were V_G = 2.8 V and V_G = 1.3 V, respectively.

In the AC characterization mode the ISPVA was applied. This technique consists of a sequence of increasing voltage pulses (V_{PULSE} = 0.2-5 V, V_{STEP} = 0.1 V, t_{PULSE} = 10 µs, $t_{FALL/RISE}$ = 1 µs) on the drain terminal during set and forming operation, whereas this sequence of pulses is applied on the source terminal during the reset operation. The applied voltage values V_G were the same as in DC mode, respectively. After every pulse a Read-verify operation is performed with V_G = 1.3 V, V_{READ} = 0.2 V (applied at the drain contact) for 10 µs. When the read current reaches the target value of 6 µA the set and forming operations are stopped, whereas the reset operation is stopped when the target value of 3 µA is achieved.

From the reset I-V characteristics measured in the DC mode, the analysis of the conductive filament properties using the QPC model was performed. The model is based on the idea that in HRS a constriction point (rupture point) is formed in the filament (Figure 2(b)),

defined by an energy barrier (Figure 2(a)). Thereby, the HRS current can be calculated by the following expression [9]:

$$I_{HRS} = \frac{2e}{h} G / G_0 \left(eV + \frac{1}{\alpha} \ln \left[\frac{1 + e^{\alpha(\phi - \beta eV)}}{1 + e^{\alpha(\phi + [1-\beta]eV)}} \right] \right) \quad (1)$$

where ϕ is the barrier height (bottom of the first quantized level), α is a parameter related to the inverse of the potential barrier curvature (assuming a parabolic longitudinal potential), β defines the position of the constriction point with respect to the two electrodes, G/G_0 is a conductance parameter equivalent to the number of filaments, and $G_0 = 2e^2/h$ is the quantum conductance unit corresponding to the creation of a single mode nanowire where e is the electron charge and h the Planck's constant.

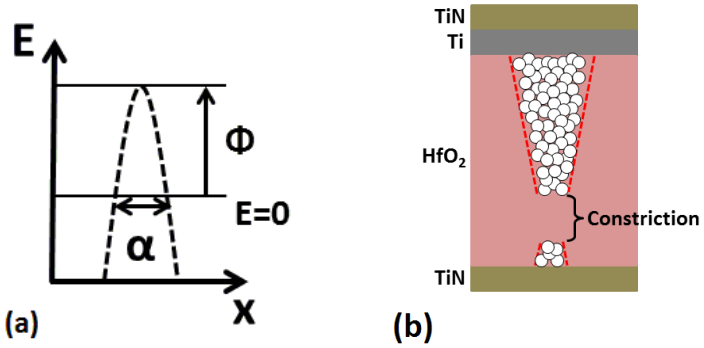

Figure 2. Schematic illustration of QPC barrier parameters (a) and of the conductive filament shape after reset (HRS) (b).

DISCUSSION

In order to activate the resistive switching behavior, the RRAM devices require a preliminary forming step. This initial operation plays a fundamental role in determining the subsequent device performance. In Figure 3 the forming voltages and LRS current values measured in DC and AC modes in 80 devices are compared. There are no substantial differences in the forming voltage distributions, nevertheless the variability of the forming currents is strongly reduced by ISPVA.

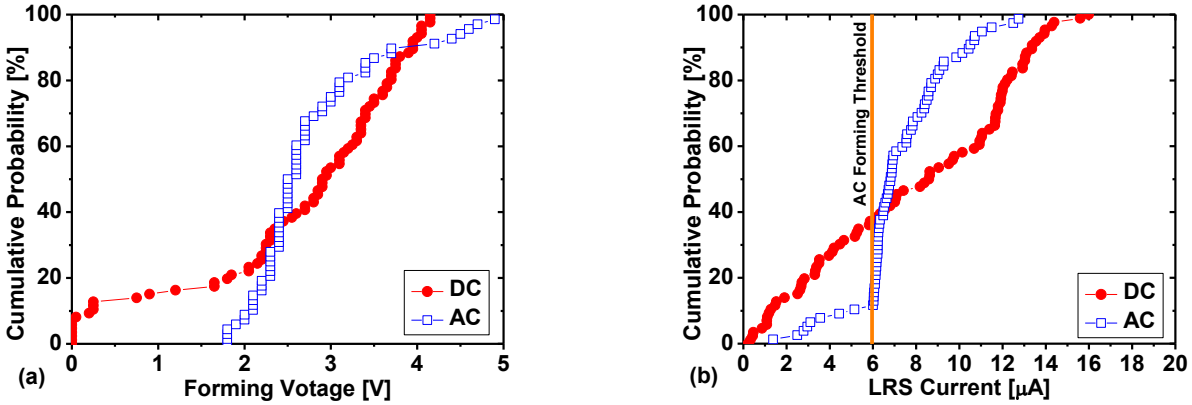

Figure 3. Cumulative distributions of forming voltages (a) and LRS currents (b) in both modes.

The distributions of the reset/set parameters are illustrated in Figure 4. In agreement with previous publications [13], the reset voltages are larger than the voltages required to set the filaments. As shown in Figure 4(b), there is no clear window between HRS and LRS in the DC mode. In contrast, the ISPVA lead to an evident gap defined by current thresholds of 3 and 6 µA, respectively. Therefore, the use of such algorithms is mandatory in order to define the HRS and LRS levels with strongly reduced cell to cell variability.

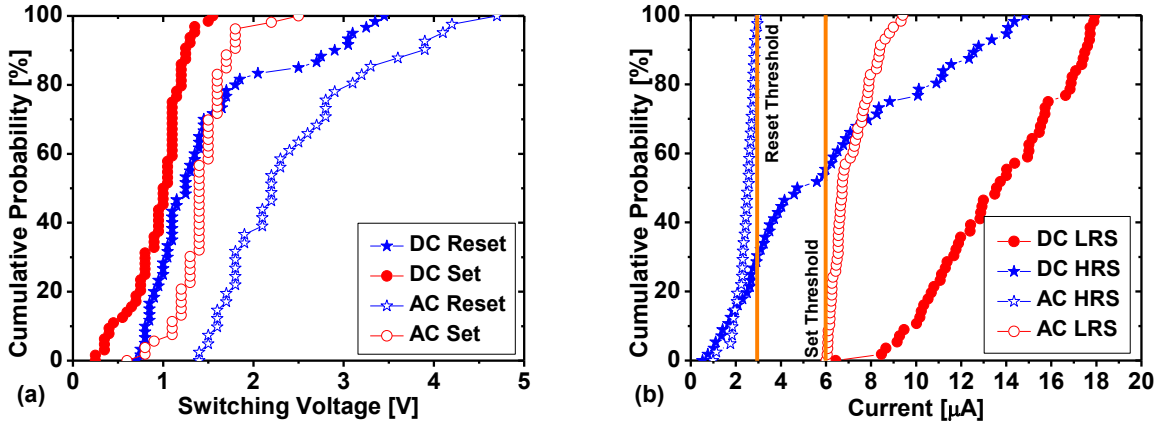

Figure 4. Cumulative distributions of the reset/set voltages (a) and HRS/LRS currents (b) in DC and AC mode.

The endurance performance of the best 11 devices has been verified by 100 cycles. Good switching voltage stability is shown in Figure 5(a), except for reset in the AC mode. During cycling, the current values remain stable. According to Figure 5(b), the DC mode provides better current ratio (~3) than the AC mode (~2). Nevertheless, the average values shown in Figure 5(b) do not take into account the higher cell to cell variability in the DC mode. Therefore, the ISPVA remains a better approach to program the devices.

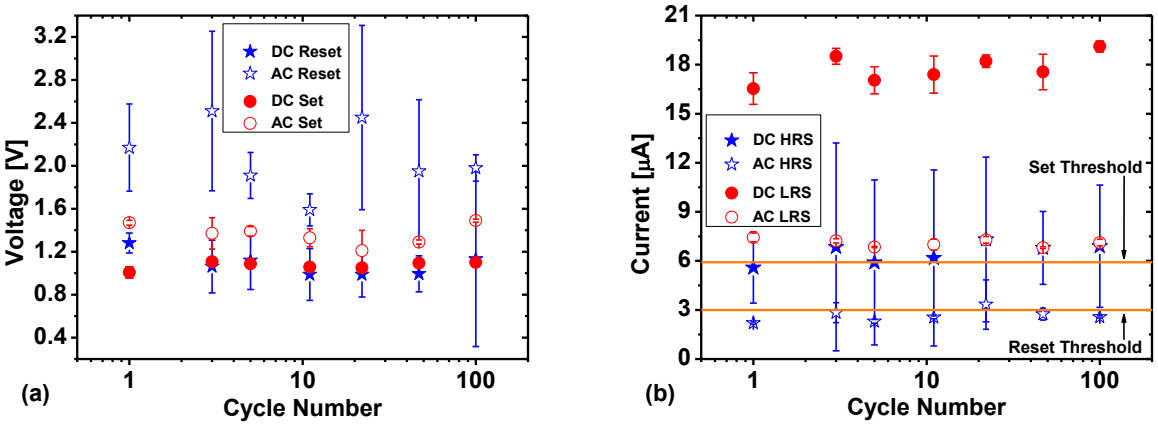

Figure 5. Average and dispersion values of reset/set voltages (a) and of HRS/LRS currents (b), received by applying DC and AC modes as function of cycling.

In order to study the evolution of the filament constriction as function of cycling, the QPC model was applied to the experimental HRS curves after reset operation as shown in Figure

6. According to the QPC model [9], the current of a single filament is defined by $I = G_0V$, as illustrated by the dashed line.

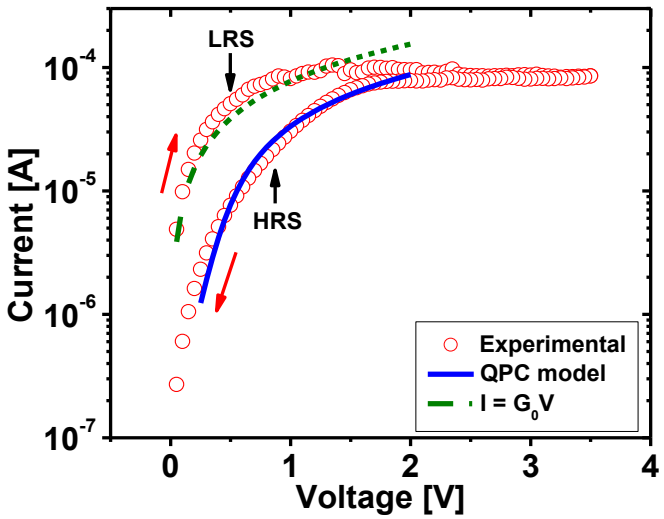

Figure 6. Reset I-V characteristics measured in DC mode. The solid line represents the adaption of the QPC model detailed by equation 1.

Using equation 1 the QPC parameters (ϕ, α and β) were extracted as illustrated in Figures 7(a) and (b). Alpha and phi show opposite evolutions, and their product remains constant as illustrated in Figure 7(c). The correlation between these two parameters can explain the current stability during cycling [14]. Beta remains constant around 0.85 locating the constriction point near the bottom contact.

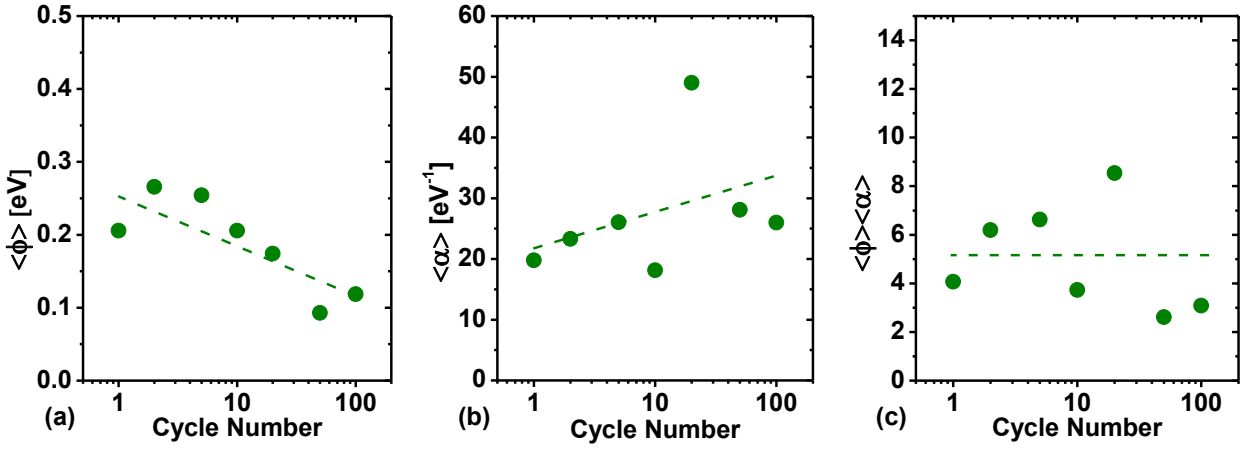

Figure 7. Average values of the ϕ (a) and α (b) parameters and their product (c) as function of cycling.

CONCLUSION

The switching performance of 1T-1R devices based on ELT as the selector device has been investigated in AC and DC modes. Caused by the high cell to cell variability in the DC

mode it is not possible to define a clear gap between HRS and LRS. The reduction of the cell to cell variability by applying the ISPVA makes it a mandatory approach for programming operations. In cycling, the compensation effect between QPC parameters (ϕ and α) seems to be responsible for the current stability. The good performance of the devices, programmed using the ISPVA, makes thus RRAM-based ELT approach a good candidate to be a Rad-Hard Non Volatile Memory solution.

ACKNOWLEDGMENTS

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