# Monolithically Integrated MZM with Segmented Driver in Photonic BiCMOS showing High ER

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***Abstract*—In this work, a Si depletion-type MZM monolithically integrated with a segmented driver using 0.25 μm SiGe:C photonic BiCMOS technology is demonstrated. The phase shifter has a total length of 6.08 mm and is divided into 16 sections which are driven by the driver segments. Electro-optic time-domain measurements show extinction ratio higher than 12 dB at 28 and 32 Gb/s with a differential input voltage swing equal to 800 $mV_{pp}$. This is one of the highest extinction ratio values shown by a monolithically integrated Si MZM at those data rates. The driver dissipates a total DC power equal to 1.8 W.**

***Index Terms*—optical transmitters, silicon, integrated optoelectronics.**

## I. Introduction

COHERENT transmission systems and advanced modulation techniques are becoming increasingly attractive in data center applications. Because of the system requirements in speed, extinction ratio (ER), loss and linearity, modulator devices are currently based on lithium niobate ($LiNbO_3$) technology. Silicon (Si) photonics has drawn significant attention recently due to the need for a broadband communication technology at a relatively low cost offered by the electronic-photonic integration platforms. The on-chip fabrication of opto-electronic devices enables design flexibilities that allow for the optimization of the transmitter performance. The carrier depletion-based Si Mach-Zehnder modulator (MZM) is considered a promising candidate for this technology mainly because of its large intrinsic bandwidth and the simplicity in fabrication [1]–[3].

State-of-the-art depletion type Si MZMs are typically based on traveling-wave electrodes (TWEs) used to achieve high-speed operation [4]. Common TWE designs consist of phase shifters with length equal to approximately 4-5 mm so as to provide $V_\pi$ of the order of 6 V. This value of $V_\pi$ is significantly large and non compatible with modern digital to analog converters (DACs). Consequently, the major drawback of Si MZMs so far is the large peak-to-peak voltage required in order to be driven effectively. In case the input voltage swing is much less than $V_\pi$ they are under-driven, thus showing low ER. In order to further reduce $V_\pi$ and make Si MZMs compatible with digital signal processing (DSP) systems, longer phase shifters would be necessary. However TWEs have been considered inefficient for this mainly because of the microwave loss on the transmission line which results in no improvement in the efficiency at high frequencies despite the length increase [5]. A different approach to this problem is the segmented MZM (SE-MZM) design in which the driver is distributed along the phase shifter. With this technique good velocity matching can be achieved which is a critical issue when using long phase shifters. Another advantage is that high ER is expected since the radio frequency (RF) voltage is kept constant along the phase shifter. Using this topology the modulator bandwidth is expected to be independent of the phase shifter length and it will only depend on its RC constant which is typically small enough to provide high-speed operation.

We implement such an MZM-driver design by using photonic-electronic integration which enables the fabrication of photonic components in the immediate vicinity of bipolar complementary metal oxide semiconductor (BiCMOS) electronics. More specifically the MZM is integrated in the frontend of a high performance BiCMOS technology with $f_T$ and $f_{max}$ of about 200 GHz [6]. BiCMOS offers a superior $f_T \times V_{breakdown}$ in comparison to CMOS technologies [7] and is therefore preferred for our driver design.

In our previous work we had demonstrated our monolithic integration concept by presenting a 10 Gb/s MZM with driver [8]. However, that device had limited speed and ER due to transmission line-based driver design and small phase shifter length, thus resulting in large $V_\pi$. In the current work we demonstrate for the first time the SE-MZM concept on long Si modulators (6 mm) that offers the possibility to minimize driving voltage without sacrificing available bandwidth. 28 and 32 Gb/s on-off keying (OOK) operation is presented showing more than 12 dB ER with differential input voltage swing equal to 800 $mV_{pp}$. Such a low value of input voltage makes our device compatible with commercial DACs. The ER of the SE-MZM presented here is one of the highest reported among similar topologies [9]. Other high ER Si-based devices are using asymmetric Mach-Zehnder interferometers (MZIs) [4], [10] which are not preferred for commercial applications due to temperature sensitivity and wavelength drifts. Our results indicate that Si-based transmitters could be suitable for future

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long-haul application systems.

## II. Circuit Description

The circuit is fabricated using IHP's 0.25 μm SiGe:C BiCMOS process [6]. Initially an 8 inch silicon-on-insulator (SOI) wafer with a top Si layer of 220 nm and a buried oxide (BOX) layer of 2 μm is used. Then a module called 'local SOI' is implemented in the process flow to produce SOI and bulk regions located close to each other. The SOI areas are used for the fabrication of the photonic components while the electronic devices are formed on bulk Si regions. In Fig. 1 a microphotograph of the monolithically integrated SE-MZM is shown where all the main chip components are noted. The chip area is approximately 12.7 mm$^2$ (9.8 mm x 1.3 mm).

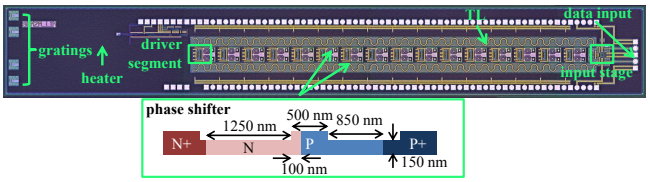


Fig. 1. Microphotograph of the monolithically integrated Si SE-MZM.

### A. MZM

The device is based on a symmetric MZM structure so as to be suitable for commercial applications. The phase shifter has a length of 6.08 mm and is divided into 16 segments, each of which can be considered as a lumped element for data rates up to 40 Gb/s and is driven by a separate driver. The phase shifter is based on a PN junction formed inside the waveguide using self-aligned process. With this technique larger confinement between the optical mode and the depletion region can be achieved without increasing the complexity of the process. Consequently this type of junction shows lower $V_\pi \cdot L$ (Fig. 2) than our previous demonstrations [11]. The target boron doping concentration is chosen to be equal to $3{\cdot}10^{17}$ cm$^{-3}$ while arsenic doping concentration is targeted at $1{\cdot}10^{18}$ cm$^{-3}$. Larger doping concentration would result in lower $V_\pi \cdot L$ but it would increase significantly the absorption loss. The highly-doped regions are placed at a distance far enough from the waveguide core to not cause additional absorption loss (Fig. 1). At the p-side the distance to the highly-doped region is designed to be smaller than the n-side because of being lower-doped thus resulting in larger resistivity at the p-side. A series resistance of approximately 50 Ω is estimated per segment. The high value of series resistance is a significant limiting factor for the modulator bandwidth. The device performance could be further optimized by using additional masks with intermediate doping levels that could be approached closer to the waveguide and would reduce the series resistance significantly without adding extra absorption loss [4].

The total fiber-to-fiber optical loss is of the order of 19 dB. The insertion loss due to the phase shifter itself is estimated to be approximately 6 dB. For coupling the light in and out from the chip two standard grating couplers are used which are responsible for approximately 8 dB loss (4 dB each). The remaining loss can be attributed to the multimode interference (MMIs) devices, the waveguide parts that connect the optical components as well as the 1.5 mm long heaters designed to provide DC tuning.

### B. Segmented Driver

The driver amplifier part integrates two stages. The input stage which is matched to 50 Ω, drives a differential signal to two single-ended transmission lines. The second stage is distributed laterally to the modulator segments. Each driver segment samples the differential voltage from the lines, amplifies it and applies it to each modulator section. The segments are simulated by using their equivalent electrical model loaded by the phase shifter depletion capacitance and series resistance. The modulator load represents the dominant pole that determines the MZM bandwidth. Each driver segment dissipates power equal to almost 110 mW. The driver is strategically positioned between the MZM arms for symmetry reasons.

In order to optimize the MZM' s electro-optic (EO) response the transmission lines are properly folded to create an artificial delay between the electrical and optical signal. Using this technique the timing difference of both waves between segments is matched to a value of 4.6 ps thus achieving velocity matching. Furthermore, to minimize the electrical loss due to the transmission line, its characteristic impedance is designed to be 40 Ω. This impedance results into wider lines with less microwave loss than the conventional 50 Ω. The lines are terminated with resistors with the same resistance value. More details about the electrical circuit are described in our previous work [11].

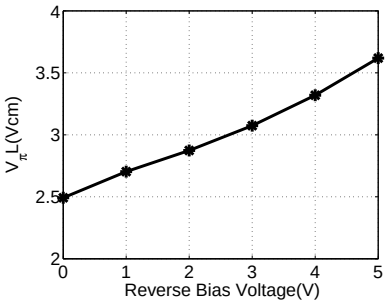


Fig. 2. Phase shifter inverse efficiency $V_\pi \cdot L$ extracted from measurements.

## III. Co-Simulation Technique

The integrated SE-MZM system is simulated as follows. The optical depletion-type phase shifter is modeled by using device simulation tools as described previously [12]. With this technique the refractive index as well as the phase shifter absorption loss change with applied voltage are calculated. The values of the depletion capacitance and the series resistance are also estimated using Sentaurus TCAD. In Fig. 3 the measured and simulated depletion capacitance change with applied voltage is shown. The measurement curve represents multiple chips in order to show the deviation from the simulated curve. The optical delay is also calculated so as to analyze

the effects of velocity mismatch. After having calculated all these parameters the phase shifter can be treated as an optical component described by the above properties.

In the next step the optical components such as phase shifters, MMIs and DC tuning sections are implemented into a standard electronic design platform such as Cadence Virtuoso by creating instances using VerilogA. VerilogA models for optical components have already been shown [13]. The segmented driver was also simulated by using Cadence Virtuoso and consequently the optical and electrical components are easily combined together so as to predict the modulator EO response. The simulation setup can be easily adapted in order to predict time-domain behavior or frequency response of the MZM. It is also simple to expand the co-simulation in order to simulate different MZM topologies such as IQ modulators.

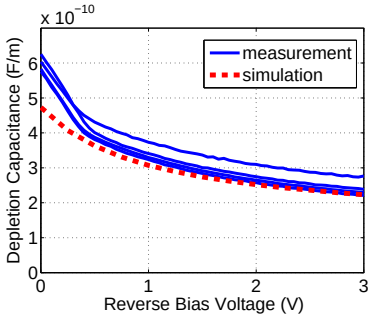


Fig. 3. Phase shifter depletion capacitance change with reverse bias voltage.

## IV. Measurement Results

The EO frequency response of the SE-MZM was characterized using a Keysight 67 GHz lightwave component analyzer (LCA). The measurements were performed on wafer with a 67 GHz GSGSG RF probe. The MZM EO $S_{21}$ is depicted in Fig. 4. A 3 dB bandwidth of approximately 18 GHz is measured when the reverse bias voltage ($V_{bias}$) is equal to 1 V. By changing the bias voltage of the modulator the bandwidth increases due to the depletion capacitance reduction. The peaking observed at high frequencies can be attributed to non-optimal on-chip supply decoupling and can be minimized in future designs.

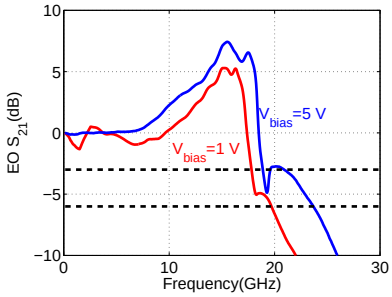


Fig. 4. Normalized measured EO $S_{21}$ with frequency when $V_{bias}$ is equal to 1 and 5 V.

For the optical eye-diagram measurement a bit pattern generator provided a $2^{31}$-1 pseudo random binary sequence (PRBS). The differential output was connected to the modulator RF input for OOK demonstration. The differential input voltage amplitude was equal to 800 $mV_{pp}$. At the optical input a continuous wave (CW) laser signal was injected. At the optical output an erbium-doped fiber amplifier (EDFA) was used to reamplify the signal for subsequent evaluation. For the eye measurements of the generated data sequence a photodetector was connected to the input of a sampling head of an oscilloscope. Photodetector and sampling head have a bandwidth of 50 and 70 GHz respectively.

In Fig. 5 the measured as well as the co-simulated optical eye diagrams at 28 and 32 Gb/s are shown when $V_{bias}$ is equal to 1 V. Good agreement between measurement and simulation proves the accuracy of our co-simulation technique. ER 13.2 and 12.0 dB was measured at 28 and 32 Gb/s respectively. The high value of ER can be attributed to the fact that the long phase shifter (6.08 mm) enabled to fully drive the MZM. This conclusion was derived after observing that an increase in the input voltage swing beyond 800 $mV_{pp}$ was saturating the modulator performance. Furthermore, the large number of segments (16) allowed for the RF voltage to be kept constant all along the phase shifter. Higher values of reverse bias voltage were also tested because they are expected to increase the MZM cut-off frequency (Fig. 4). However due to the trade-off between bandwidth and phase shifter efficiency with reverse bias voltage (Fig. 2) a significant reduction in the ER was observed for larger values of $V_{bias}$. The jitter noticed at 32 Gb/s is due to the limited bandwidth at this data rate.

The total power consumption of the device is equal to 1.8 W. This large value of power dissipation is the trade-off to the large number of segments that are necessary to demonstrate high ER. Moreover, the driver incorporates a linear topology suitable for pulse amplitude modulation (PAM) systems. This functionality will be shown in the near future.

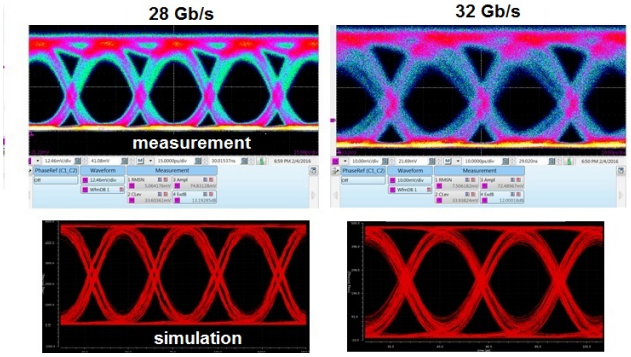


Fig. 5. Measured and simulated EO eye-diagrams at 28 and 32 Gb/s when $V_{bias}$ is equal to 1 V.

## V. Conclusion

A monolithically integrated Si depletion-type MZM with a linear segmented driver in IHP's photonic BiCMOS process is demonstrated. High ER is measured at 28 and 32 Gb/s with input voltage swing equal to 800 $mV_{pp}$ a value compatible with modern DACs. The high ER together with the linear driver topology are crucial for the future demonstration of coherent

systems based on SE-MZM IQ modulators [7], [14]. Further decrease in the total loss figure is however required in order to make Si SE-MZMs competitive towards $LiNbO_3$ devices. Our technology predicts that total loss of the order of 13 dB can be expected from the same chip design by further optimizing the process and phase shifter specifications. Further decrease in loss would require different coupling mechanisms or more efficient PN junctions [12] that would result in shorter phase shifters thus providing the same $V_\pi$ but smaller absorption loss [15]. In terms of speed, our device could be further optimized by using a photonic BiCMOS technology with faster bipolar transistors [16] and by reducing the phase shifter series resistance with the implementation of additional doping masks in our process.

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