

# Impact of HfO<sub>2</sub> deposition techniques on the switching parameters in embedded 1T-1R cells and arrays

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## Abstract

Resistive RAM technology is on a maturity level that calls for its integration in array structures. This requires a perfect understanding of the cells performance and reliability in relation to the process steps used for their manufacturing. In this paper, through and extensive characterization of 1T-1R cells, it is performed a comparison of the cell-to-cell variability and reliability of different HfO<sub>2</sub> deposition processes exploited as dielectric for the MIM element of the cell. Cells behaviour during Forming, Set and Reset operations is monitored in order to analyze their peculiarity in terms of conduction behavior activation and process-induced variability of the switching voltages.

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## 1. Introduction

Resistive Random Access Memories (RRAM) gathered increasing interest in the last few years [1], [2]. However, an extensive research activity is still to be performed on this innovative technology in order to improve RRAM reliability and performance for array level integration. RRAM behavior is based on the possibility of electrically modifying the conductance of a Metal-Insulator-Metal (MIM) stack: the Set operation moves the cell in a low resistive state (LRS), whereas Reset switch the cell back to a high resistive state (HRS) [3]–[7]. The Ratio between LRS and HRS is defined as Resistance Ratio, while switching voltages are those applied to the cells to toggle between HRS and LRS states. To activate such a switching behavior, some technologies require a preliminary Forming operation [8]–[10]. The choice of proper MIM technology for RRAM with good uniformity and low switching voltages is a key issue for optimized electrical operations [11]–[13]. In this work a comparison in terms of cell-to-cell variability and reliability of different HfO<sub>2</sub> Atomic Vapour Deposition (AVD) processes on 1T-1R cells is performed. Cell behavior during Forming, Set and Reset is monitored through an incremental pulse and verify algorithm [14], [15] in order to analyze the peculiarity of each cell in terms of the switching behavior activation and the

process-induced intercell variability of the threshold voltages, on 100 cells for each process.

## 2. Experimental

A standard 0.25 μm CMOS process line was employed. Figure 1 illustrates the final structure of the device. Firstly, the NMOS transistors were processed, with width (W) of 1.14 μm and length (L) of 0.24 μm. The resistive switching cell was then placed between the metallization levels 2 and 3. In order to reduce the surface roughness of the bottom electrode, a 20 nm-thick TiN layer was additionally deposited by atomic vapour deposition (AVD), using liquid metal organic TEMAH precursor. Finally, HfO<sub>2</sub> was capped by 7 nm ionized metal plasma (IMP) Ti and 150 nm PVD TiN.

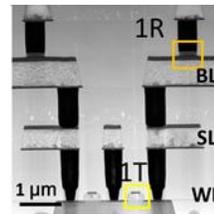


Fig. 1: TEM cross-sectional image of 1T1R architecture with a NMOS access transistor (1T, marked by a yellow square) and a 0.4 μm<sup>2</sup> MIM cell (1R, marked by an orange square).

The Forming/Set/Reset operations on the arrays were performed by using an Incremental Pulse and Verify algorithm. Reset operations were performed by applying the highest voltage available (2.8 V) to maximize the cells switching yield while avoiding the breakdown of the MIM. Pulses were applied during Forming by increasing V with  $\Delta V=0.01V$ , whereas during Set and Reset  $\Delta V = 0.1V$  has been used. Each pulse featured duration of  $10\mu s$ , with a rise/fall time of  $1\mu s$  to avoid overshoot issues. Set operation was stopped on a cell when the read-verify current reached the threshold value of  $20\mu A$ , whereas Reset was stopped when  $10\mu A$  was reached.

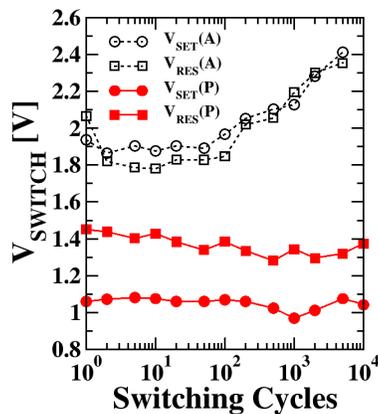


Figure 2:  $V_{SET}$  and  $V_{RES}$  average values of amorphous (A) and polycrystalline (P)  $HfO_2$  based cells as function of cycling.

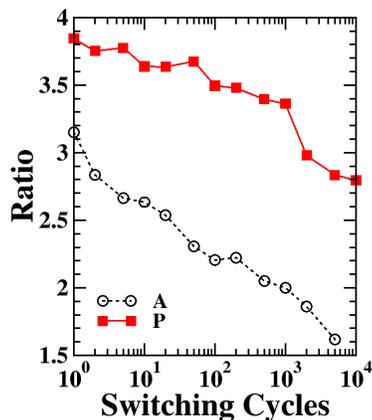


Figure 3: HRS/LRS ratio of amorphous (A) and polycrystalline (P)  $HfO_2$  based cells as function of cycling.

#### 4. Conclusion

The different performance of several  $HfO_2$  deposition processes for RRAM applications have been investigated. Quantum point contact modelling allowed understanding the physical properties of each process by analyzing the conductive filament properties. The grain boundaries conduction in the poly-crystalline  $HfO_2$  structures could be the reason of the high cell-to-cell variability. The use of tuned deposition parameters allowed obtaining amorphous  $HfO_2$  instead of poly-crystalline, resulting in the highest inter-cell and intra-cell uniformity, as evidenced by electrical characterization and model fitting parameters. Metal-organic precursors-based processes result in amorphous  $HfO_2$  films as well, although featuring higher carbon content than other processes. The inter-cell uniformity seems to be affected by carbon: processes with high carbon content show reduced Resistance Ratio and increased variability of the Set and Reset parameters.

#### References

- [1] S. F. Karg et al., IBM Journal of Research and Development, vol. 52, no. 4.5, pp. 481–492, 2008.
- [2] R. Waser, Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices. New York, NY, USA: John Wiley & Sons, Inc., 2003.
- [3] G. Bersuker et al., J. Appl. Phys. vol. 110, no. 12, pp. –, 2011.
- [4] S. Yu, X. Guan, and H.-S. Wong, IEEE Trans. on Electron Devices, vol. 59, no. 4, pp. 1183–1188, 2012.
- [5] F. T. Chen et al., Science China Information Sciences, vol. 54, no. 5, pp. 1073–1086, 2011.
- [6] C. Zambelli et al., in IEEE Int. Conf. on Microelectronics Test Structures (ICMETS), Mar 2014, pp. 27–31.
- [7] C. Zambelli et al., IEEE Int. Memory Workshop (IMW), May 2014, pp. 1–4.
- [8] P. Lorenzi, R. Rao, and F. Irrera, IEEE Trans. on Electron Devices, vol. 60, no. 1, pp. 438–443, 2013.
- [9] A. Grossi et al., IEEE Trans. on Electron Devices, vol. 62, no. 8, pp. 2502–2509, 2015.
- [10] A. Kalantarian et al., in IEEE Int. Reliability Physics Symposium (IRPS), April 2012, pp. 6C.4.1–6C.4.5.
- [11] K. Morgan et al., IEEE Int. Symposium on Circuits and Systems (ISCAS), June 2014, pp. 432–435.
- [12] C. Cagli et al., IEEE Int. Electron Devices Meeting (IEDM), Dec 2011, pp. 28.7.1–28.7.4.
- [13] A. Chen and M.-R. Lin, IEEE Int. Reliability Physics Symposium (IRPS), April 2011, pp. MY.7.1–MY.7.4.
- [14] A. Grossi et al., IEEE Int. Memory Workshop (IMW), May 2015, pp. 1–4.
- [15] K. Higuchi et al., IEEE Int. Memory Workshop (IMW), May 2012, pp. 1–4.