Design of Resistive Non-Volatile Memories for Rad-Hard Application

Nicola Lupo*, Cristiano Calligaro†, Roberto Gastaldi†, Christian Wenger‡
, Franco Maloberti*
*Univerity of Pavia, Pavia, Italy
†RedCat Devices, Via Moncucco 22, Milan, Italy
‡IHP-Microelectronics, Frankfurt, Germany

***Abstract*—In this paper a rad-hard design flow for emerging non-volatile memories is discussed. The always growing demand of memory performances is driving to an increasing investigation in new technologies; many emerging technological solutions have been introduced and, as all of them are still an embryonic stage, it is necessary to improve and optimize their characterization process in order to achieve as soon as possible the reliability necessary to stand out in the market. Among them, the resistive memories arose a significant interest for space and high-energy applications. In this scenario, hence, it may be effective and crucial to design an architecture capable to manage different demands like the use in radiation environment. At this purpose a radiation-hardened design of a 1Mbit resistive non-volatile RAM providing full bit DMA access, is proposed. A basic RRAM cell and its structure are explained and the radiation hardened architecture that includes a redundant differential approach presented.**

I. Introduction

In the last years communication technologies have led to a fast and aggressive evolution of the consumer electronics. Personal communications mainly exchange multimedia contents and huge amounts of data are constantly transmitted and stored, thus demanding larger and larger non-volatile memories. Moreover, the Internet of Things (IoT), i.e. the use of smart devices in every aspect of life, leads to complex system architectures in which the embedded non-volatile memories play an always-expanding role. More critical are space applications that require robustness agains radiation damages and very high reliability.

While flash-memories density increases metrics such as endurance, reliability, and overall performance, decline [1]. Therefore, new flash-based structures have been studied in order to obtain larger capacity with sufficient reliability and performances; possible avenues are the 3D approaches, studied for stacked structures and vertical-developed arrays [2]. Beside this, alternative technologies have been developing; among them, the ones based on resistivity change are raising interest because of their cost effectiveness, performance, low-power consumption, and small footprint.

In particular, recent advances in the performance of resistive random access memory (RRAM) have engendered significant interest for system-on-chip (SoC) applications in Si-based CMOS technologies for radiation hard applications [3]. Resistive memories do not store information by mean of charge retention; this grants intrinsic robustness against single event upset (SEU) caused by high-energy particles.

Research is still on going because understanding of the inter-cell and intra-cell variability of memory elements in a memory array is relevant for process optimization [4][5]. An accurate analysis of the real behaviour of the cell array as a memory module is therefore necessary.

This paper analyzes radiation-hard design issues having of 0.25μm CMOS memory technology as implementation vehicle. An accordingly designed prototype will permit experimental processes useful to optimize the technology and improve performances for an effective use of memories in rad-hard applications.

II. The RRAM cell

Given the wide range of possible transition metal oxides, HfO_2-based RRAM provides an ideal CMOS back-end-of-line (BEOL) compatibility with sufficient performance parameters and thus considerable progress has been made in integrating 1T-1R devices as well as in understanding the physical and chemical properties of the resistive switching behavior [6][7].

The basic oxide RRAM cell is based on a Metal-Insulator-Metal (MIM) structure whose technology steps are the following: first the selecting element, the nMOS transistor, is fabricated. After that, featuring width (W) of 1.14μm and length (L) of 0.24μm, the resistive switching cell of MIM is placed between the metal levels 2 and 3, as illustrated in Fig. II. In order to study the impact of the bottom electrode deposition process, an additional AVD TiN with thickness of 20nm is deposited on top of the metal 2 stack. In addition, in order to study thickness dependence, HfO_2 films with thickness of 10nm are deposited at 400C by using AVD method. Finally, HfO_2 is capped by 7nm ionized metal plasma (IMP) Ti and 20nm PVD TiN. The devices is then induced by a 400C/30 min post-metallization annealing (PMA) step.

The described fabrication steps are to fabricate an observable structure implementing the basic concept of a resistive cell: a device with a conductive filament (CF) in it obtained either by varying the intensity of the current flowing through the device (unipolar approach) or by switching the polarity of the voltage applied (bipolar approach). In the second case a lower power dissipation and lower operation time are expected. The simple structure, as it is, has no conductive properties; in

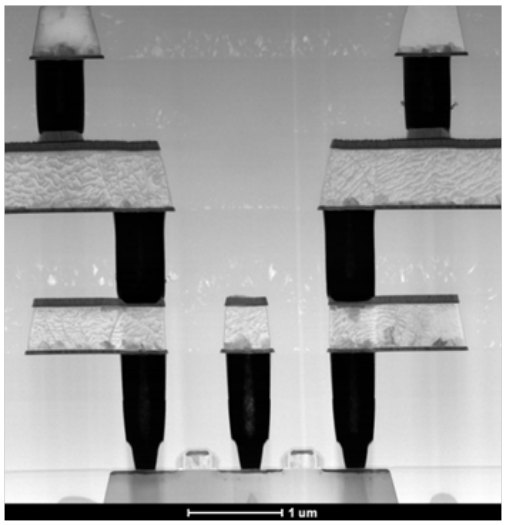


Fig. 1. Transmission electron microscopy image of two 1T-1R cells, sharing the source-contact. The resistive MIM cells are placed on metal 2

order to create a conductive state, the cell has to be initialized via a *forming* operation.

When an electric potential is applied, with the positive pole connected to the Titanium side, a filament of oxygen vacancies between the two plates is obtained. As these vacancies are mobile under the action of an electric field, the filament is conductive (CF) and ensures a current path within the structure: a low resistance state (LRS) is obtained. When a reverse voltage is applied, oxygen vacancies recombine breaking the CF to achieve a high resistive state (HRS) (*reset*). If, again, a direct voltage is applied, the CF is restored bringing the cell to the LRS (*set* operation).

As it happens in flash technology, the stress affecting the cell by the set/reset operation has to be minimized, as it influences the cell lifetime. In order to minimize the stress, a *write and verify* algorithm has to be used: a voltage that increases by step is applied to the cell; after each writing pulse a read operation is performed and when the target conductivity is reached the process stops.

III. Radiation Hardening By Design Approach

Radiation hardening by design is a cost effective approach to the design of integrated circuits for space applications because it is immediately suitable for the integration in conventional technologies. Since it is relevant ensuring reliability, the rate of failures due to radiative effects must be minimized with effective architectures, basic circuits and layout.

The damage caused by radiations can induce either a simple single event transient (SET) or, when propagating, multiple bit upset (MBU). The latter is obviously more critical and used solutions must inhibit soft or hard error propagation inside the device. The strategy can be splitting the whole core in independent sub-arrays (one per bit), each provided with its decoding and control structure (Fig. 2); the redundancy of logic blocks ensures that eventual errors in the device are confined into the single section [8].

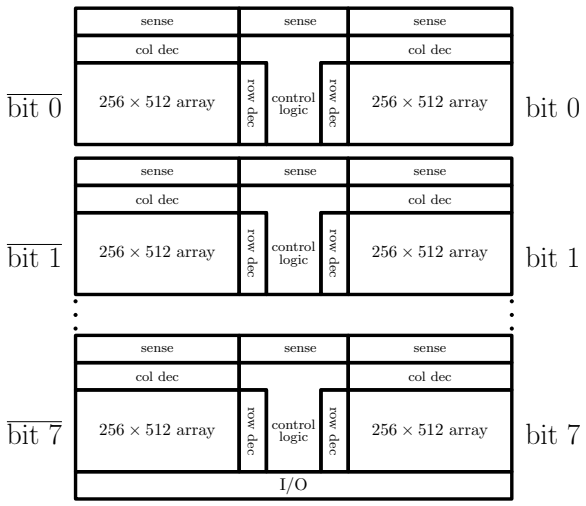


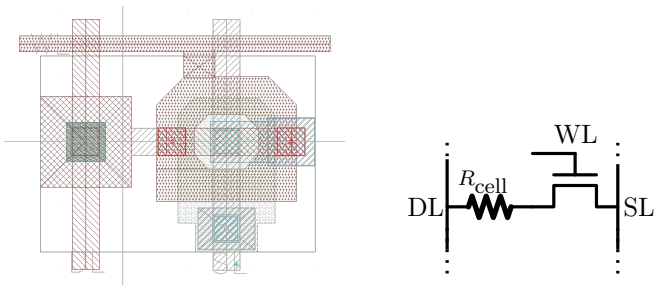
Fig. 2. Block arrangement of the 1Mbit structure.

Thanks to the duplication strategy each block contains a double array where complementary bits can respectively be stored. In such a way, when two complementary cells are accessed, the current difference is maximized and sensing yield is improved, thus extending the reliability even in presence of component degradation.

At the circuit level, it is important to minimize the number of floating nodes, as they are subjected to charge injections due to the radiative phenomena. Therefore, the digital logic must be implemented in a static fully CMOS fashion.

Since errors propagate via the clock distribution, it is a good practice to use asynchronous architectures [8].

A long term phenomenon that affects the reliability of devices is the drift caused by high energy particles. Oxide impurities at the edge of thin and thick oxide layers are traps for the carriers generated by colliding particles and this induces leakage currents leading to the device degradation or to destructive latch-up events. Because of this, edge-less transistors (ELT), including the cell selector, should be used. Fig. 3(a) shows the layout optimal of the basic 1T-1R with the selector implemented with ELT; as shown by the schematic in Fig. 3(b) the connection to both drain-line and source-line grants the bipolar access to the cells.



(a) Layout of the 1T-1R cell; an ELT structure is used.

(b) 1T-1R schematic

Fig. 3. Basic 1T-1R RRAM cell

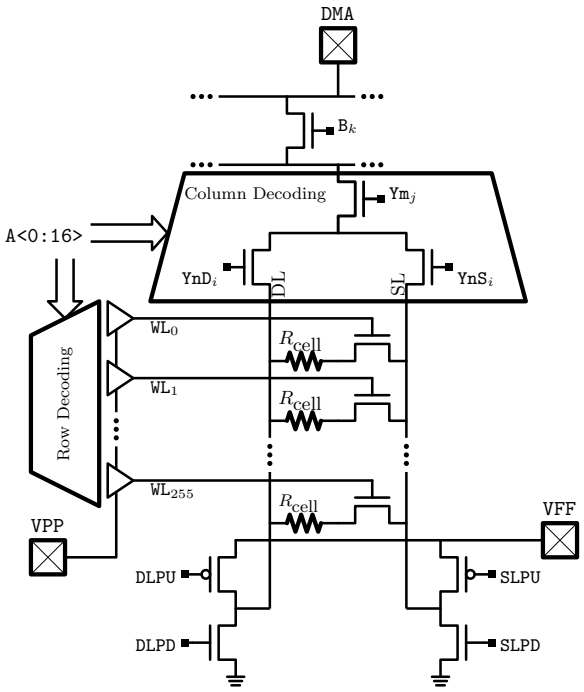


Fig. 4. DMA architecture

IV. DMA Architecture

In the infant phase of the technology it is necessary to study key parameters (initial current, forming/set/reset voltages, endurance, reliability, etc.) and their inter-cell and intra-cell variability. Thus, in addition to the normal functions it is necessary to provide a direct memory access (DMA). This is done with the scheme of the architecture shown in Fig. 4; the device used extra dedicated pins (DMA, VFF and VPP) through which the test equipment can connect and drive all the terminals of each RRAM cell.

The row decoder outputs are buffered by level shifters driven by an external supply voltage using the pin VPP. This allows to understand the effects of high voltage applied to the gate of the selector transistor, and define the optimal value. Similarly, with pin VFF it is possible to apply a variable voltage to either the source-line or the drain line for characterizing and measuring the forming/set/reset steps. The selection of the target cell is implemented by a nMOS two-stage column decoder (signals B_k address the array, while signals Ym_j and YnD_i/YnS_i address the desired column); set/reset voltages are applied through pMOS transistors, enabled by the control logic.

V. Sensing Architecture

The logical state is stored in the cell as resistance value. The reading operation may basically consist in measuring the current flowing through these resistors when a fixed voltage is applied across them. The method is straightforward but, practical issues make the reading process problematic. First, the ratio of the resistance in the two conditions is relatively low; reading means sensing very small difference of currents.

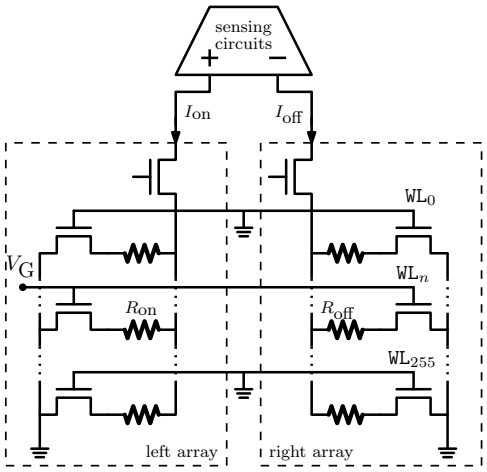


Fig. 5. Differential sensing

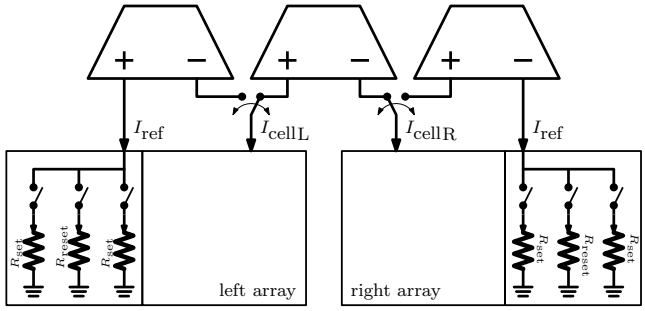


Fig. 6. Use of different sense amplifiers for reading and verify

In addition, the fixed voltage used must be low for a minimum electrical stress of the cell (≈0.2V). Furthermore, since the technology is at an infant stage, the inter-cell and infra-cell variability is significant [5]; consequently, the real current difference that has to be sensed is much lower than the nominal value. The use of a differential approach for the current sensing attenuates the limits. The sense is done with the signal of the two complementary memory arrays as a conceptual indicated in the scheme of Fig. 5. The block is a trans-conductance amplifier described in details shortly.

The writing processes requires a successive reading operations to verify the writing correctness. For this it is necessary to compare the value of the set resistance with comparison with an internal reference. Because of this the circuit must use two more sense amplifiers, as shown in Fig. 6. The reference value is given by a set of poly resistors, conveniently selected in order to control the forming, set and reset.

A. Sense Amplifier

The current to voltage conversion is problematic because of the small value of the current. Instead than using a conventional transconductance amplifier it can be convenient to directly integrate the current over a capacitor. Two current mirrors sense the current flowing through the memory cells and inject a replica (amplified by α) into two capacitors initially discharged; the voltages constantly increase in time

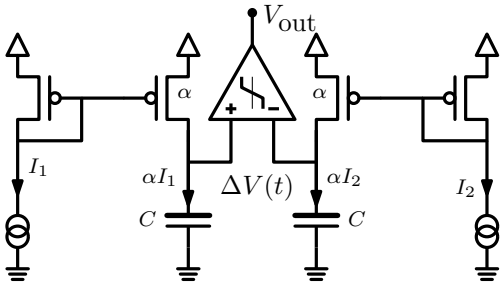


Fig. 7. Sense amplifier

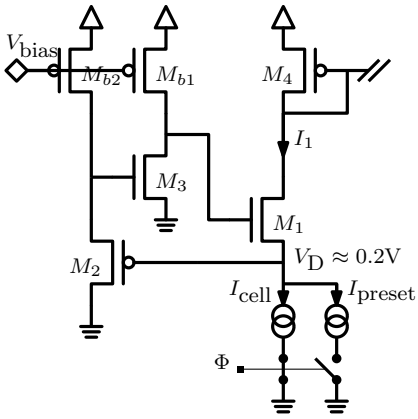


Fig. 8. Voltage regulator

and, as the schematic in Fig. 7 shows, their difference is the input of the comparator

$$\Delta V(t) = \frac{\alpha}{C}(I_1 - I_2)t \tag{1}$$

The use of redundancy makes the current difference $|\Delta I| = |I_{\text{on}} - I_{\text{off}}|$ twice the current difference sensed in a traditional circuit $|\Delta I'| = |I_{\text{on,off}} - \hat{I}|$, with $\hat{I} = \frac{I_{\text{on}} + I_{\text{off}}}{2}$. However, the use of capacitor is error prone because of possible radiations hitting the structure. The issue is relevant for the choice of the capacitances values. Small capacitances obtain a large gain in short integration times. Large capacitances are less sensitive to burst of charge generated by radiation. The trade-off is carefully studied for achieving a suitable reliability of the device and a relative degradation of the access time.

The comparator is just a gain stage without latch. The positive feedback granted by the latch, even if advantageous for the speed, may determine a soft error that, once evaluated, would be impossible to recover during the reading phase.

B. Voltage Regulator

The last block of the architecture is the voltage regulator. It is used during the evaluation phase to keep the drain voltage applied to the resistive cell around 0.2V. Since it is not critical it can be the simple voltage regulator shown in Fig. 8. The voltage V_{D} is up-shifted by transistor M_2 and applied to transistor M_3; hence, the common source stage together with the source follower provide a negative feedback to regulate the node. The transistor M_1 also behaves as a current follower and it starts to work as soon as the feedback loop turns on, taking some time; for this reason, in order to suppress this delay, when no cell is selected yet, a preset current, close to the average cell current value, is provided to the loop some time in advance.

TABLE I
RRAM FEATURES

Device Size	Technology	Supply Voltage (pads/core)	Dimension (cell/die)	Access Time
1Mbit	0.25μm	3.3V/2.5V	16.31μm^2/64mm^2	15ns

VI. CONCLUSIONS

Rad-Hard non-volatile memories are more and more necessary for space applications. The request of high reliability direct the study toward emerging technologies that realize resistive-based memory cells. Since the design phase must proceed in parallel with the technology development special design strategies must be used. This paper presented a design of a rad-hard non-volatile memory whose main features are reported in Tab. I; various aspects of the design flow were analyzed and a useful direction for the design phase was provided.

REFERENCES

[1] Laura M. Grupp, John D. Davis, Steven Swanson, *The Bleak Future of NAND Flash Memory*, 10th USENIX Conference on File and Storage Technologies, 2015.

[2] Sung-Kye Park , *Technology Scaling Challenge and Future Prospects of DRAM and NAND Flash Memory*, Memory Workshop (IMW), 2015 IEEE International.

[3] D. Chen, H. Kim, A. Phan, E. Wilcox, K. LaBel, S. Buchner, A. Khachatrian, N. Roche, *Single-Event Effect Performance of a Commercial Embedded ReRAM*, IEEE Transactions On Nuclear Science, VOL. 61, NO. 6, 2014.

[4] K. Higuchi et al., *Investigation of Verify-Programming Methods to Achieve 10 Million Cycles for 50nm HfO_2 ReRAM*, 4th IEEE International Memory Workshop (IMW), pp. 1-4, 2012.

[5] Alessandro Grossi, Damian Walczyk, Member, IEEE, Cristian Zambelli, Member, IEEE, Enrique Miranda, Senior Member, IEEE, Piero Olivo, Valeriy Stikanov, Alessandro Feriani, Jordi Su, Fellow, IEEE, Gunter Schoof, Rolf Kraemer, Bernd Tillack, Alexander Fox, Thomas Schroeder, Christian Wenger, and Christian Walczyk, *Impact of Intercell and Intracell Variability on Forming and Switching Parameters in RRAM Arrays*, IEEE Transaction on Electron Devices, vol. 62, no. 8, August 2015.

[6] S.-S. Sheu et al., *A 4Mb Embedded SLC Resistive-RAM Macro with 7.2 ns Read-Write Random-Access Time and 160 ns MLC-Access Capability*, in Proc. ISSCC, pp. 200202, Feb. 2011.

[7] Tz-Yi Liu et al., *A 130.7mm2 2-Layer 32Gb ReRAM Memory Device in 24nm Technology*, in Proc. ISSCC, pp. 210212, Feb. 2013.

[8] Arbat, A. RedCat Devices srl Co., Milan, Italy, Calligaro, C.; Roizin, Y.; Nahmad, D., *Radiation Hardened 2Mbit SRAM in 180nm CMOS Technology*, 2012 IEEE First AESS European Conference on Satellite Telecommunications (ESTEL).

[9] Alberto Stabile and Valentino Liberali, Department of Information Technologies, University of Milano, Cristiano Calligaro, RedCat Devices, *Design of a Rad-Hard Library of Digital Cells for Space Applications*, 15th IEEE International Conference on Electronics, Circuits and Systems, 2008. ICECS 2008.