

INNOVATIONS  
FOR HIGH PERFORMANCE MICROELECTRONICS



# **SiGe BiCMOS Technologies with RF and Photonic Modules**

Multi Project and Low Volume Wafer Production

# About Us

**Leibniz IHP** is a German R&D institution, focused on wireless and broadband communication.

Core competencies are:

- Mixed signal process technology
- RF & digital circuit design
- Communication system design

IHP is running an 8" pilot line housed in a 1,500 square meter class-3 cleanroom.

Several 0.25  $\mu\text{m}$  and 0.13  $\mu\text{m}$  SiGe:C BiCMOS technologies are available.

**IHP Solutions GmbH** is a 100% subsidiary of IHP. IHP Solutions was founded to focus on and grow the transfer of research results (technology transfer) of IHP research activities as well as the commercial partner for value added services along the value chain of IC manufacturing. In the context of IHP's service offerings IHP Solutions is responsible for commercial IC production.



About Us

## Low-Volume & MPW Service

IHP offers research partners and customers access to its powerful SiGe:C BiCMOS technologies and special integrated RF modules.

These technologies are especially suited for applications in the higher GHz bands (e.g. for wireless, broadband, radar).

They provide integrated HBTs with cut-off frequencies of up to 500 GHz including complementary devices.

- For products in fiber optics, aerospace, broadband and wireless communication, radar, data centers, measurement equipment, THz imaging, e-health
- 8" wafer fab for research and production in Germany
- Reliable service since 2001
- SiGe BiCMOS with state-of-the-art 500 GHz HBTs



Measurement  
equipment



Space applications



Radars



Wireless  
communication

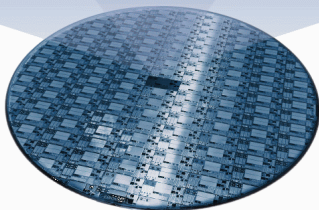


Fiber-optic communication

**Your  
specific  
application**



Data centers



## SiGe:C BiCMOS Technologies for MPW & Prototyping

- SG25H3      A 0.25  $\mu\text{m}$  technology with a set of npn-HBTs ranging from a higher RF performance ( $f_T/f_{\text{max}} = 110/180$  GHz) to higher breakdown voltages up to 7 V.
- SGB25V      A cost-effective technology with a set of npn-HBTs up to a breakdown voltage of 7 V.
- SG13S      A high-performance 0.13  $\mu\text{m}$  BiCMOS with npn-HBTs up to  $f_T/f_{\text{max}} = 250/340$  GHz, with 3.3 V I/O CMOS and 1.2 V logic CMOS.
- SG13G2      A 0.13  $\mu\text{m}$  BiCMOS technology with higher bipolar performance of  $f_T/f_{\text{max}} = 300/500$  GHz.
- SG25H5\_EPIC      A monolithic photonic BiCMOS technology combining 0.25  $\mu\text{m}$  CMOS, high-performance npn HBT's ( $f_T/f_{\text{max}} = 220/290$  GHz), and full photonic device set for C/O-band.

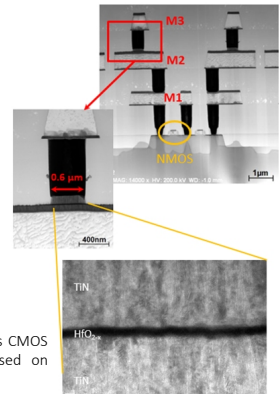
The backend for 0.13  $\mu\text{m}$  process offers 5 thin and 2 thick metal layers (TM1: 2  $\mu\text{m}$  TM2: 3  $\mu\text{m}$ ).

The schedule for MPW & Prototyping runs is located at [www.ihp-microelectronics.com](http://www.ihp-microelectronics.com).

Cadence-based mixed signal Design Kit is available. For high frequency designs an analog Design Kit in ADS can be used. IHP's reusable blocks and IPs for wireless and broadband are offered to support your designs.

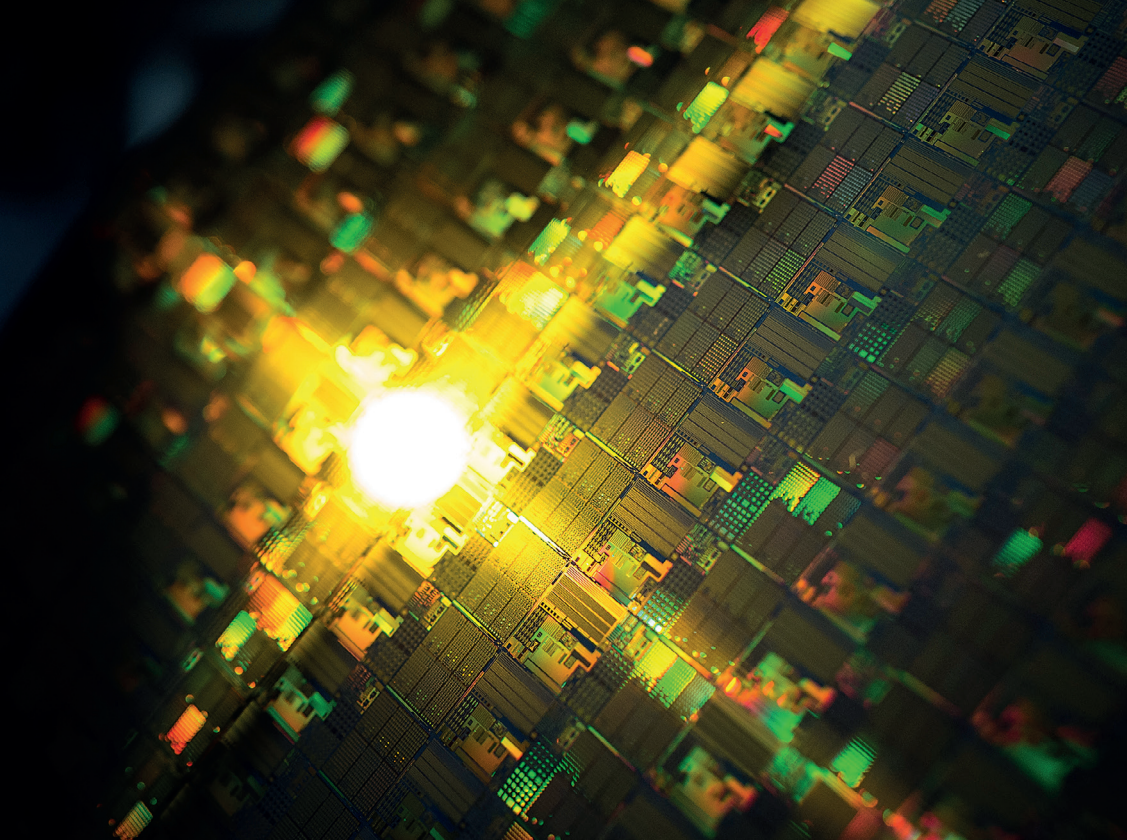
# The Following Modules are Available

- PIC Additional photonic design layers together with BiCMOS BEOL layers on SOI wafers.
- LBE The Localized Backside Etching module is offered to remove silicon locally to improve passive performance (available in all technologies).
- TSV Module is an additional option in SG13S and SG13G2 technology which offers RF grounding by vias through silicon to improve RF performance.
- MEMRES A fully CMOS integrated memristive module based on resistive TiN /  $\text{HfO}_{2-x}$  / TiN switching devices in SG13S technology. Process Design Kit including layout and VerilogA simulation model is also available.



High resolution micrographs, illustrating IHP's CMOS integrated MEMRES module, which is based on resistive TiN /  $\text{HfO}_{2-x}$  / TiN switching devices





Available Modules

## Key Specification

Feature	SG13S	SG13G2	SG25H3	SGB25V
Technology node (nm)	130	130	250	250
$f_{\max}$ NPN (GHz)	340	500	180	95
CMOS core supply (V)	1.2, 3.3	1.2, 3.3	2.5	2.5
$C_{\text{MIM}}$ (fF/ $\mu\text{m}^2$ )	1.5	1.5	1.0	1.0
Poly Res ( $\Omega/\square$ )	250	275	210—280	210—310
High Poly Res ( $\Omega/\square$ )	1300	1360	1600	2000
BEOL	7× Al	7× Al	5× Al	5× Al
Varactor ( $C_{\max}/C_{\min}$ )	1.7	1.7	3	3
Q inductor	37*	37*	37*	37*

\*1 nH (with LBE)

# Bipolar Transistors

Feature	SG13S	SG13G2	SG25H3	SGB25V
NPN1 $f_T / f_{max}$ (GHz)	250 / 340	300 / 500	110 / 180	75 / 95
NPN2 $f_T / f_{max}$ (GHz)	45 / 165	120 / 330	45 / 140	45 / 90
NPN3 $f_T / f_{max}$ (GHz)			25 / 80	25 / 70
NPN1 $BV_{CE0}$ (V)	1.7	1.7	2.3	2.4
NPN2 $BV_{CE0}$ (V)	3.7	2.5	5	4
NPN3 $BV_{CE0}$ (V)			7	7
NPN1 $BV_{CBO}$ (V)	5	4.8	6	7
NPN2 $BV_{CBO}$ (V)	15	8.5	10.5	15
NPN3 $BV_{CBO}$ (V)			21	20

## CMOS Section

Feature		SG25H3*	SG13S**	
Core Supply Voltage (V)		2.5	3.3	1.2
nMOS	$V_{TH}$ (V)	0.6	0.71	0.50
	$I_{OUT}^{***}$ ( $\mu A/\mu m$ )	540	280	480
	$I_{OFF}$ (pA/ $\mu m$ )	3	10	500
pMOS	$V_{TH}$ (V)	-0.6	-0.61	-0.47
	$I_{OUT}$ ( $\mu A/\mu m$ )	-230	-220	-200
	$I_{OFF}$ (pA/ $\mu m$ )	-3	-10	-500

\* Parameters for SGB25V are similar

\*\* Parameters for SG13G2 are similar

\*\*\* @  $V_G = 2.5$  V

## Passive Section

Feature	SG25H3	SGB25V	SG13S	SG13G2
MIM Capacitor (fF/ $\mu\text{m}^2$ )	1	1	1.5	1.5
N+ Poly Resistor ( $\Omega/\square$ )	210	205	-	-
P+ Poly Resistor ( $\Omega/\square$ )	280	310	250	260
High Poly Resistor ( $\Omega/\square$ )	1600	2000	1300	1360
Varactor $C_{\text{max}}/C_{\text{min}}$	3	3	1.7	1.7
Inductor Q @ 5 GHz	18 (1 nH)	18 (1 nH)	18 (1 nH)	18 (1 nH)
Inductor Q @ 10 GHz	20 (1 nH)	20 (1 nH)	20 (1 nH)	20 (1 nH)
Inductor Q @ 5 GHz	37 (1 nH)*	37 (1 nH)*	37 (1 nH)*	37 (1 nH)*

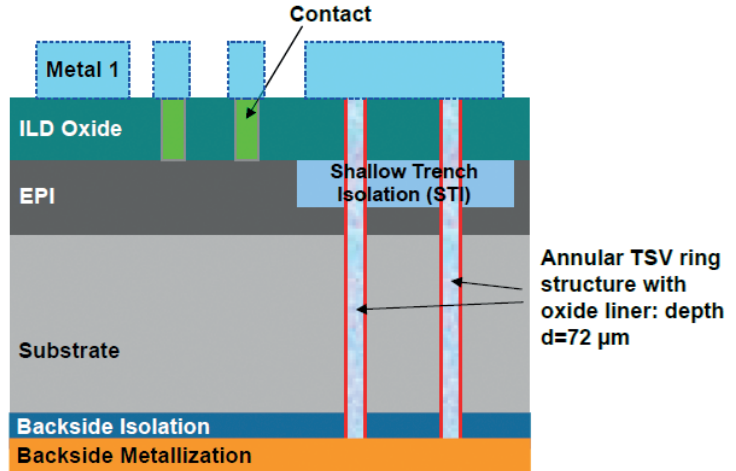
\* with LBE

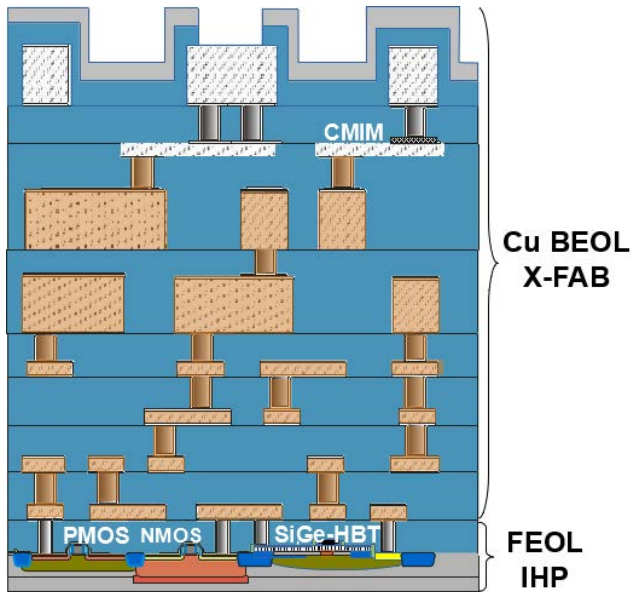
## TSV-Module

Through-Silicon Via Module for RF Grounding available in SG13 technologies.

Single TSVs can provide low GND inductance  $\approx 30$  pH to improve RF circuit performance.

A backside metallization is provided as chip-to-package interface for die attach.





SG13S/G2 FEOL



XR013 Cu BEOL



Joint foundry offer  
via  
IHP Solutions

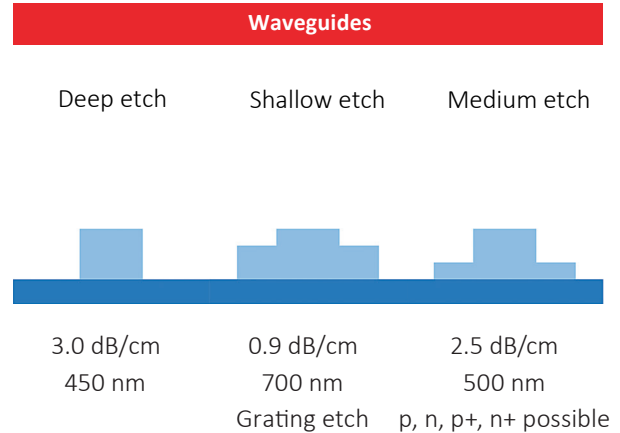
- More than 2 times higher current handling of thin metal lines
- More than 3 times higher current handling of small vias
- 40% higher area density of MIM capacitor

# Photonic Integrated Circuit Module

## Main features

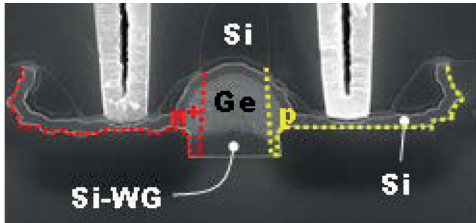
- 220 nm Si on 2  $\mu\text{m}$   $\text{SiO}_2$
- 3 etch depths
- 4 doping levels (p, n, p+, n+)
- 3 + 2 thick Al backend metal layers
- Germanium photo diodes ( $f_{3\text{dB}} > 60 \text{ GHz}$ )
- HBT's ( $f_T/f_{\text{max}} = 220/290 \text{ GHz}$ )
- Optional localized backside etching
- Complements BiCMOS in SG25H5\_EPIC

**Loss**  
**Core width**  
**Features**





### Photodiode



- $f_{3dB} > 60 \text{ GHz@-2 V}$
- $R > 0.8 \text{ A/W}$
- $I_{dark} = 200 \text{ nA@-2 V, } 20^\circ\text{C}$
- lpkiss3 building block
- GDSII cell

### Phase-shifter



#### Typical values

- 7 mm in length
- $V_{\pi} L = 3.0 \text{ Vcm}$ ,  $V_{bias} = -2 \text{ V}$
- $C = 1.8 \text{ pF}$

# Design Kit

The design kits support a Cadence mixed signal platform.

## *Analog/Mixed-Signal Flow:*

- Verification
  - Cadence Assura and PVS DRC/LVS/QRC
  - Calibre DRC/LVS
  - POLYTEDA PowerDRC/LVS
- Selected PDKs offer Cadence VPS for EMIR Analysis
- Sonnet support for all design kits
- Empire support for all design kits
- ADS support via Golden Gate/RFIC dynamic link to Cadence available
- Standalone ADS Kit including Momentum substrate layer file
- EMX stack for SG13 technology with aluminium backend

## *Digital Design Flow:*

- Digital CMOS libraries and IO cells for 0.25  $\mu\text{m}$  CMOS and 0.13  $\mu\text{m}$  CMOS are available: Behavioral Models (Verilog), Timing Files (LIB) and Abstracts (LEF)

- Simulation: ModelSim (Mentor Graphics), Incisive Enterprise Simulator IES (Cadence)
- Logic Synthesis: Design Compiler (Synopsys), RTL Compiler (Cadence)
- Formal Verification: Formality (Synopsys)
- Scan Insertion and Test Pattern Generation: DFT Compiler/TetraMax (Synopsys)
- Place & Route: Encounter Digital Implementation System (Cadence)
- OA views of digital libraries are available for mixed-signal flow
- Power Analysis: PrimeTime with PrimePower Option (Synopsys)
- Static Timing Analysis: PrimeTime (Synopsys)

Models	SG25H3	SGB25V	SG25H5 EPIC	SG13S	SG13G2
PSP	x	x	x	x	x
MOSVAR				x	x
HSIM		x		x	x
VBIC/HICUM	x	x	x	x	x

EM simulations	SG25H3	SGB25V	SG25H5 EPIC	SG13S	SG13G2
Keysight momentum	x	x		x	x
Sonnet	x	x		x	x

Design platforms	SG25H3	SGB25V	SG25H5 EPIC	SG13S	SG13G2
Cadence Virtuoso & Virtuoso XL	x	x	x	x	x
Cadence Spectre & Spectre RF	x	x	x	x	x
Cadence Assura DRC/LVS/QRC	x	x	x	x	x
Cadence VPS & Voltus FI	x	x		x	x
Keysight ADS	x	x	x	x	x
Mentor Calibre DRC/LVS				x	x
Polytada Power DRC/LVS			x	x	x
TexEDA RFIC Studio	x	x	x	x	x
NI AWR Design Environment	x			x	x
IPKISS3			x		



Leibniz Institute  
for high  
performance  
microelectronics

## Contact

Dr. René Scholz  
Phone: +49 335 5625 647  
Email: [scholz@ihp-microelectronics.com](mailto:scholz@ihp-microelectronics.com)  
Website: [www.ihp-microelectronics.com](http://www.ihp-microelectronics.com)

## Address

Im Technologiepark 25  
5236 Frankfurt (Oder)  
Germany



## Contact

Dr. Juliane Berghold  
Phone: +49 335 5625 800  
Email: [juliane.berghold@ihp-solutions.com](mailto:juliane.berghold@ihp-solutions.com)  
Website: <https://www.ihp-solutions.com>

## Address

Im Technologiepark 7  
5236 Frankfurt (Oder)  
Germany

## Our Representatives

**Europpractice** Thomas Drischel [virtual-asic@iis.fraunhofer.de](mailto:virtual-asic@iis.fraunhofer.de)

**France** Fabio Coccetti [coccetti@rfmicrotech.com](mailto:coccetti@rfmicrotech.com)

**Italy** Claudio Marziali [info@alfamicroonde.it](mailto:info@alfamicroonde.it)

**China/Asia** Dr. Yaoming Sun [y.sun@hk-microsystem.com](mailto:y.sun@hk-microsystem.com)

**Russia** Radiant-EC JSC [foundry@ranet.ru](mailto:foundry@ranet.ru)

**Americas, Japan** Volker Blaschke [volker.blaschke@siliconrfsynergy.com](mailto:volker.blaschke@siliconrfsynergy.com)

