SG25H5EPIC – Demonstrators



Monolithic integrated 40 GHz silicon modulator with driver in SG25H5EPIC SiGe:C BiCMOS technology.



Monolithic integrated high-speed coherent receiver.



Back-to-back constellation diagram at 64 GBd.



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Leibniz Institute for high performance microelectronics

IHP Photonic Technologies

Take advantage of IHP's innovative photonic technologies



Photonic Integrated Circuit Technology – SG25PIC

IHP develops photonic integrated circuit (PIC) technology offering passive photonic components, modulators and photodetectors to provide early opportunities for realizing photonic integrated designs.

The technology is compatible with fully integrated photonic BiCMOS allowing the re-use of SG25PIC designs in IHP electronic-photonic integrated circuits in SG25H5EPIC.

Passive Waveguide Features

- Dual-etch passive nano-waveguide technology
- 220 nm SOI
- Oxide cladding



SEM image of a grating coupler

Electronic Photonic IC Technology-SG25H5EPIC



Waveguide-coupled Ge PIN photodiode

The monolithic integration of photonic devices, such as detectors and modulators in the frontend of a Sibased integrated circuit technology, allows shortest possible interconnects between photonics and electronics from which high-speed performance of electronic-photonic integrated circuits (EPIC) greatly benefit.

SG25H5EPIC Photonic BiCMOS process features:

- High performance silicon photonics
- High performance BiCMOS electronics

0.25µm BiCMOS core				
SiGe HBT	f _{max}	f _τ		BV _{CEO}
SG25H5	290 GHz	240 GHz		1.9 V
Photonic components				
Ge-PIN-PD	I _{dark} (@-2V)	Responsivity (@-2V, 1550 nm)		3dB Bandwidth (@-2V)
	<200 nA	>0	.8 A/W	>60 GHz
p-n phase shifter	V _π L (@-1V)		Loss (@-1V)	
	2.7 V⋅cm		1.2 dB/mm	
Grating Coupler	Optical Loss (@ 1550 nm)			
	4 dB			
Waveguides	Nano-WG: 3.0 dB/cm		Rib-WG: < 0.9 dB/cm	
Back-End-Of-Line: 5 layers AlCu with 2 and 3µm thick top level metal				

Process Design Kit features:

- Luceda IPKISS support for photonic designs (including simulation using Caphe)
- Cadence support for electronic-photonic circuit design (DRC, LVS, QRC)



TEM X-section of the photonic BiCMOS process: WG-coupled Ge-PIN diode (1st generation) on SOI and SiGe HBT fabricated in an adjacent bulk region.