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09.10.2019

How to Improve the Security of IoT Devices
IHP scientist Yauhen Varabei received Best Paper Award

Frankfurt (Oder). With the advent of the Internet of things security and more recently artificial intelligence became hot research topics of utmost societal importance. IHP scientist Yauhen Varabei and his colleagues are combining these two fields in order to improve the security of IoT devices. In their paper entitled "Intelligent Clustering as a Means to Improve K-Means Based Horizontal Attacks" they are reporting on their improvements when it comes to applying AI means to identify weaknesses of cryptographic implementations. "We see a lot of potential applications of our new approach in the field of security," says Yauhen Varabei. This highly innovative approach got a lot of attention and a best paper award at the Workshop on Machine Learning for Security and Cryptography that was part of the "A"-rated IEEE Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC) taking place from 8th to 11th of September in Istanbul, Turkey. It is one of the two major conferences of the IEEE Communications Society (ComSoc) in the field of wireless communications and networking. PIMRC was founded in 1989 as a workshop in London and developed over the years to become a major international conference attracting the technical community from all regions and continents.

IHP scientist Yauhen Varabei (r.) received the Best Paper Award at the 1st International Workshop on Machine Learning for Security and Cryptography from Workshop organisator Dr. Pelin Angin (l.). © Privat

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The IHP is an institute of the Leibniz Association and conducts research and development of silicon-based systems and ultrahigh frequency circuits and technologies including new materials. It develops innovative solutions for application areas such as wireless and broadband communication, security, medical technology, industry 4.0, automotive industry, and aerospace. The IHP employs approximately 300 people. It operates a pilot line for technological developments and the preparation of high-speed circuits with 0.13/0.25 μm BiCMOS technologies, located in a 1000 m² class 1 cleanroom.

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