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High Gain Graphene Based Hot Electron Transistor with Record High Saturated Output Current Density

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Hot electron transistors (HETs) represent an exciting new device for integration into semiconductor technology, holding the promise of high-frequency electronics beyond the limits of SiGe bipolar hetero transistors. With the exploration of 2D materials such as graphene and new device architectures, hot electron transistors have the potential to revolutionize the landscape of modern electronics. This study highlights a novel hot electron transistor structure with a record output current density of 800 A cm^{-2} and a high current gain α, fabricated using a scalable fabrication approach. The hot electron transistor structure comprises 2D hexagonal boron nitride and graphene layers wet transferred to a germanium substrate. The combination of these materials results in exceptional performance, particularly in terms of the highly saturated output current density. The scalable fabrication scheme used to produce the hot electron transistor opens up opportunities for large-scale manufacturing. This breakthrough in hot electron transistor technology holds promise for advanced electronic applications, offering high current capabilities in a practical and manufacturable device.

1. Introduction

The terahertz gap refers to a region of the electromagnetic spectrum between the frequencies of the microwave range and infrared radiation. It extends roughly over the frequency range from 0.1 to 10 THz. The terahertz gap has historically been considered difficult to explore as there are both technical and physical challenges to generating, capturing, and exploiting terahertz radiation. However, terahertz radiation has the potential to enable a variety of applications in communications, imaging, spectroscopy, and security. Terahertz radiation can be used in medicine, for example, for noninvasive diagnostics of tissue samples or for screening objects for security checks.[1,2] Traditional electronic devices such as transistors have difficulty processing signals in the THz range. Classic transistors such as the high electron mobility transistors (HEMTs), the metal–oxide–semiconductor field-effect transistors (MOSFETs), and the bipolar junction transistors (BJTs) have so far covered the lower end of the terahertz range.[3–5] Maximum cutoff frequencies f_T of around 700 GHz have been reported for HEMTs[3] and BJTs,[5] while the MOSFET is still a bit behind with f_T = 400 GHz.[4] Thereby, lateral devices like the MOSFET and HEMT are subject to intrinsic limitations such as gate lithography, short channel effects, and velocity saturation. On the other hand, vertical BJTs require a certain minimum base thickness to reduce lateral base resistance. Thus, the cutoff frequency of BJTs is ultimately limited by the base transit time of electrons traveling perpendicular to the junction planes from the emitter toward the collector.[6] An alternative high-speed transistor technology is the hot electron transistor (HET). It is designed to take advantage of the kinetic energy of hot electrons, which are electrons with higher energy levels than the equilibrium thermal energy. The HET is also a vertical device but unipolar in nature with tunneling[7,8] or Schottky barriers[9,10] instead of pn-junctions like in a BJT. Cutoff frequencies larger than 10 THz have been predicted for HETs with the integration of 2D materials.[11] The first HET was proposed in 1960 by Mead with a metal/insulator/metal/insulator/metal (MIMIM) structure.[12] Thereby, the first metal electrode corresponds to the emitter (E), the second to the base (B), and the third to the collector (C). In the ON state, the BE voltage is able to modulate the

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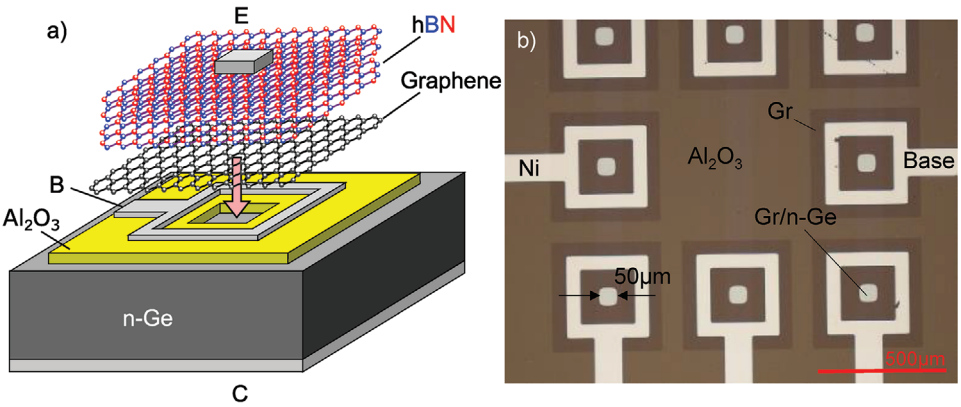

Figure 1. a) 3D representation of the hot electron transistor with a multilayer hexagonal boron nitride (hBN) emitter-base (E/B) insulator, a monolayer graphene base (B), and an n-Ge collector (C) semiconductor. b) Top view of the hot electron transistor after lithography and subsequent wet transfer of hBN.

collector current I_C when a fixed B/C voltage is applied. However, these early metal-based HETs had the disadvantage that the base thickness could not be scaled down sufficiently. This led to scattering events in the metal base, preventing the device from realizing its full potential. The situation changed with the advent of 2D materials such as graphene (Gr).[13] Now, the metal base of the HET could be replaced by monolayer thin graphene, and ultrashort base transit times, which is key for high-frequency HETs, could be realized. Only recently, a 2D-based HET with a very good common-base current gain α of 0.99 and a high output current density of 400 A cm^{-2} was demonstrated.[14] This was realized with a hBN/graphene/WSe_2 structure. All 2D materials were exfoliated by a conventional scotch tape exfoliation technique and transferred by micromanipulators using a polycarbonate/polydimethylsiloxane stack. The disadvantage of this approach is the limited scalability and also the output current of this HET is saturated only in a very limited V_{CB} window. In this study, we present the results of an improved hexagonal boron nitride (hBN)/graphene/n-Ge HET which was fabricated by much more scalable wet-transfer techniques and standard optical lithography. Record high output current densities of around 800 A cm^{-2} were achieved while the output current is saturated in a much wider V_{CB} window. Thereby, the current gain remains high showing values of α up to 0.87. The increased output current can be explained by reducing the hBN thickness and by utilizing a reduced B/C Schottky barrier between graphene and n-germanium. This study represents an important step towards realizing scalable 2D-based high-frequency HETs.

2. Results and Discussion

2.1. Hot Electron Transistor Design

A 3D representation of the HET is shown in **Figure 1**a. The n-type germanium collector is covered with a 60 nm thick Al_2O_3 layer that isolates the square-shaped base metallization of Ti/Ni from the Ge substrate. An area of 50 × 50 µm^2 is exempt from Al_2O_3 and thus constitutes the active device area. A monolayer graphene sheet is transferred on top of the base metallization and the active device area. Finally, a multilayer hexagonal boron nitride covers the graphene and an emitter contact of Ti/Ni is placed on top. A top view of the real device after the wet transfer of graphene and hBN is shown in Figure 1b. While transferred graphene is patterned into isolated flakes of approximately 350 × 350 µm^2 by oxygen plasma, hBN can remain in the transferred form since it is laterally isolating anyway (see Figure S1, Supporting Information). During the electrical characterization of the HETs, the probe tips easily pierce through the thin hBN to make good electrical contact. The exposed active device areas can be clearly seen in the middle of the square-shaped metal electrodes. Thus, 4, 8, and 12 nm thick hBN layers were used as E/B tunnel barriers to fabricate and characterize eight individual devices. A simplified band scheme of the HET is illustrated in **Figure 2**. Thereby, the equilibrium state is shown in Figure 2a. Between the emitter and the base of the HET, the hBN layer represents the E/B insulator and there is a tunnel barrier having a height $q\varphi_{EB}$.

On the other side of the device, a B/C Schottky barrier $q\varphi_{BC}$ between graphene and n-Ge serves as a filter barrier for cold electrons. When the device is in the OFF state (Figure 2b), only a few carriers from the emitter can pass through the E/B tunneling barrier and most of these carriers are then reflected at the B/C filter barrier.

Thus, only a minor fraction of cold electrons from the base can overcome the filter barrier $q\varphi_{BC}$ and contribute to the collector current I_C. In this situation, the carriers are propelled by the reverse-biased B/C junction. In the ON state (Figure 2c), the emitter is negatively biased by $V_{BE,}$ and the tunneling barrier becomes narrower. Now, most of the electrons injected from the emitter tunnel through the E/B barrier and gain energy to become hot carriers in the base. If V_{BE} is larger than φ_{BC}/q, the hot electrons are able to surpass the B/C Schottky barrier and contribute to the collector current I_C. Note that there is another effect that must be considered in the ON-state. When the emitter is negatively biased, this leads to the field-induced accumulation of holes in graphene.[15] Thus, the Fermi energy level in graphene decreases while the B/C Schottky barrier increases. This makes the filter barrier more effective since cold electrons from the base are now reflected even more strongly at this barrier. This could also

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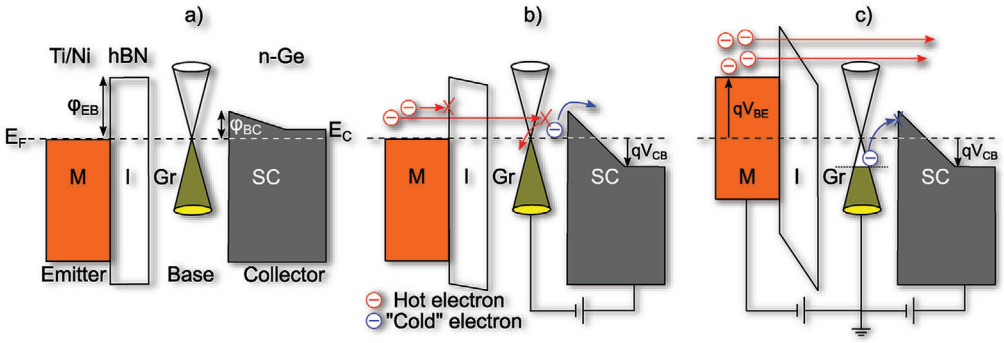

Figure 2. Simplified band scheme of the metal (M), insulator (I), graphene (Gr), semiconductor (SC) hot electron transistor in a) thermal equilibrium, b) OFF-state, and c) ON-state.

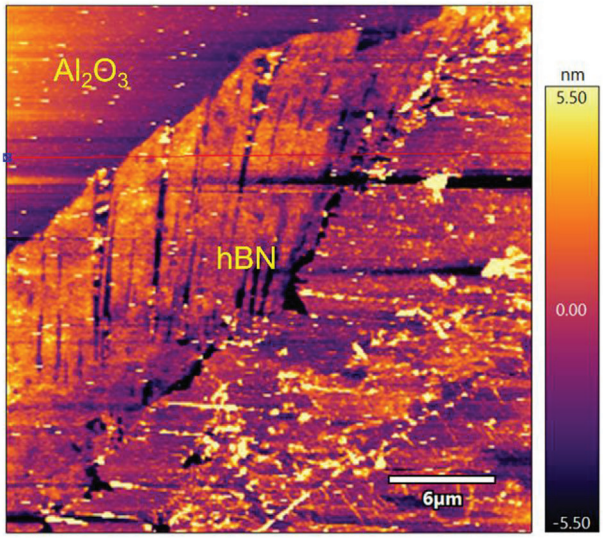

Figure 3. AFM image of wet transferred hexagonal boron nitride (hBN) on aluminum oxide (Al_2O_3).

increase the current gain of the device because in this situation the reflection factor at the collector interface decreases.[16] On the other hand, the thick lightly doped n-Ge substrate should effectively shield the graphene Fermi energy level from being raised with V_{CB}. In addition, an AFM image of hBN on Al_2O_3 is represented in **Figure 3**. It is obvious, that the thickness of the multilayer hBN flake is below 5 nm. Multiple line scans were performed (see Figure S2, Supporting Information) that further specify hBN thickness, deriving values of 4 ± 0.5 nm. Thus, approximately 12 monolayers of hBN have been transferred. Several localized elevations can be observed on the hBN flake which can be attributed to PMMA residues from the hBN wet transfer. Cracks at the fringe of the hBN flake can also be observed. However, in the middle of the hBN flake, where the active devices are located, the hBN is uniform and mostly free of cracks (see Figure S3, Supporting Information). Thus, we expect the device performance is not much influenced by cracks or pinholes in hBN. In this work, several devices each containing 4, 8, and 12 nm hBN were fabricated by multiple sequenced hBN transfers.

2.2. Electrical HET Characterization

Figure 4 shows the two-terminal IV characteristics of the graphene/n-Ge B/C-diode. A good rectification with on-off ratios of 5×10^3 ($\pm 2 \times 10^3$) at ± 5 V could be realized. From IV–T characterizations, the Schottky barrier height $q\varphi_{BC}$ of this junction was determined to be 0.32 eV (± 0.05 eV).[17] Note that this barrier height is much lower than the WSe_2-based B/C barrier of 0.6 eV reported in Ref.[14>17] The forward current of the Gr/n-Ge diode is up to 4×10^3 A cm^{-2} and already reaches the measurement limit at large forward voltages.

The common-base output characteristics of the hot electron transistor with germanium, graphene, and one multilayer hBN (4 nm) E/B insulator are shown in **Figure 5**a). Thereby, the emitter voltage V_E is chosen as the parameter.

This device represents an average device whose parameters approximately resemble the mean values. As can be seen, the collector current I_C strongly scales with the emitter voltage V_E. Thereby, the collector current is highly saturated in a large V_{CB} window. Note that I_C shows some elevations for $V_{CB} < 0$ V and

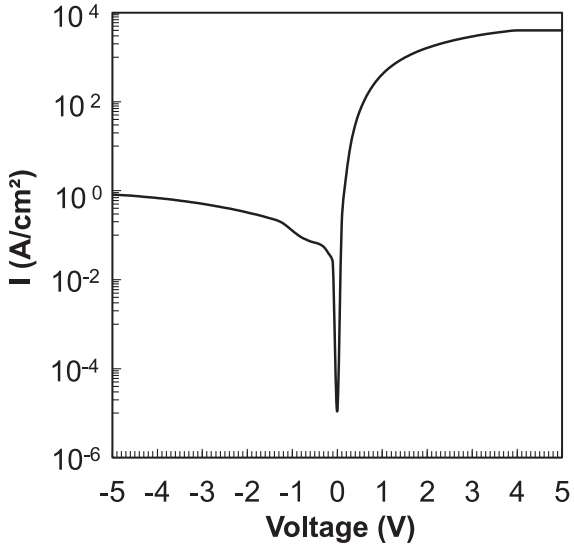

Figure 4. IV characteristics of the base-collector Schottky diode representing the graphene/n-Ge junction.

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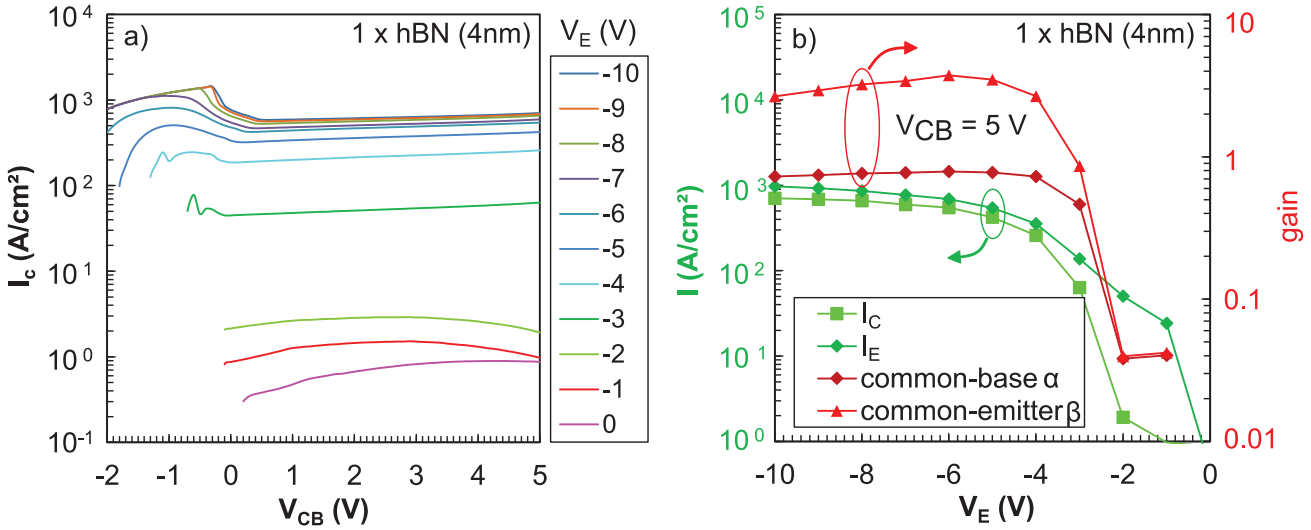

Figure 5. a) Common-base output characteristics of the hBN/ Gr/ n-Ge hot electron transistor with the emitter voltage as a parameter. b) Emitter current, collector current, and gain of the hot electron transistor as a function of the emitter voltage.

large V_E. Although not yet fully understood, we speculate that this can be attributed to automatic changes in the measurement range when the current changes from a high slope ($V_{CB} < 0$) to saturation with a low slope ($V_{CB} > 0$ V). It must be also noted that the emitter current I_E already reaches the limit of our measurement setup (0.1 A) for $V_{CB} < 0$ V, which could again affect the quality of the I_C measurement. We therefore decided to extract device parameters such as I_{Cmax} or α_{max} (see **Table 1**) only in the saturation range at $V_{CB} = 5$ V, where both I_C and I_E are explicitly below the compliance limit.

In Figure 5b the individual device currents and gains are represented. It can be seen that the collector and emitter currents increase simultaneously with the emitter voltage. The common-base current gain α, defined as the ratio of I_C to I_E, for this particular device, reaches values close to unity. Further, the common-emitter current gain β can be calculated according to $\beta = \alpha/(1-\alpha)$.

Table 1. Statistics of eight individual hBN–Gr–Ge HET devices for each hBN thickness with 4, 8, and 12 nm hBN respectively. Denoted are the average values (avg.) and ± deviations for the device parameters on-off ratio ($V_{CB} = 3$ V), maximum common-base current gain α_{max}, maximum common-emitter current gain β_{max}, and maximum current density I_{Cmax} (the latter three parameters evaluated each at $V_{CB} = 5$ V).

		On–off	α_{max}	β_{max}	I_{Cmax}
		$V_{CB} = 3$ V	(I_C/I_E)	$\alpha/(1-\alpha)$	[A cm^{-2}]
HET 1 (4 nm hBN)	avg.	1088	0.73	3.27	589
	±	606	0.14	3.56	216
HET 2 (8 nm hBN)	avg.	1379	0.77	3.52	322
	±	827	0.06	1.35	108
HET 3 (12 nm hBN)	avg.	811	0.77	3.49	246
	±	323	0.16	1.93	156

Current gains β larger than unity are achieved for emitter voltages of more than 3 V. Thus, the hot electron device is also expected to show amplifying characteristics in the common-emitter configuration. Additional devices with two and three multilayer hBN sheets, corresponding to around 8 and 12 nm hBN thickness, were also fabricated and characterized (see Figures S4 and S5, Supporting Information). The most distinctive difference between the devices with thin hBN and thicker hBN is the decreasing maximum current density with increasing hBN thickness. This can best be observed by considering the statistics of all devices in Table 1. Regarding the on–off ratio, α_{max}, and β_{max} the devices behave quite similarly. However, the maximum current density I_{Cmax} ($V_E = -10$ V, $V_{CB} = 5$ V) strongly increases with reduced hBN thicknesses due to an increased tunneling probability. A record current density of 800 A cm^{-2} and a high α_{max} of 0.87 was achieved for a 4 nm hBN champion device.

2.3. Benchmarking of Different HET Devices

In **Table 2** selected HET devices from different reports and their performance parameters J_C and α_{max} are compared.[7,8,14,18–23] The devices are ordered by the achieved output current density J_C. Most of the HETs utilize a tunnel barrier at the emitter-base junction. Only devices number 4, 5, and 7 employ a thermionic E/B barrier. All devices covered in this summary use a monolayer thin base material, which in most cases is graphene (Gr). It can be seen, that the early devices (1, 2) suffered from low output current densities. This is due to a low-quality SiO_2 injection barrier and thick and high filtering barriers (e.g., 14 nm HfO_2, 2 eV).

For the HET number 3 with a MoS_2 base, a high current gain has been achieved but the high lateral MoS_2 base resistance so far limited the output current density. Improved thermionic (e.g., GaN/AlGaN) and double-layer tunnel barriers ($TmSiO/TiO_2$) were employed at the emitter-base junction for devices number 4–7 which resulted in much higher output current densities. However, a combination of high output current

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Table 2. Benchmarking of various experimental HET devices with E as the emitter, barrier 1 as the tunnel or thermionic barrier, B as the base, barrier 2 as the filter barrier, J_C as the output current density, α_{max} the maximum common-base current gain.

No.	Year	Structure				J_C	α_{max}	Limitations	Reference
		E	Barrier 1	B	Barrier 2	[A cm^{-2}]			
1	2013	n-Si++	SiO_2	Gr	HfO_2	9×10^{-8}	0.048	low α_{max}, low J_C	[8]
2	2013	n-Si+	SiO_2	Gr	Al_2O_3	2×10^{-5}	0.065	low α_{max}, no current saturation	[7]
3	2015	n-Si++	SiO_2	MoS_2	HfO_2	10^{-4}	0.95	low J_C, no current saturation	[19]
4	2019	Al	$SrTiO_3$	$SrRuO_3$	Nb:$SrTiO_3$	1	0.35	low α_{max}	[21]
5	2019	GaN	AlGaN	Gr	Al_2O_3	1	0.15	low α_{max}	[22]
6	2015	n-Si+	$TmSiO/TiO_2$	Gr	Si	3	0.2	low α_{max}	[18]
7	2023	Ti	n-a-Si:H	Gr	n-Si	3	0.02	low α_{max}	[20]
8	2017	GaN	AlN	Gr	WSe_2	50	0.75	no current saturation	[23]
9	2019	Gr	hBN (10 nm)	Gr	WSe_2	400	0.99	low V_{CB} window	[14]
this work		Ti	hBN (4 nm)	Gr	n-Ge	800	0.87		

density and high current gain was first achieved in 2017 with device number 8. This was realized by using an ultrathin AlN on a GaN emitter with the exploitation of a 2D electron gas (2-DEG) in the GaN side of the heterostructure. This in turn enables a very low emitter resistance. A further optimized device with increased J_C and α_{max} has been reported in 2019 (HET number 9). In this case, the whole device was fabricated by stacking 2D materials on top of each other by exfoliation and transfer techniques. This allows for atomically sharp interfaces within the device which results in record high current densities and gains. However, even for these sophisticated devices number 8 and 9, limited current saturation and a small V_{CB} window remained to be issued. In this work, high α_{max} and record high J_C have been achieved (see last row in Table 2) by our proposed structure showing a large V_{CB} operation window and current saturation.

2.4. Discussion

Tunneling junctions at the emitter-base junction possess the advantage of quasi-monoenergetic electrons with a peak distribution near the E_F of the emitter. It can be assumed, that the present device in this work favors direct tunneling through the E/B barrier for $V_E < \varphi_{EB}/q < 4$ V. **Figure 6** shows the energetic distribution of the calculated emitter-base tunneling current density through the 4 nm thick hBN E/B insulator. Details on the calculation can be found in the supporting information. The narrow quasi-monoenergetic distribution of the current around the E_F of the emitter can be clearly seen. The current density increases with the emitter-base potential V_{EB} and reaches values similar to the experimentally observed emitter currents (see Figure 5b). The transmission probability through the hBN E/B insulator is derived from the data and is between 0.05 % ($qV_{EB} = -1$ eV) and 1.1 % ($qV_{EB} = -4$ eV). For emitter voltages larger than the E/B barrier (here $q\varphi_{EB} = 4.0$ eV),[14] Fowler–Nordheim tunneling (FNT) through a reduced effective triangular barrier is expected to occur.[24] The FNT range is where our devices perform best in terms of current gain and output current. This means, that even the thinnest hBN of 4 nm is too thick to allow for efficient direct tunneling. The observed increase of the output current with decreasing hBN thickness in our devices can be easily explained by the tunneling probability T, which is inversely and exponentially proportional to the barrier height (φ) and thickness (t)[23]: $T \propto e^{\frac{1}{\varphi t}}$. Another requirement for an ideally designed HET is an E/B barrier larger than the B/C barrier ($q\varphi_{EB} > q\varphi_{BC}$) to prevent backscattering at the B/C interface. This is fulfilled for the present germanium-based HET with $q\varphi_{EB} = 4.0$ eV and $q\varphi_{BC} = 0.32$ eV.

In addition, the optimum base material must be thin enough to allow for ballistic vertical transport across the base. It should also possess a high conductivity to minimize the lateral sheet resistance and isolate the E/B and B/C barriers for good electro-

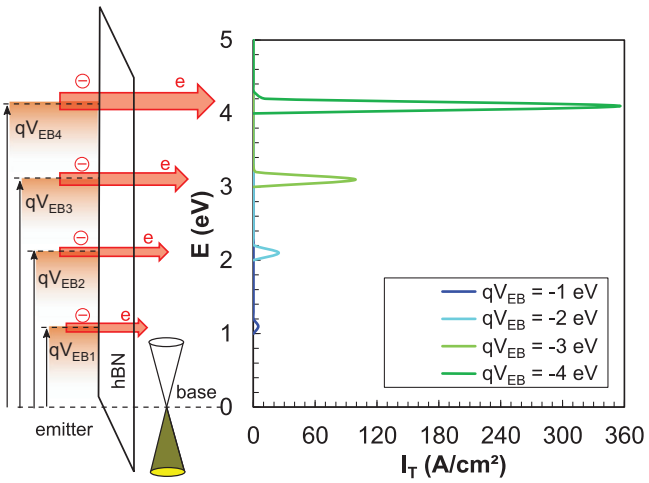

Figure 6. Energetic distribution of the calculated emitter-base tunneling current density I_T through 4 nm hBN with the parameter qV_{EB}.

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static gate control. The choice of ultrathin 2D graphene with a high mobility as in the present device is a logical consequence. It is known that graphene constitutes a Schottky junction when in contact with semiconductors such as Ge[25] or Si. [26] The difference between a Gr/semiconductor versus a metal/semiconductor junction is the tunable Fermi energy level in graphene. This has consequences for the HET, such as a prevention of the output current saturation, since the collector-base voltage also generates an electric field at the E/B junction due to the poor isolation of the tunnel and filter barriers by graphene. This might be one reason for the limited I_C saturation observed in Ref.[14] where a thin Gr-WSe_2 B/C barrier is used. In our device, the tunnel and filter barrier seem to be better isolated and the Gr/n-Ge junction exhibits high reverse blocking characteristics (avg. breakdown voltage 108 ± 13 V)[17] leading to I_C saturation. Furthermore, the B/C barrier of $q\varphi_{BC} = 0.32$ eV is high enough to prevent cold electron emission from the base to the collector, especially when considering the V_{BE}-induced increase in the B/C barrier height. Our hBN-Gr-Ge HET is not only promising for future high-speed electronics but is also based on scalable fabrication schemes that facilitate the determination of f_T by means of conventional ground-signal-ground (GSG) contacts.[27] It can also be noted that graphene transfer is a routine process in 200 mm CMOS pilot lines for the fabrication of 2D-based electronic and optoelectronic devices.[28] Moreover, the devices show record output current densities which are saturated in a wide V_{CB} window. Further improvements of the device parameters can be expected from, e.g., optimized doping of the n-Ge B/C semiconductor and improved passivation of the Ge surface. Also, lowering the E/B tunnel barrier height and reducing the barrier thickness is a viable approach to decreasing device threshold voltage and further improving device performance.

3. Conclusion

In conclusion, we have demonstrated a scalable fabrication of an hBN–Gr–Ge hot electron transistor (HET) using standard optical lithography and wet transfer approaches for 2D materials. Record high output current densities of 800 A cm^{-2} were achieved in combination with large common-base current gains α of 0.87. Thereby, J_C is highly saturated in a wide V_{CB} window. The improvements in the device parameters can be attributed to a reduced hBN thickness of only 4 nm and the utilization of a low energetic B/C barrier consisting of a thermionic Gr/n-Ge junction. These results can inspire further research on the investigation of vertical transport in devices that combine 2D layers with classic 3D bulk materials. Additional optimization strategies such as varying collector semiconductor doping level and/or surface passivation of n-Ge are envisioned to further improve the limits of this novel HET platform.

4. Experimental Section

Lightly n-doped germanium wafers with a resistivity of 1–25 Ω·cm are used as the substrate. The wafers were first cleaned in acetone with ultrasonic agitation. Then, a cleaning cycle of H_2O_2 and 5% hydrofluoric acid (HF) was applied and repeated three times. In addition, a standard RCA-1 clean and HF treatment finalized the wafer preconditioning. A Ti/Ni contact was deposited by electron beam evaporation as the backside collector metallization. Afterward, a 60 nm thick Al_2O_3 layer was deposited on top of the Ge wafer by atomic layer deposition (ALD tool from FHR GmbH). Next, lithography step 1 (positive resist AZ4562, 7 µm thickness) was performed to define the 50 × 50 μm^2 active area of the device. Therefore, the aluminum oxide was exposed locally by 5 % HF. In addition, lithography step 2 occurred to create the square-shaped Ti/Ni-base metallization of 10 and 90 nm, respectively. Next, commercially available graphene on copper with PMMA coating from Graphenea, Inc. was used to cover the base metallization, Al_2O_3, and the active area of the device. Therefore, a standard wet chemical transfer approach using ammonium persulfate etchant and PMMA removal in acetone was applied. Further, the large area transferred graphene was patterned by oxygen plasma in combination with lithography step 3. It is necessary to isolate the eight individual devices. In the next step, commercially available multilayer hexagonal boron nitride (hBN) on copper substrates from "graphene supermarket" was also transferred on top of graphene by a similar wet transfer approach as used for graphene. Thereby, eight individual devices with each one hBN transfer, two hBN transfers, and three hBN transfers were fabricated. Note that due to the wet transfer approach, a homogeneous coverage of hBN is possible even though there are steps of more than 100 nm present in the device structure. In the experience, this would be difficult with standard exfoliation and dry transfer techniques. Finally, lithography step 4 was performed to equip the hBN multilayers with a top metal emitter contact consisting of Ti/Ni again.

The structure of the devices was characterized by a high-resolution AFM from Oxford Instruments. The electrical characterization was performed using a Keithley SCS 4200 semiconductor analyzer connected to a vacuum probe station. The measurement limit of the three individual source measure units is limited to each 0.1 A.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

graphene, high current density, high current gain, high frequency, hot electron transistor, saturated

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