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Lateral Selective SiGe Growth for Local Dislocation-Free SiGe-on-Insulator Virtual Substrate Fabrication

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Dislocation free local SiGe-on-insulator (SGOI) virtual substrate is fabricated using lateral selective SiGe growth by reduced pressure chemical vapor deposition. The lateral selective SiGe growth is performed around a ∼1.25 μm square Si (001) pillar in a cavity formed by HCl vapor phase etching of Si at 850 °C from side of SiO_2/Si mesa structure on buried oxide. Smooth root mean square roughness of SiGe surface of 0.14 nm, which is determined by interface roughness between the sacrificially etched Si and the SiO_2 cap, is obtained. Uniform Ge content of ∼40% in the laterally grown SiGe is observed. In the Si pillar, tensile strain of ∼0.65% is found which could be due to thermal expansion difference between SiO_2 and Si. In the SiGe, tensile strain of ∼1.4% along ⟨010⟩ direction, which is higher compared to that along ⟨110⟩ direction, is observed. The tensile strain is induced from both [110] and [−110] directions. Threading dislocations in the SiGe are located only ∼400 nm from Si pillar and stacking faults are running towards ⟨110⟩ directions, resulting in the formation of a wide dislocation-free area in SiGe along ⟨010⟩ due to horizontal aspect ratio trapping.

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SiGe virtual substrates (VS) having low-surface roughness with fewer defects and uniform strain distribution are essential for fabricating emerging devices.[1] Various techniques to grow high crystallinity VS are reported e.g. conventional graded buffers[2,3] and reverse graded buffers.[4,5] However, there are several problems with these methods as they require several micrometer-thick buffer layers to reduce threading dislocation (TD) density (TDD), having random distribution of TD networks in the SiGe layer and develop cross-hatch patterns resulting in high surface roughness and tilt-lattice plane at the SiGe VS surface. The surface roughness can be planarized by chemical mechanical polishing, however, the random distribution of the TDs and the fluctuation of the SiGe lattice plane cannot be solved. The high SiGe VS thickness causes difficulties for local interconnections between devices on the SiGe VS and those on Si. Therefore, process development of thin SiGe VS with controlled distribution of defects are of interest.[6]

In our previous work, lateral selective Ge growth was performed in a cavity formed by selective vapor phase etching (VPE) of Si from side of mesa-patterned SiO_2/Si-on-insulator (SOI) wafer.[7] By the lateral selective growth of Ge, local dislocation-free, thin and smooth Ge-on-insulator is fabricated by horizontal aspect ratio trapping (ART) mechanism. In this work, we present lateral-selective SiGe growth to realize smooth and dislocation-free local SiGe-on oxide (SGOI) VS by lateral ART and discuss its surface morphology and distribution of strain and dislocations.

Experimental

Lateral selective SiGe growth is carried out in a reduced pressure chemical vapor deposition (RPCVD) system. SOI wafer with (001) surface orientation is used. Schematic images of the sample preparations are shown in Figs. 1a–1d. First, epitaxial Si is deposited on the SOI wafer to adjust total thickness of Si to 435 nm. Then 300 nm thick SiO_2/300 nm thick Si/buried oxide (BOX) layer stack is fabricated by wet oxidation. After that 6.3 μm square checkerboard SiO_2 mesa structures with ⟨110⟩ oriented sidewalls are fabricated by photolithography and dry etching of the SiO_2 cap and SOI (Fig. 1a). In order to prevent selectivity-loss by residual carbon contamination by the reactive ion etching, the Si surface of the checkerboard mesa structured wafer are oxidized for 10 nm and etched by HF. Furthermore, the wafer is cleaned by standard RCA cleaning followed by HF dip. Afterwards, the wafer is loaded into the RPCVD reactor and baked at 850 °C in reduced pressure H_2 to remove residual oxide on the Si surface. Thereafter, lateral HCl VPE of Si at 850 °C is performed from sidewall of the mesa to form a Si pillar and a cavity under the mesa (Fig. 1b). Around ∼2.5 μm of lateral cavity interposed between SiO_2 and BOX is formed around the Si pillar by the HCl VPE. Then, SiGe is selectively deposited in the cavity using a SiH_2Cl_2-GeH_4-HCl gas mixture at 750 °C (Fig. 1c). HCl is added for maintaining selectivity during selective SiGe epitaxy. Finally, the SiO_2 cap is removed by HF (Fig. 1d).

Atomic force microscopy (AFM) is used for measuring the surface roughness. Cross section and plan-view transmission electron microscopy (TEM) are used for characterizing the dislocations in the SiGe as well as at Si/SiGe interface. For cross section TEM, the samples are cut out by using focused ion beam (FIB) along [110] direction next to the Si pillar (as shown in the schematic image of Fig. 5a). Micro-Raman spectroscopy excited with 532 nm wavelength laser (500 ± 10 nm spot size) is used for strain distribution analysis in Si and SiGe. Energy dispersive X-ray spectroscopy (EDX) is used for Ge concentration measurement in the laterally grown SiGe. It is to be noted that there is a small background noise of Si existing in the EDX analysis because of presence of Si in the EDX detector. The EDX specimen used for Fig. 3 is same TEM lamella as used for Fig. 5. Electron Nano-beam diffraction (NBD) are used for measuring strain distribution in the laterally grown SiGe.

Results and Discussion

Figure 2a shows an angle-view scanning electron microscopy image of laterally grown selective SiGe around Si pillar after top SiO_2 removal by HF. The angle from Si and SiGe surface is 40°. We can clearly see that a smooth SiGe surface around Si pillar is realized with tapered facets at the corners of laterally grown SiGe and vertical {111} facets at the SiGe growth front. Figure 2b shows an AFM surface topography image of a Si mesa structure after HCl VPE followed by lateral selective growth of SiGe and SiO_2 cap removal by HF. After the HCl VPE, ∼1.25 μm square Si mesa with ⟨110⟩ oriented sidewalls are formed. The interface between the Si pillar and the deposited SiGe can be identified by small step height

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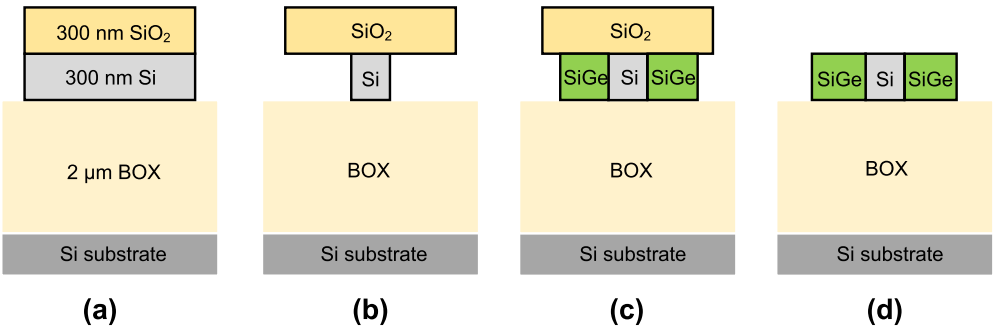
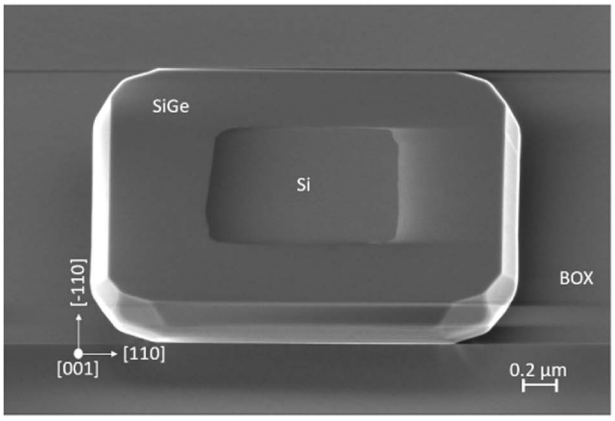
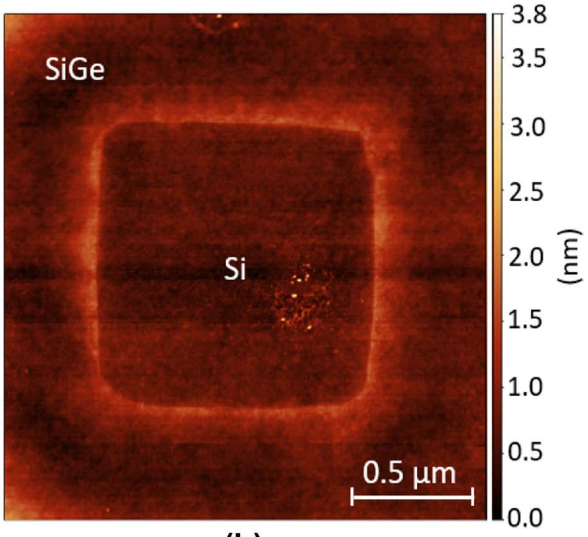


Figure 1. Schematic diagrams after (a) mesa structure formation by photolithography and dry etching, (b) HCl VPE for Si pillar and lateral cavity formation at 850 °C. (c) lateral selective SiGe epitaxy at 750 °C. (d) thermal oxide removal by HF dip.



(a)



(b)

Figure 2. (a) Angle-view scanning electron microscopy image of laterally grown selective SiGe around Si pillar after top SiO_2 removal by HF, (b) AFM surface topography image of lateral-selective SiGe around Si pillar after top oxide removal.

of ∼0.6 nm. Possible reason of the step formation at interface between the Si pillar and SiGe is as follows. At an initial stage of the lateral selective SiGe growth, the SiGe is pseudomorphically grown and fully strained. During the SiGe growth, plastic relaxation occurs after exceeding critical thickness by misfit dislocation (MD) formation at the interface by slipping. By the plastic deformation of SiGe, thickness of SiGe toward [001] direction becomes higher compared to that of Si pillar part, resulting in step formation. The root mean square roughness (RMS) of the selectively grown SiGe part is ∼0.14 nm, and top of the Si pillar is ∼0.15 nm. These are as smooth as blanket Si (001). The RMS roughness is determined by interface roughness of the sacrificially etched SOI and the SiO_2 cap. The HCl VPE process of Si is highly selective to SiO_2, therefore roughness of oxide is maintained after the HCl VPE. By the lateral selective SiGe growth, the roughness of the bottom of the SiO_2 cap is transferred to the surface roughness of the SiGe.

Figure 3 shows EDX line-profile of laterally grown SiGe. The SiGe lamella which is used for this EDX analysis is cut out from laterally grown SiGe near Si pillar. The Ge content of ∼40% is obtained and uniformly distributed in the SiGe layer along ⟨110⟩. It is to be noted that the difference of Ge composition along ⟨010⟩ direction was within the measurement error of top-view Micro-Raman measurements. At the edge of SiGe, a drop of the Ge composition is observed. This is because at the edge of SiGe, there is reduction of TEM lamella thickness due to tapered facets at the corners of laterally grown SiGe. By the thickness reduction, EDX intensity of both Si and Ge becomes weaker, but the Si intensity cannot reduce to zero even if the TEM lamella thickness becomes zero, because of presence of Si in the EDX detector. Based on these results, we conclude that micro-loading effect of the lateral selective SiGe growth process used for this experiment is low. This means enough amount of each reactant gases (in this case, SiH_2Cl_2, GeH_4 and HCl) are reaching to growth front of the SiGe in the cavity. As a result, the Ge content in the SiGe (and also growth rate of SiGe) in the cavity is uniform. Therefore, this process can be applied for local SGOI VS fabrication.

Figures 4a, 4b shows in-plane strain distribution mappings of the Si pillar and the laterally grown SiGe by micro-Raman spectroscopy analysis. Biaxial strain and composition of SiGe were evaluated using the peak energy Ge-Ge (∼290 cm^{-1}), Si-Ge (∼405 cm^{-1}) and Si-Si (∼500 cm^{-1}) modes. Using the parameters and the method reported in,[8] we calculated the composition and biaxial strain at each point of the map. For Si, the strain shift coefficient −830 cm^{-1} was used,[9] after calibration of the position of the Si peak with an unstrained Si wafer. A relative uniform tensile-strain of ∼0.65% is observed in the Si pillar part (Fig. 4a). However, the strain is negligible in the SOI in unpatterned wide area outside of the checkerboard mesa structures. This means the tensile strain in the Si pillar is formed by HCl VPE and/or lateral selective growth of SiGe. A possible mechanism of strain inducing is as follows. SOI is compressively strained at 850 °C for HCl VPE process, because Si has higher thermal expansion compared to SiO_2. During the HCl VPE, area of the Si pillar/SiO_2 interface decreases since SOI is etched from all sides of the mesa structure. Due to the reduced area, mechanical robustness of the interface becomes weaker. The weakened robustness allows slipping of the interface to compensate the compressive strain of the Si pillar during HCl VPE at 850 °C. During cooling from 850 °C to SiGe deposition temperature of 750 °

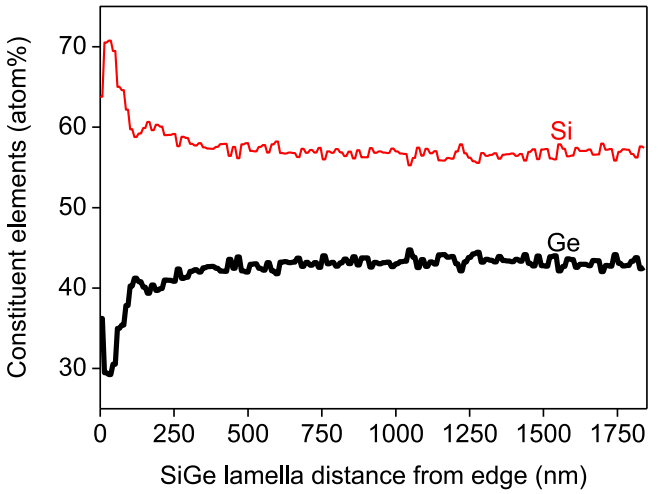


Figure 3. EDX line-profile of laterally grown selective SiGe around Si pillar. SiGe lamella used for the EDX analysis is cut out from laterally grown SiGe near Si pillar (as marked in Fig. 5a).

C, the interface could slip back, but a slight tensile strain could remain in the Si pillar at 750 °C, because driving force for the slipping becomes lower due to reduced temperature. Therefore, there could be a possibility of some tensile strain developed in Si just after HCl VPE and before SiGe growth. After the growth of SiGe at 750 °C, the tensile strain in the Si pillar is formed during cooling down to room temperature, because the Si pillar is pinned with the SiO_2. On the other hand, in the laterally grown SiGe part (Fig. 4b), tensile strain of ∼1.4% and ∼0.9% are observed along ⟨010⟩ and ⟨110⟩ directions, respectively. The root cause of the tensile strains could be that the laterally grown SiGe is not fully relaxed. Therefore, lattice parameter of the SiGe towards growth direction is higher compared to perpendicular directions.

In order to discuss the strain distribution of SiGe in more detail, NBD of laterally grown SiGe around the Si pillar is performed. Figure 5a represents 3D schematic image of the laterally grown SiGe around the Si pillar on BOX after the SiO_2 cap removal. The mappings of relative change of in-plane and out-of-plane lattice parameters of SiGe near the Si pillar by NBD are shown in Figs. 5b, 5c, respectively. The SiGe sample lamella is cut out along [110] direction beside the Si pillar, whose position is marked as a square in

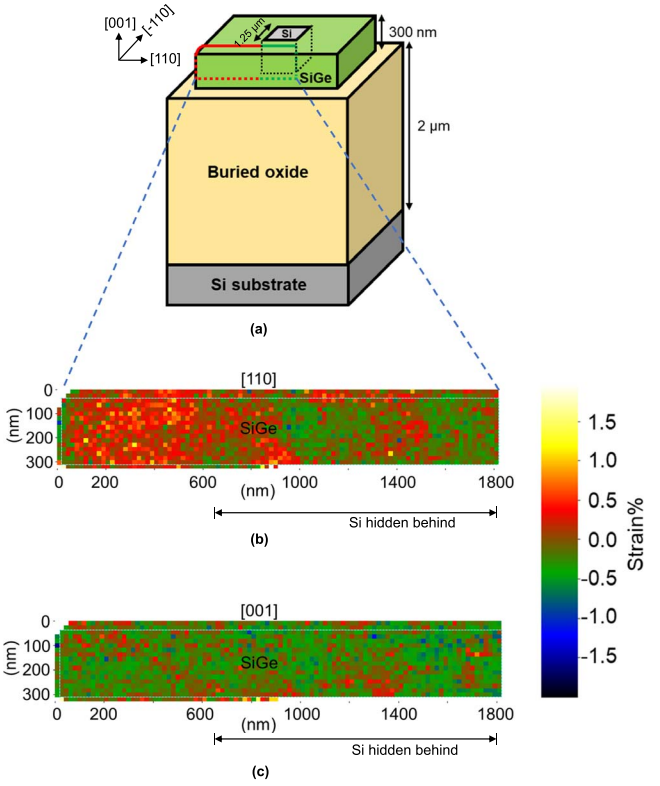


Figure 5. (a) 3D schematic image of laterally grown selective SiGe around Si pillar on SOI after top SiO_2 removal by HF. (b) in-plane strain distribution and (c) out-of-plane strain distribution of laterally grown selective SiGe measured by NBD. (a) shows the position of lamella used for (b) and (c).

Fig. 5a. In Fig. 5b, higher in-plane lattice parameter along [110] is observed in the edge part of SiGe lamella as compared to the center part. However, the out-of-plane lattice parameter along [001] (Fig. 5c) is homogeneous across the entire SiGe. Because uniform Ge concentration in the SiGe layer is confirmed by Fig. 3, the higher lateral lattice parameter near the edge is due to higher tensile strain as compared to near the center area. Based on the result of a 700 nm thick 40% SiGe layer deposited on a Si (110) substrate, which has the same thickness as the laterally grown SiGe around the Si pillar in the cavity, a degree of relaxation of ∼90% is confirmed. Therefore,

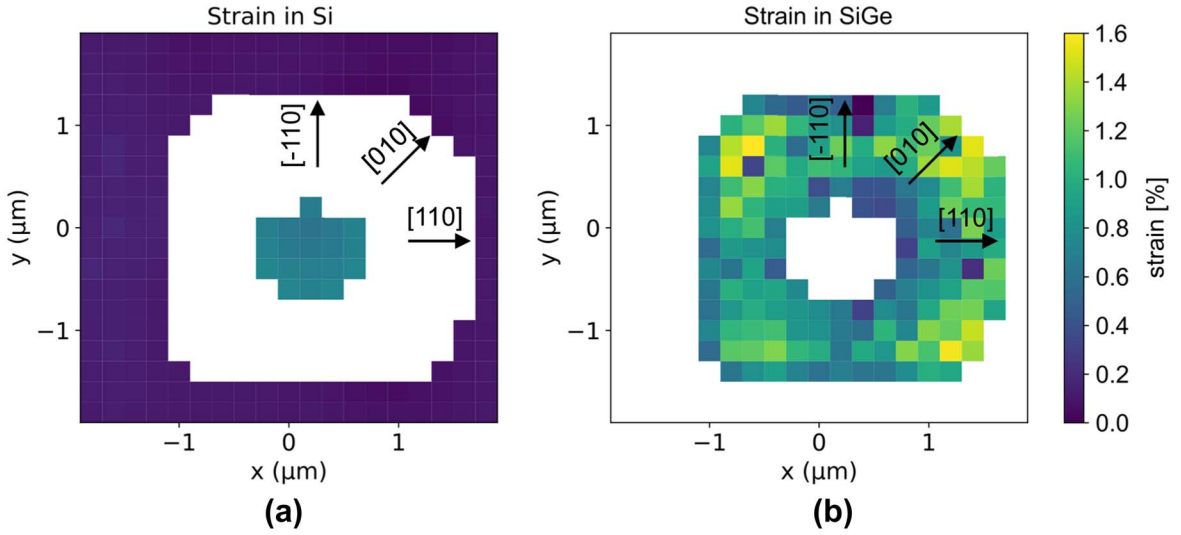


Figure 4. In-plane strain distribution obtained by micro-Raman measurements in (a) Si pillar and (b) laterally grown selective SiGe around Si pillar.

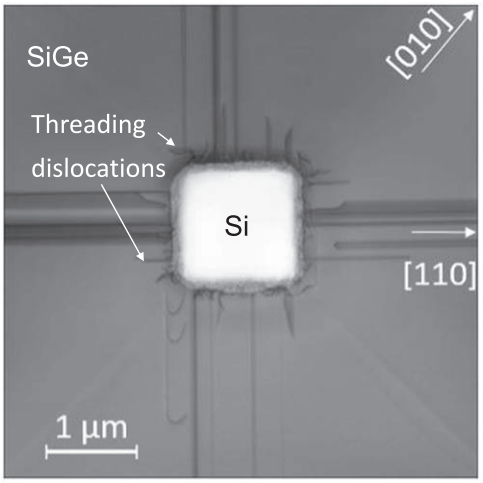


Figure 6. Plan-view TEM image of lateral-selectively grown SiGe around Si pillar.

the degree of relaxation of the laterally grown SiGe is also expected to be ∼90%. This indicates the presence of compressive strain towards vertical [001] direction and tensile strain towards horizontal [110] direction in the laterally grown SiGe layer. Around the Si pillar, the strain distribution along 90° rotated direction (i.e. along [−110] and [1–10]) should be symmetric to [110] direction. Therefore, higher tensile strain is formed at the corners of the SiGe along [010] which is induced from both [110] and [−110] directions.

Figure 6 shows a plan-view TEM image of lateral selectively grown SiGe around the Si pillar. Stacking faults of SiGe on (111) plane are observed along [110] and [1–10] directions. There is also presence of TDs along ⟨111⟩, which terminates at the SiO_2 cap and the BOX. Also, these TDs are located only up to ∼400 nm from Si, which indicates that ART mechanism[10] is working in horizontal direction. The misfit dislocations are present only at the Si/SiGe interface. Because the stacking faults run only towards [110] and [1–10] directions, dislocations cannot be eliminated in [110] directions. However, toward [010] direction, it is possible to fabricate wide region of dislocation-free area.

Conclusion

Dislocation free local SGOI VS by lateral selective growth of SiGe by RPCVD is demonstrated. Lateral HCl VPE of the Si from all sides of 6.3 μm square checkerboard mesa structured SiO_2 cap on SOI is performed to form Si pillar and the cavity and lateral selective SiGe growth is performed. A smooth SiGe surface, whose RMS roughness of 0.14 nm, is realized because the surface roughness of the SiGe is determined by the interface roughness of the sacrificially etched SOI and the SiO_2 cap. The Ge content in the laterally grown SiGe is uniform across the SiGe layer, which is advantageous for VS applications. The Si pillar has ∼0.65% tensile strain which may be due to thermal expansion difference between SiO_2 and Si. In the SiGe part, additional tensile strain of ∼1.4% in SiGe along ⟨010⟩ directions, which is induced from both [110] and [−110] directions, is observed. TDs in the SiGe are located only ∼400 nm from Si pillar and stacking faults are running toward ⟨110⟩ directions, resulting in a wide dislocation-free area in SiGe along ⟨010⟩ due to horizontal aspect-ratio trapping. The dislocation-free area can be applied for local SGOI VS fabrication.

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