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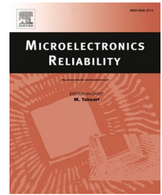

PS-BBICS: Pulse stretching bulk built-in current sensor for on-chip measurement of single event transients

Marko Andjelkovic [a,*], Milos Marjanovic [b], Junchao Chen [a], Stefan Ilic [b,d], Goran Ristic [b], Milos Krstic [a,c]

[a] IHP – Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder), Germany
[b] Faculty of Electronic Engineering, University of Niš, Niš, Serbia
[c] University of Potsdam, Potsdam, Germany
[d] Center for Microelectronic Technologies, Institute for Chemistry, Technology and Metallurgy, Belgrade, Serbia

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ABSTRACT

The bulk built-in current sensor (BBICS) is a cost-effective solution for detection of energetic particle strikes in integrated circuits. With an appropriate number of BBICSs distributed across the chip, the soft error locations can be identified, and the dynamic fault-tolerant mechanisms can be activated locally to correct the soft errors in the affected logic. In this work, we introduce a pulse stretching BBICS (PS-BBICS) constructed by connecting a standard BBICS and a custom-designed pulse stretching cell. The aim of PS-BBICS is to enable the on-chip measurement of the single event transient (SET) pulse width, allowing to detect the linear energy transfer (LET) of incident particles, and thus assess more accurately the radiation conditions. Based on Spectre simulations, we have shown that for the LET from 1 to 100 MeV cm^2 mg^{-1}, the SET pulse width detected by PS-BBICS varies by 620–800 ps. The threshold LET of PS-BBICS increases linearly with the number of monitored inverters, and it is around 1.7 MeV cm^2 mg^{-1} for ten monitored inverters. On the other hand, the SET pulse width is independent of the number of monitored inverters for LET > 4 MeV cm^2 mg^{-1}. It was shown that supply voltage, temperature and process variations have strong impact on the response of PS-BBICS.

1. Introduction

The radiation-induced soft errors are one of the most common causes of performance degradation and operational failures in spaceborne electronics. A soft error denotes an undesired bit-flip in storage elements (memory and sequential logic). It may occur when a high energy particle, such as a heavy ion, proton, or neutron, hits a sensitive transistor in storage elements or in combinational logic. The memory and sequential elements are generally most susceptible to soft errors. However, with the scaling of transistor size and supply voltage, and the increase in clock frequency, the soft error rate (SER) due to particle strikes in combinational logic has increased significantly [1].

If an incident particle deposits sufficient charge in a sensitive transistor within a combinational gate, a transient current pulse may be induced. The current pulse may result in a transient voltage pulse, known as a single event transient (SET), which may then cause one or more bit-flips if it propagates through the circuit and is captured by the memory or sequential elements. The SER of a combinational circuit is linearly proportional to particle flux and SET pulse width. The SET pulse width varies from tens of ps to several ns, and it is defined by the linear energy transfer (LET) of incident particles, as well as the design, operating, and technology parameters. On the other side, the particle flux in space may vary over several orders and magnitude, where the peak flux periods may last for several hours or days [2]. Thus, having the real-time information on particle flux and LET is essential for selecting the most suitable soft error mitigation approach.

Because of variable intensity of space radiation, the use of static mitigation measures is not cost-effective. Namely, with the static mitigation, the protection mechanisms would be always active, even under low radiation intensity that may not be critical for system operation, thereby leading to an increased power consumption. An optimal fault tolerance of a complex digital design can be achieved by dynamic activation of protection mechanisms only at critically high radiation intensity. This allows to achieve a trade-off between performance, fault tolerance and power consumption during the runtime. To enable such a scenario, the radiation sensors for monitoring of both particle flux and

* Corresponding author.
E-mail address: andjelkovic@ihp-microelectronics.com (M. Andjelkovic).

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LET are necessary. Therefore, when the sensors detect critical radiation levels, the fault-tolerant mechanisms can be activated to protect the most sensitive elements in the system, and then switched-off when the radiation intensity decreases below the critical level.

Numerous solutions for soft error monitoring in space have been proposed. The most common sensors are PN/PIN diodes or photodiodes [3,4], stand-alone SRAMs [5,6], 3D NAND flash detectors [7], acoustic wave detectors [8], and bulk built-in current sensors (BBICS) [9–13]. We have proposed two alternative solutions: embedded SRAM [14] and custom-sized inverter chain [15,16]. Each sensor has advantages over other counterparts, but also certain limitations. A brief comparison is given in Section 2, while a more detailed analysis can be found in [17].

In this paper, we introduce a pulse stretching BBICS, denoted as PS-BBICS. The PS-BBICS extends the standard BBICS by adding a custom-sized pulse stretcher composed of two inverters. The proposed solution combines the unique advantages of standard BBICS with the possibility to measure the SET pulse width. The benefits offered by the BBICS and PS-BBICS are elaborated in Section 2.

The rest of the paper is structured as follows. In Section 2, a brief review of common particle detectors and contributions of our paper are presented. Section 3 discusses the design and operating principles of conventional BBICS. The proposed pulse stretching BBICS is introduced in Section 4. The simulation results are presented and discussed in Section 5.

2. Related work and paper contribution

In general, a particle detector must have higher sensitivity than the circuit that should be protected, and the complexity of the detector and corresponding processing logic should be as low as possible in order to reduce the overhead in terms of area and power consumption. As none of available solutions satisfies all requirements, the selection of the most suitable approach for particle detection in a given application is based on a trade-off between the requirements and the sensor performance.

One of the most common types of radiation detectors are PN/PIN diodes and photodiodes [3,4], which can be implemented either as discrete detectors or integrated on a chip. With appropriate mixed-signal processing circuitry, these detectors can provide very accurate measurement of radiation exposure, with detailed information on induced charge, particle LET, energy spectra and flux. However, the complexity of mixed-signal processing circuitry is very high, which is reflected in the cost of implementation. In addition, the power consumption due to complex processing logic is usually high.

A low-cost alternative to diode-based detectors are the SRAM-based detectors. Due to high sensitivity of SRAM cells to particle strikes, a stand-alone SRAM chip can be used to measure the particle count rate in terms of the number of bit-flips [5,6], from which the particle flux can be determined. The advantages of SRAM detectors are simple operating principle and fully digital processing. To reduce the overhead, we have proposed the use of embedded SRAM, i.e., the SRAM used for data storage also acts as a radiation sensor [14]. However, the main issue with SRAM-based detectors is susceptibility to multiple bit-flips, potentially leading to error accumulation.

In [7], the applicability of 3D NAND flash memory as a particle detector has been investigated with heavy ions experiments. A flash memory based on floating gate transistors was analyzed, and the heavy ion strikes were detected by measuring the threshold voltage shift of floating gate transistors. This solution enables to measure the particle count rate, angle of incidence, and LET. However, analog processing is required, and the integration on the same chip with the target design is challenging.

The monitoring of soft errors with acoustic wave detectors has been investigated in [8]. As a result of a particle strike, the acoustic waves are generated in the substrate of the target chip. Special cantilever devices are used as acoustic wave detectors, and the detection principle is based on measuring the change of the sensor's capacitance. The acoustic wave detectors are distributed across the chip, enabling to detect the strike location. However, the need for mixed-signal processing increases the overall design complexity. In addition, the functionality of this sensor has still not been verified experimentally.

As the particle strikes induce current pulses in target devices, specially designed current sensors could be employed for soft error monitoring. A typical solution is the bulk built-in current sensor (BBICS), which generates a transient voltage pulse, i.e., an SET, as a response to particle-induced current. The use of BBICS [9–13] for soft error detection offers several advantages. First, these sensors are distributed across the chip, allowing to detect the locations of particle strikes, and subsequently apply the error correction only to the affected logic. Second, the area and power overhead are lower compared to the sensors which require mixed-signal processing. Third, the signal processing can be done with simple digital logic.

In our previous work [15,16], we have proposed the use of customized pulse stretching inverter chains as particle detectors. The operating principle is based on detecting the SETs induced in inverter chain. Serially connected inverters can measure the particle count rate in terms of SET count rate [15], while parallel configuration enables to measure also the LET variations in terms of SET pulse width variations [16]. The main advantage of proposed solution is that it requires only digital readout electronics.

Among the aforementioned detectors, BBICS is the only experimentally verified detector that can be distributed across the chip, allows identifying the strike locations, and requires only digital readout. However, to our best knowledge, previous works on BBICS have not analyzed the possibility of SET pulse width monitoring. In this work we analyze the possibility to improve the BBICS performance by enabling the SET pulse width measurement. Such a solution would allow for a more detailed assessment of the radiation conditions, providing the information on the strike location, particle count rate and LET, which is not possible with any other particle detector supporting only digital readout.

3. Particle detection with BBICS

The BBICS can detect the particle strikes in both combinational and sequential logic. It is connected directly to the bulk of monitored transistors, and the operating principle is based on detecting the particle-induced transient current flowing through the bulk of sensitive (off-state) transistors [9,10].

Two separate sensors are required for monitoring PMOS and NMOS transistors. Fig. 1 depicts the simplest architecture of BBICS for monitoring the PMOS transistors [9,10]. To ensure proper functioning, the transistors M1 and M2 should have a large W/L ratio, while the pull-down transistor M3 should have a small W/L ratio. The resistance of transistor M3 can be adjusted by varying the gate voltage V_G, thus controlling the sensitivity of the sensor. Under normal operation the

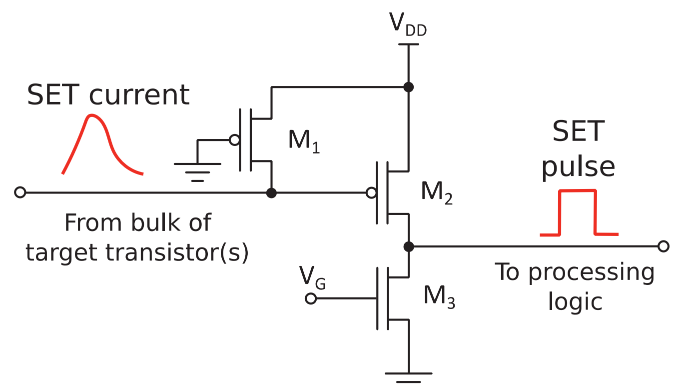

Fig. 1. A BBICS for detecting SETs in PMOS transistors.

output of sensor is at logic 0. When a particle hits a sensitive transistor, a transient current pulse will flow through M1. If the current pulse has sufficient amplitude and width, it will be converted into a voltage pulse, which serves as an indication of a particle strike. For monitoring the NMOS transistors, M2 should be NMOS while M3 should be PMOS, and M1 should be NMOS transistor connected between the gate of M3 and ground.

In general, a single BBICS can monitor tens of transistors, depending on the sensor design. However, the sensitivity of BBICS decreases with the number of monitored transistors. Fig. 2 shows a schematic for monitoring the particle strikes in a chain of inverters using two BBICS. The output of each BBICS is interfaced to a register that records the number of detected errors. Based on the collected data, the soft error mitigation mechanisms can be activated to restore the normal operation of the affected circuit.

Various alternative BBICS designs with improved sensitivity, but with more transistors than the variant in Fig. 1, have been proposed [11–13]. The operation of BBICS has been verified with both simulations and laser/irradiation experiments for bulk CMOS technology nodes from 28 nm to 130 nm [11–13]. In practical implementations, the area overhead due to addition of BBICS is an important design constraint. The area overhead depends on the sensor configuration (number of transistors) and the target design. Due to variable sensitivity of on-chip logic, the sensors can be connected only to the most sensitive circuits, thus minimizing the area overhead. The analysis presented in [12] shows that the area overhead may vary from 12 to 36 %.

4. Proposed pulse stretching BBICS (PS-BBICS)

In order to enable the on-chip SET pulse width measurement, we propose a pulse stretching BBICS (PS-BBICS). The PS-BBICS is composed of a standard BBICS (transistors M1, M2 and M3) and a custom-sized pulse stretcher (transistors M4, M5, M6 and M7), as illustrated in Fig. 3. The idea of adding the pulse stretcher is to extend short SET pulses, and thus facilitate their processing in the subsequent SET pulse width measurement circuit.

The transistor sizes for the pulse stretcher are selected according to relations (1)–(4). The pulse stretching, i.e., the ratio between the input and output pulse widths, is defined by the PMOS-to-NMOS channel width ratio. More details on the operation of the pulse stretcher can be found in [18].

$$W_M_4 = W_M_7 \tag{1}$$

$$W_M_5 = W_M_6 \tag{2}$$

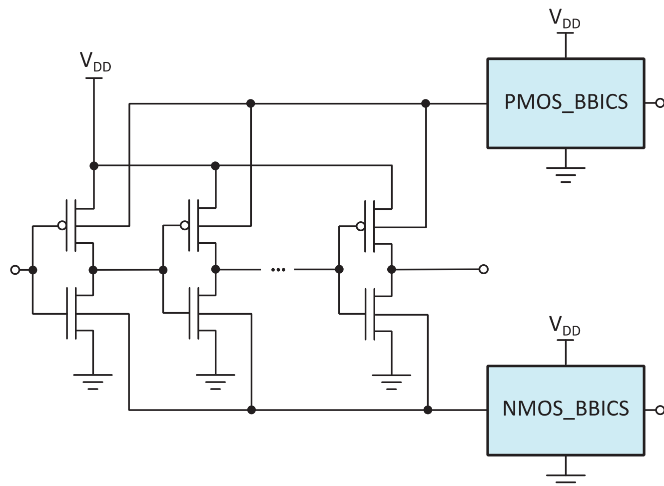

Fig. 2. Monitoring of a chain of inverters with two sensors.

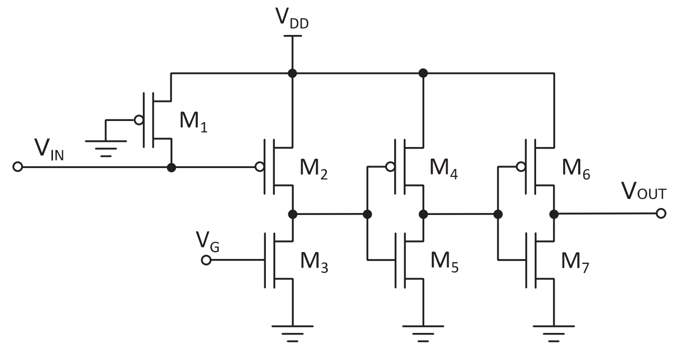

Fig. 3. Proposed PS-BBICS for monitoring PMOS transistors.

$$W_M_5 > W_M_4 \tag{3}$$

$$W_M_6 > W_M_7 \tag{4}$$

Besides modification of the sensor design, the processing logic should be also modified. In addition to the registers for storing the number of detected strikes, a dedicated logic is needed for SET pulse width measurement and processing of acquired data.

5. SET response of PS-BBICS

5.1. Simulation setup

To investigate the SET response of the proposed PS-BBICS design, we have conducted exhaustive electrical simulations using Cadence Spectre. As a case study, we have used the IHP's 130 nm bulk CMOS technology. The simulation setup is shown in Fig. 4. A chain of standard inverters with minimum size was used as a target circuit. Without loss of generality, the analysis was done for high logic level at the input of inverter chain. Thus, the PS-BBICS is connected to the bulk of all PMOS transistors, which are in off-state and are sensitive to SETs.

The SETs were simulated by injecting the current pulse I_{SET} in the PMOS transistor in first inverter. For this purpose, the bias-dependent current model proposed in [19] was used. This model is composed of a storage capacitor C whose value can be chosen arbitrarily, and three current sources: a standard double-exponential current source I_{DEXP} and voltage-dependent current sources G_{REC} and G_{SEE}. The capacitor and current sources are connected in parallel, as illustrated in Fig. 5. G_{REC} represents the recombination current, while G_{SEE} is the internal single-event junction current. Detailed equations for G_{REC} and G_{SEE} can be found in [19].

According to [20], the double-exponential current source I_{DEXP} can be expressed with relation (5), where τ_{rise} is the rise time constant, τ_{fall} is

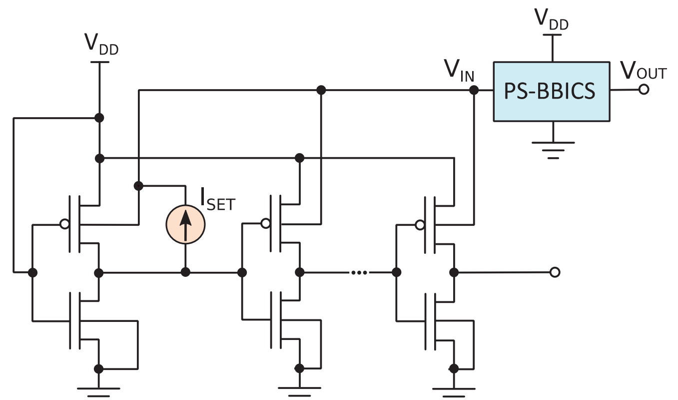

Fig. 4. Monitoring of PMOS transistors in a chain of inverters with PS-BBICS.

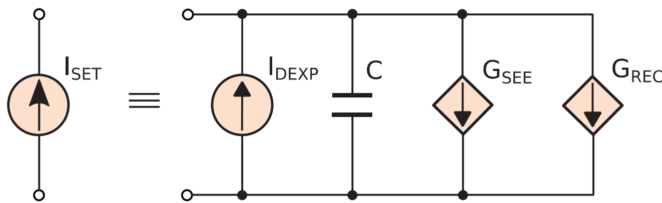

Fig. 5. Bias-dependent SET current model [20].

the fall time constant, and Q is the total collected charge. In this case, the rise and fall time constants were 10 and 100 ps, respectively. These values correspond well to the average SET pulse widths measured for 130 nm technology, and were chosen based on comparison of experimental results from [21] and our simulation results from [17]. Note that the rise and fall time constants depend on the particle's strike location and angle of incidence. The collected charge Q (in pC) can be expressed in terms of effective charge collection length l (in μm) and particle LET through the relation (6). For this analysis we have chosen $l = 2.1$ μm, based on the results for 130 nm technology obtained from device simulations [22]. The value of LET was varied from 1 to 100 MeV cm^2 mg^{-1}.

$$I_{DEXP}(t) = \frac{Q}{\tau_{fall} - \tau_{rise}}\left(e^{\frac{-t}{\tau_{fall}}} - e^{\frac{-t}{\tau_{rise}}}\right) \quad (5)$$

$$Q = 1.035 \times 10^{-2} \times l \times LET \quad (6)$$

The SET response of PS-BBICS was analyzed in terms of two metrics: threshold LET (LET_{TH}) and SET pulse width. The transistor sizes were initially chosen to obtain as low LET_{TH} as possible. The LET_{TH} was determined as the minimum value of LET which causes a SET pulse with amplitude beyond the half of supply voltage at the output of PS-BBICS. With the selected transistor sizes, the SET pulse width at the output of PS-BBICS was analyzed in terms of gate voltage at pull-down transistor M3, number of monitored inverters, supply voltage, temperature, process corners, and LET. Unless otherwise specified, the simulations were done for supply voltage of 1.2 V and temperature of 27 °C.

5.2. Results and discussion

The primary requirement for a particle detector is to have as high sensitivity as possible, i.e., as low LET_{TH} as possible. To this end, the dependence of LET_{TH} on transistor size was investigated, and the obtained results are given in Table 1. We have chosen the transistor sizes for $LET_{TH} = 1$ MeV cm^2 mg^{-1}, and all following results are for this value. This LET_{TH} value was chosen because most particles in space have LET > 1 MeV cm^2 mg^{-1}.

The response of standard BBICS (without pulse stretcher) and PS-BBICS (with pulse stretcher) is illustrated in Fig. 6. It can be noticed that the addition of a pulse stretcher causes significant increase of the SET pulse width, which is a desirable feature when it is required to measure short SET pulses. The impact of pulse stretcher is particularly pronounced for low voltage at the gate of M3 transistor. Accordingly, all following results are for the gate voltage of 0.8 V.

Fig. 7 depicts the threshold LET and SET pulse width as a function of the number of monitored inverters. The SET pulse width is obtained for

Table 1
LET_{TH} and transistor sizes for PS-BBICS.

LET_{TH} (MeV cm^2 mg^{-1})	W/L (μm/μm)		
	M1, M2	M3, M4, M7	M5, M6
0.7	0.6/0.13	0.15/0.13	0.35/0.13
0.8	0.9/0.13		1.5/0.13
0.9	1/0.13		2.75/0.13
1.0	1.2/0.13		4/0.13
2.0	3.25/0.13		12.5/0.13

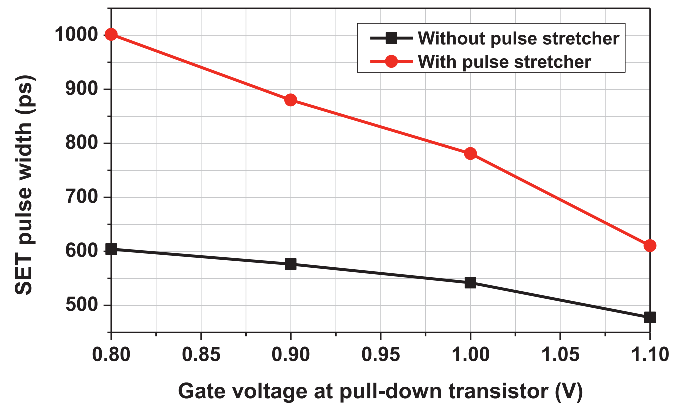

Fig. 6. SET pulse width as a function of gate voltage at pull-down transistor M3, for LET = 60 MeV cm^2 mg^{-1}, with and without pulse stretcher.

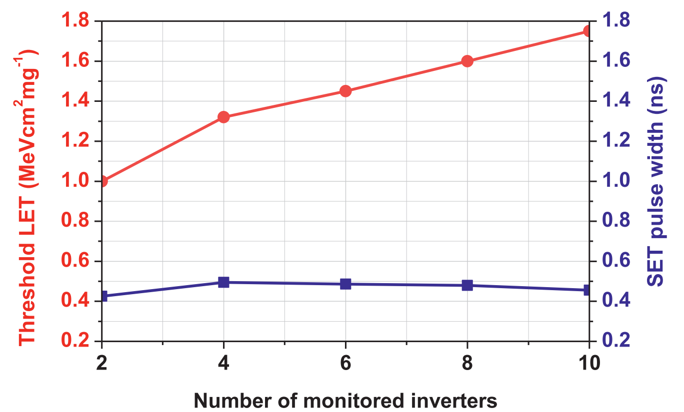

Fig. 7. Threshold LET and corresponding SET pulse width as a function of number of monitored inverters.

$LET = LET_{TH}$. As can be seen, the LET_{TH} increases almost linearly with the number of inverters. This is because the increase of the number of inverters increases the load capacitance, which directly impacts the total charge that can be accumulated in the target node. However, it is interesting that the SET pulse width is almost invariant with the number of inverters.

The SET pulse width as a function of LET, for 2 and 10 monitored inverters, is illustrated in Fig. 8. In Fig. 9, the waveforms of SET pulses at the input and output of PS-BBICS, for 2 and 10 monitored inverters, and

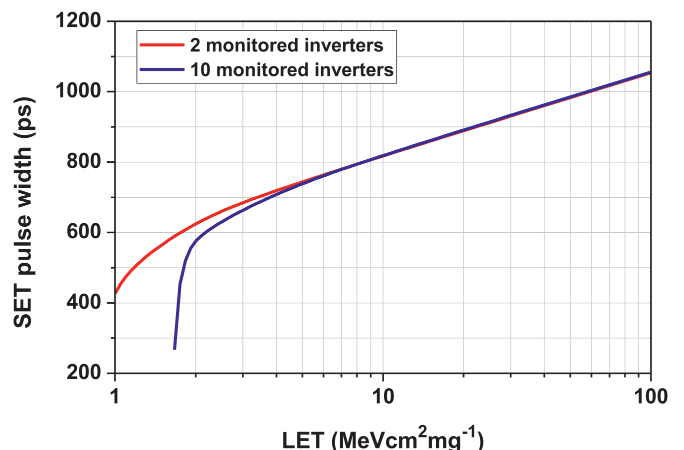

Fig. 8. SET pulse width as a function of LET, for 2 and 10 monitored inverters.

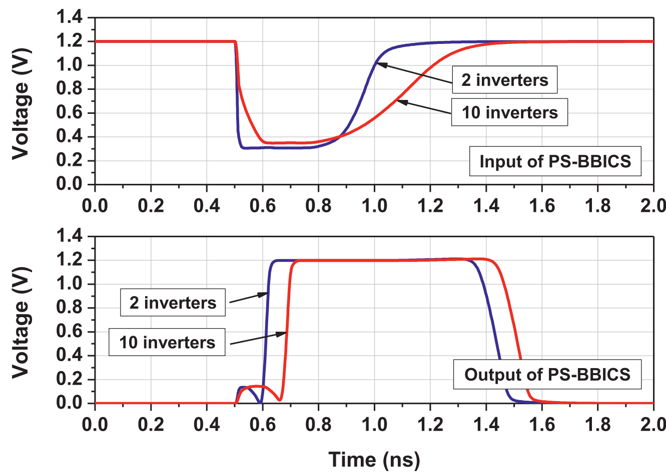

Fig. 9. Waveforms at input and output of PS-BBICS, for 2 and 10 monitored inverters, when the current pulse with LET = 10 MeV cm^2 mg^{-1} is injected in first inverter.

LET of 10 MeV cm^2 mg^{-1}, are shown. The SET pulse width is dependent on the number of inverters only for LET < 4 MeV cm^2 mg^{-1}, while at higher LET the SET pulse width is the same, which is in good agreement with the results in Fig. 7. As can be observed, the SET pulse width varies by 620–800 ps over the analyzed LET range. Thus, by measuring the SET pulse width, the LET of incident particles can be estimated.

Based on the results presented in Figs. 8 and 9, we assume that the number of monitored inverters does not affect the SET pulse width at higher LET because the total capacitance of ten inverters is insufficient to suppress the SET pulses induced by the high-LET particles. To investigate this in more detail, we plan to conduct the analysis with different sizes of monitored inverters, as well as with different types of monitored gates.

Fig. 10 illustrates the SET pulse width as a function of LET, for different supply voltages and ten monitored inverters. As supply voltage increases, the SET pulse width decreases, while the LET_{TH} increases. This is due to the increase of driving current with the increase of supply voltage. For the supply voltage from 1 to 1.2 V, the SET pulse width variation is around 120 ps. Similar variation in SET pulse width was observed for smaller number of monitored inverters. However, decreasing the supply voltage below 1 V leads to a degradation of sensor's response, implying that the sensor should not be operated at low supply voltage.

The increase in temperature leads to a decrease of the sensitivity of PS-BBICS, i.e., the SET pulse width decreases and LET_{TH} increases, as depicted in Fig. 11. The variation of SET pulse width may be >500 ps over the investigated temperature range from −40 °C to 125 °C. The conducted analysis has shown that the SET pulse width variation with temperature increases with the number of monitored inverters. It is important to note that the impact of temperature is opposite to that in other standard cells, where the increase in temperature results in a decrease in LET_{TH} and an increase in SET pulse width. The observed effect can be attributed to the specific transistor sizing applied for PS-BBICS.

In Fig. 12, the SET pulse width dependence on process corners, for ten monitored inverters, is depicted. Three corner cases have been considered: *tt* (typical-typical), *ss* (slow-slow) and *ff* (fast-fast). For *ff* corner (when both NMOS and PMOS transistors are fast), the SET pulse width may be up to 100 ps shorter than for *tt* corner. On the other hand, for *ss* corner (when both NMOS and PMOS transistors are slow), the SET pulse width may be almost 200 ps longer than for *tt* corner. The number of monitored inverters has minor impact on these variations. Nevertheless, the observed variations in the SET pulse width may affect the measurement accuracy. Therefore, it is necessary to take into account the impact of process corners during the calibration of on-chip sensor.

6. Conclusion

In this paper, the applicability of a BBICS with a pulse stretcher (PS-BBICS) for monitoring the SET pulse width in digital circuits has been analyzed for the first time. The simulation results indicate that the proposed PS-BBICS can detect the SET current pulses caused by energetic particles with LET from 1 to 100 MeV cm^2 mg^{-1}. It was shown that the SET pulse width increases by 620–800 ps over the investigated LET range, for up to ten monitored inverters. For accurate SET pulse width measurement, the supply voltage and temperature variations must be monitored online, and the impact of process corners must be taken into account.

As a future work we will investigate alternative PS-BBICS configurations, in order to reduce the impact of supply voltage, temperature and process corners, and increase the number of gates that can be monitored with a single PS-BBICS. Moreover, we will analyze the impact of different types and sizes of monitored gates on the SET pulse width. To verify the proposed sensor, we plan to design a test chip and perform the irradiation campaign with heavy ions.

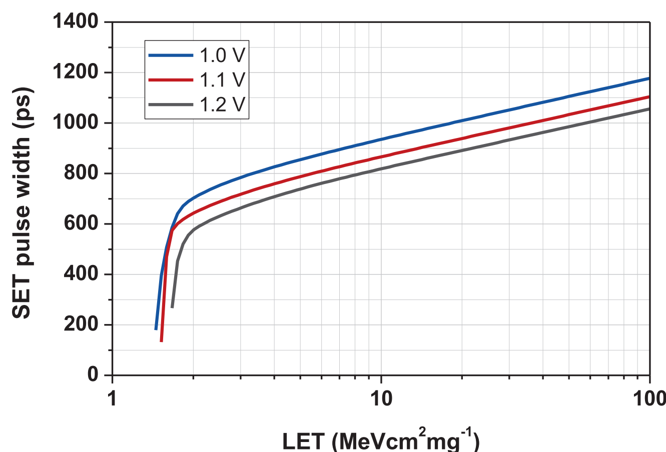

Fig. 10. SET pulse width as a function of LET and supply voltage, for 10 monitored inverters.

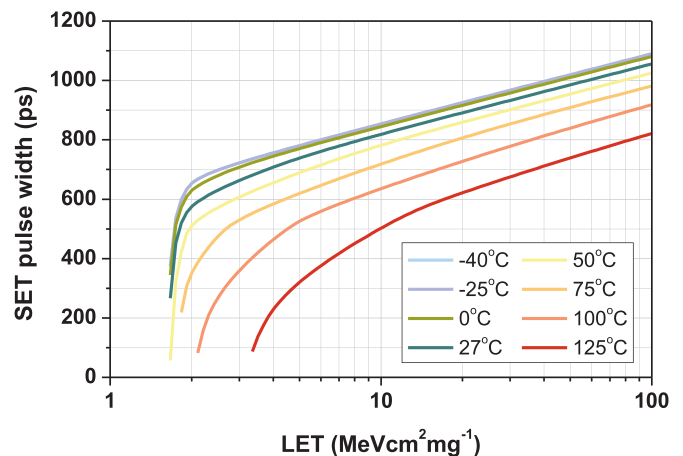

Fig. 11. SET pulse width as a function of LET and temperature, for 10 monitored inverters.

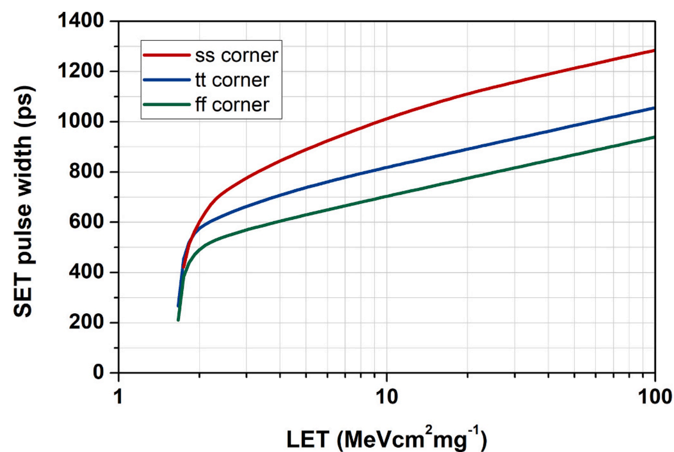

Fig. 12. SET pulse width as a function of LET, for three process corners and 10 monitored inverters.

CRediT authorship contribution statement

Marko Andjelkovic: Conceptualization, Methodology, Investigation, Validation, Data curation, Writing – Original draft, Project administration, Supervision
Milos Marjanovic: Conceptualization, Methodology, Investigation, Validation, Data curation, Writing – Review & editing
Junchao Chen: Methodology, Writing – Review & editing
Stefan Ilic: Methodology, Writing – Review & editing
Goran Ristic: Resources, Project administration, Supervision
Milos Krstic: Resources, Project administration, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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