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Analysis of Single Event Transient Effects in Standard Delay Cells Based on Decoupling Capacitors*

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Single Event Transients (SETs), i.e., voltage glitches induced in combinational logic as a result of the passage of energetic particles, represent an increasingly critical reliability threat for modern complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) employed in space missions. In rad-hard ICs implemented with standard digital cells, special design techniques should be applied to reduce the Soft Error Rate (SER) due to SETs. To this end, it is

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essential to consider the SET robustness of individual standard cells. Among the wide range of logic cells available in standard cell libraries, the standard delay cells (SDCs) implemented with the skew-sized inverters are exceptionally vulnerable to SETs. Namely, the SET pulses induced in these cells may be hundreds of picoseconds longer than those in other standard cells. In this work, an alternative design of a SDC based on two inverters and two decoupling capacitors is introduced. Electrical simulations have shown that the propagation delay and SET robustness of the proposed delay cell are strongly influenced by the transistor sizes and supply voltage, while the impact of temperature is moderate. The proposed design is more tolerant to SETs than the SDCs with skew-sized inverters, and occupies less area compared to the hardening configurations based on partial and complete duplication. Due to the low transistor count (only six transistors), the proposed delay cell could also be used as a SET filter.

Keywords: Single event transients; standard delay cells; decoupling capacitors.

1. Introduction

The natural radiation in space poses a serious threat to the electronic systems employed in space missions. As a consequence of exposure to ionizing radiation, the electrical characteristics of devices and circuits may be altered, leading to performance degradation, malfunction and permanent or temporary failures. Since maintenance is usually impossible in space, it is necessary to ensure that the spaceborne electronics meets the highest level of reliability. To this end, the effects of radiation on a target system need to be investigated from the early design phases, and appropriate mitigation measures should be applied to ensure that the system remains operational under all radiation conditions.

Single Event Transients (SETs) are one of the radiation-induced effects that has become highly critical for digital integrated circuits (ICs) designed in modern nanoscale CMOS technologies. A SET represents a voltage pulse caused by the passage of a single energetic particle (e.g., a heavy ion, neutron and proton) through a sensitive transistor in a combinational circuit. The SET voltage pulse is a direct consequence of the transient current resulting from the charge deposited in a device during the passage of an energetic particle. If a SET voltage pulse propagates through the circuit and is eventually captured by a storage element (e.g., a flip-flop), a soft error may occur. A soft error represents an unintentional change of state (bit-flip) in the storage elements, potentially resulting in computational errors and data corruption.

The technology scaling trends have led to an increase in the contribution of SETs to the total soft error rate (SER) of ICs. In order to accurately assess the impact of SETs, a wide range of radiation, design and operating parameters needs to be considered. The key parameters affecting the SET sensitivity of a circuit are the particle's linear energy transfer (LET), transistor size, supply voltage and temperature. The metrics for assessing the SET sensitivity are the critical charge (threshold LET) and SET pulse width. In general, the SET pulse width may span from tens of picoseconds to several nanoseconds. Particles with a higher LET induce more charge and generate longer SETs, which are more likely to propagate through the circuit and cause soft errors. With the scaling of transistor size and supply voltage with

every new technology generation, less deposited charge is necessary to cause SETs, i.e., the critical charge (threshold LET) decreases. For example, a particle with a LET of at least $15\,\mathrm{MeV{\cdot}cm^2{\cdot}mg^{-1}}$ may cause a SET in 250 nm technology, while a particle with a LET of only $2\,\mathrm{MeV{\cdot}cm^2{\cdot}mg^{-1}}$ is sufficient to cause a SET in sub-100-nm technologies.[1] Since the most abundant particles in space are those with LET $< 30\,\mathrm{MeV{\cdot}cm^2{\cdot}mg^{-1}}$, it is very likely that SETs would occur in an unprotected logic circuit. Furthermore, as transistor size scales and the distance between transistors reduces, a single particle may hit multiple transistors, potentially resulting in multiple soft errors. With clock frequencies in the GHz range, the probability that a SET will be latched by a storage element increases significantly. As demonstrated for the 40-nm technology node,[2] the SER of a combinational circuit may exceed the SER of a flip-flop chain at clock frequencies beyond 2 GHz. Moreover, the supply voltage and temperature variations may also have a significant contribution to the combinational SER. The analysis in Ref. 3 has shown that the temperature variation from -40°C to 125°C may cause a change of SER of combinational circuits by more than 20%, while the results in Ref. 4 have confirmed that minor fluctuations in supply voltage may cause over 150% variation in SER.

However, not every gate in a combinational circuit is critical. Because of the electrical, logical and temporal masking effects, which are inherent in combinational circuits, only a fraction of the logic gates in any circuit may potentially result in soft errors. Typically, around 50% of gates in a complex design contribute to over 80% of soft errors.[5] Therefore, applying traditional redundancy-based hardening techniques, such as the Triple Modular Redundancy, would usually not be cost-effective for combinational circuits due to their large area and power overhead. A widely used approach for reducing the combinational SER is based on selective hardening of the most sensitive gates.[6] Such an approach cannot eliminate all possible SETs, but it can significantly reduce the SER, with acceptable area, power and performance penalties.

For selective hardening of combinational logic, it is important to consider the SET sensitivity of individual logic cells. This is particularly important for designs based on standard non-rad-hard libraries. The hardening of individual standard cells can be performed by redesign of the cell's structure, replacement of a sensitive cell with a less sensitive one or an alternative logic implementation, or by connecting redundant elements to the cell's output. The aim of the applied mitigation measures is to reduce the SET generation probability by increasing the critical charge (threshold LET) of sensitive nodes, and to reduce the probability of SET propagation by attenuating or filtering the SET pulses. The two most widely used approaches for SET mitigation are the gate upsizing and the insertion of dedicated SET filters in logic paths.

In our previous work,[7] we have shown for the first time that the standard delay cells (SDCs) based on skew-sized inverters are more sensitive to SETs than other standard cells, because the particle strikes in the skew-sized transistors may result in SETs longer than 1 ns. As the SDCs are essential components of modern ICs, it is

important to ensure their SET robustness. We have proposed two designs based on hardware duplication, both of which can significantly improve the SET robustness of the cells, but with significant area overhead.[7] In this work, we explore an alternative SDC design based on inverters and decoupling capacitors. The proposed solution has higher SET robustness than the design with skew-sized inverters, and occupies less area than the duplication-based solutions from Ref. 7.

This work is an extension of our paper published at the 30th International Conference on Microelectronics (MIEL 2021).[8] In Ref. 8, we have analyzed the propagation delay and SET robustness of the proposed SDC based on decoupling capacitors. Delay cells based on decoupling capacitors are used in digital designs for providing fixed or variable delay.[9–11] However, to our best knowledge, the SET sensitivity of delay cells with decoupling capacitors has not been previously investigated. The analysis in Ref. 8 was done for different transistor sizes and LET of $60\,\mathrm{MeV{\cdot}cm^2{\cdot}mg^{-1}}$. This work extends our previous work[8] by introducing the following original contributions:

- Analysis of the power-delay trade-off dependence on the transistor size of the proposed SDC. It was shown that a cell with a larger propagation delay has a smaller power consumption.
- Analysis of the impact of supply voltage and temperature on the propagation delay of the proposed SDC. It was shown that supply voltage variations cause greater change in propagation delay than temperature.
- Analysis of the impact of LET, supply voltage and temperature on the width of the SET pulse generated at the output of the proposed SDC. It was shown that the maximum SET pulse width is below 600 ps for the investigated simulation conditions, whereas supply voltage variations have a stronger impact on SET pulse width than temperature.
- Analysis of the impact of transistor size, supply voltage and temperature on the width of SET pulse propagating through the proposed SDC. It was shown that the proposed SDC can filter the SETs shorter than 250 ps. With only six transistors and two sensitive nodes, the SET filtering capacity of the proposed SDC is comparable to other common SET filters.
- Comparison with other standard combinational cells. It was shown that the robustness of the proposed SDC for SETs is better than most commonly used standard combinational cells.

The rest of the paper is organized as follows. Section 2 discusses the related work. The SDC based on decoupling capacitors is introduced in Sec. 3. The simulation analysis of the propagation delay of the proposed delay cell is presented in Sec. 4. In Sec. 5, the SET robustness of the proposed delay cell is analyzed. Section 6 discusses the design considerations for the proposed delay cell.

In Sec. 7, the proposed delay cell is compared with alternative designs and other standard cells.

2. Related Work

SDCs are designed as a chain of an even number of inverters, where the propagation delay is directly proportional to the number of inverters. In order to obtain the required propagation delay with the minimum cell area (minimum number of inverters), some inverters in the chain are skew-sized. The skew sizing means that the channel width and length are chosen such that one edge (low-to-high or high-to-low) is faster than the other edge. With appropriate channel width and length, the skew-sized inverters may have a larger propagation delay than standard inverters.

The analysis of the SET sensitivity of SDCs with skew-sized inverters was done in our previous work,[7] using the standard cells from the IHP's 130-nm library as a case study. We denote an SDC based on skew-sized inverters as SDC_SKEW. A schematic of a SDC_SKEW cell with four inverters is illustrated in Fig. 1. The second and third inverters are skew-sized, while the first and last inverters have standard sizes (the p-type MOS (PMOS) transistor has a twice larger channel width than the n-type MOS (NMOS) transistor). In Table 1, the transistor sizes for SDC_SKEW cells with the propagation delays of 500 ps and 1.5 ns, available in the IHP's 130-nm library, are given.

The IHP's 130-nm technology is commercially available and has been used for the development of commercial rad-hard ICs for space applications.[12–15] The standard digital cells in this technology are tolerant to Total Ionizing Dose (TID) up to 50 krad, and up to 200 krad when the Enclosed Layout Transistors (ELTs) are applied.[16] No Single Event Latchup (SEL) was detected up to LET of 67 MeV·cm^2·mg^{-1}.[16] Compared to sub-100-nm technologies, the 130-nm technology provides better radiation hardness due to larger transistor sizes. In addition, the 130-nm technology is a part of IHP's SiGe BiCMOS platform, which offers unique

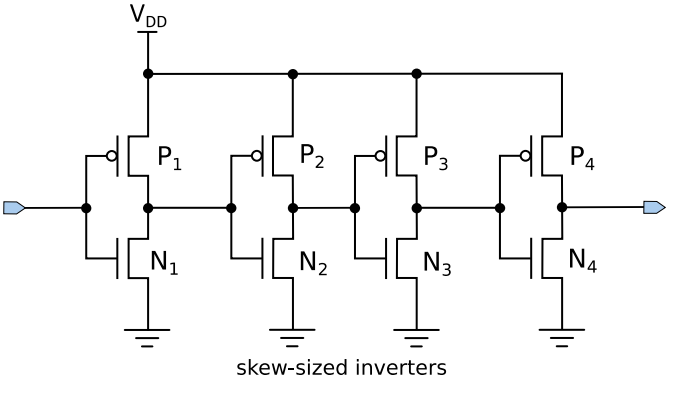

Fig. 1. SDC with skew-sized inverters (SDC_SKEW).

Table 1. Transistor sizes for SDC_SKEW cell in IHPs 130-nm technology.

	Channel width (W) and length (L)	
Transistor	Propagation delay = 500 ps	Propagation delay = 1.5 ns
P1	$W = 0.46\,\mu$m, $L = 0.13\,\mu$m	$W = 0.46\,\mu$m, $L = 0.13\,\mu$m
N1	$W = 0.3\,\mu$m, $L = 0.13\,\mu$m	$W = 0.3\,\mu$m, $L = 0.13\,\mu$m
P2	$W = 1.27\,\mu$m, $L = 0.7\,\mu$m	$W = 1.29\,\mu$m, $L = 1.25\,\mu$m
N2	$W = 0.84\,\mu$m, $L = 0.7\,\mu$m	$W = 0.7\,\mu$m, $L = 1.55\,\mu$m
P3	$W = 1.1\,\mu$m, $L = 0.6\,\mu$m	$W = 1\,\mu$m, $L = 1.55\,\mu$m
N3	$W = 0.84\,\mu$m, $L = 0.5\,\mu$m	$W = 0.84\,\mu$m, $L = 1.2\,\mu$m
P4	$W = 1.29\,\mu$m, $L = 0.13\,\mu$m	$W = 1.29\,\mu$m, $L = 0.13\,\mu$m
N4	$W = 0.84\,\mu$m, $L = 0.13\,\mu$m	$W = 0.84\,\mu$m, $L = 0.13\,\mu$m

advantages of combining bipolar and MOS technologies. Specifically, this technology offers the fastest bipolar transistors in the world, with a cut-off frequency up to 700 GHz,[17] which is crucial in the design of high-performance mixed-signal ICs.

The SET sensitivity of SDCs based on skew-sized inverters has been investigated in our previous work[7] with the standard current injection approach in SPICE simulations. For this purpose, a bias-dependent current model from Kauppila *et al.*[18] was employed to inject the current pulses into the sensitive nodes of the cell. The results in Ref. 7 show that the SETs induced in SDC_SKEW may be at least 100 ps longer than those in other combinational cells, and when the size of the skew-sized inverters is increased, the SET pulse may be longer than 1 ns. Such long SETs are attributed to the pulse stretching effect of the skew-sized inverters. In addition, we have shown that the SDC_SKEW cell is sensitive to supply voltage and temperature variations. Namely, for the corner cases (1.08 V, 125°C) and (1.32 V, −40°C), the SET pulse width may vary by 50–600 ps compared to a typical case (1.2 V, 27°C), and the impact of supply voltage and temperature variations is more pronounced for cells with a larger driving strength.

In order to reduce the sensitivity of SDC_SKEW cells to SETs, we have proposed two solutions based on redundancy.[7] The first approach employs complete duplication with a guard gate (SDC_CD), i.e., all inverters in the delay cell are duplicated and connected to a four-transistor guard gate,[19,20] as depicted in Fig. 2. Because the output of the guard gate changes only when both inputs change, a SET pulse induced in any inverter will not propagate to the output. As the guard gate has an inverting function, an additional inverter is connected to the output of the guard gate. Since the whole cell is duplicated, this approach can be applied to an existing SDC without modifying its structure. The second approach (Fig. 3) employs partial duplication with a guard gate (SDC_PD), i.e., only the skew-sized transistors are duplicated, and connected to a guard gate with an additional inverter. Thus, all SETs generated in the skew-sized inverters will be masked. In this case, the internal structure of the delay cell needs to be modified, which requires more design and characterization effort.

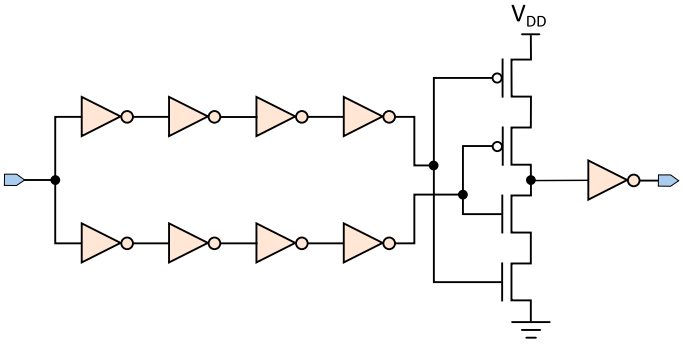

Fig. 2. SDC with complete duplication (SDC_CD).

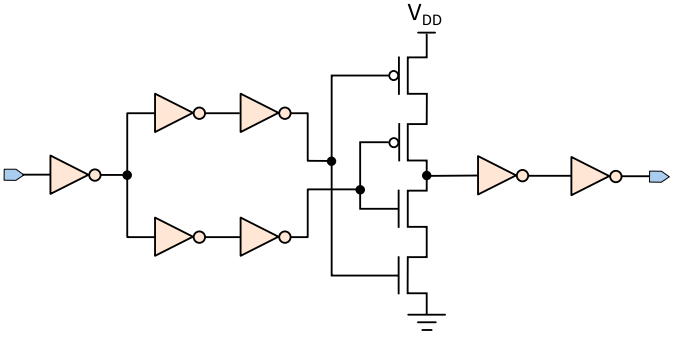

Fig. 3. SDC with partial duplication (SDC_PD).

Both approaches have been shown to eliminate the SETs in the skew-sized inverters. However, the added guard gate and inverter are additional sensitive nodes, and the SET pulse widths in these nodes are comparable to that in other standard cells. It is important to note that the duplication results in a significant area overhead at the cell level, i.e., over 85% for SDC_PD and over 120% for SDC_CD.

3. Standard Delay Cell with Decoupling Capacitors (SDC_DECAP)

As an alternative to the SDCs based on skew-sized inverters, and the proposed configurations based on partial and complete duplication, we have investigated a delay cell with decoupling capacitors. We denote an SDC with decoupling capacitors as SDC_DECAP. The SDC_DECAP is composed of two standard CMOS inverters and two decoupling capacitors (DECAPs) connected between the output of the first inverter and the supply rails, as illustrated in Fig. 4. The decoupling capacitors are constructed from PMOS and NMOS transistors, by connecting the drain, source and bulk to one terminal, while the gate is connected to another terminal.

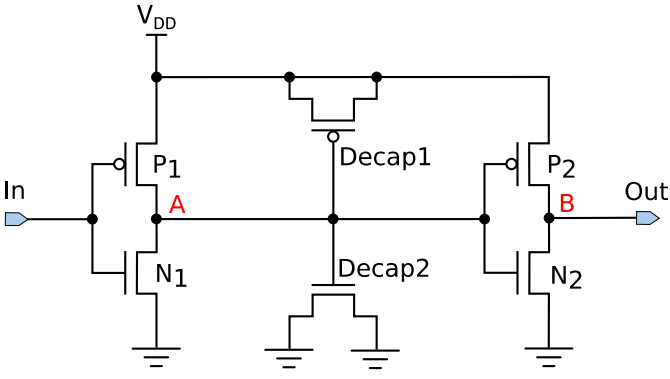

Fig. 4. Standard delay cell with decoupling capacitors (SDC_DECAP).

The propagation delay of SDC_DECAP cell is proportional to the size (driving strength) of input and output inverters, and the capacitance of decoupling capacitors C_{DECAP}. The decoupling capacitance is proportional to the transistor size (channel width and length), according to the relation,[21]

$$C_{\mathrm{DECAP}} = C_{\mathrm{OX}} \cdot W \cdot L + 2 \cdot C_{\mathrm{OL}} \cdot W, \tag{1}$$

where C_{OX} is the oxide capacitance per unit area, C_{OL} is the overlap and fringing capacitance per unit width of the device, W is the channel width of transistor and L is the channel length of transistor.

In the design depicted in Fig. 4, only the inverters are sensitive to particle strikes. The decoupling capacitors are not sensitive to particle strikes because their drain and source terminals are connected directly to supply and ground lines, and thus particle-induced current would be immediately drawn away through the supply and ground lines. In general, the off-state transistors are most sensitive to particle strikes due to the reverse-biased *pn* junctions. Therefore, only two transistors, i.e., one transistor in each inverter, will be potentially sensitive to SETs. As the drain is most sensitive to particle strikes, there are only two sensitive nodes, denoted as A and B.

4. Propagation Delay of SDC_DECAP

In this section, the impact of design and operating settings on the propagation delay of SDC_DECAP is analyzed. The section is divided into two subsections. Section 4.1 presents the simulation setup, while the results are discussed in Sec. 4.2.

4.1. *Simulation setup*

Using a commercial Cadence Spectre simulator, we have conducted a series of electrical simulations in order to investigate the dependence of the propagation delay of SDC_DECAP on the size of inverters and decoupling capacitors, supply voltage and

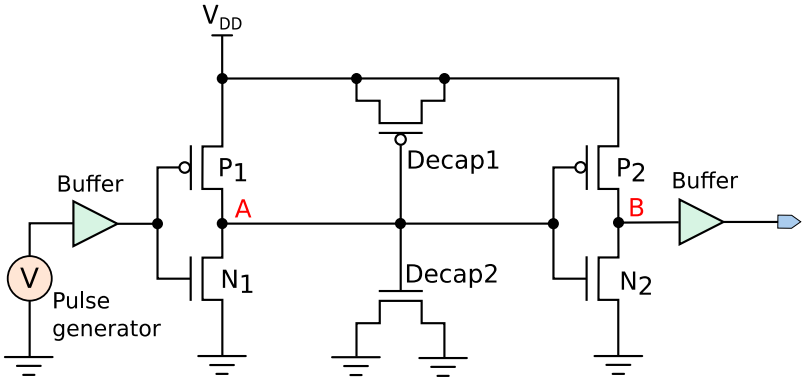

Fig. 5. Setup for simulation of propagation delay.

temperature. In addition, the relation between propagation delay and power consumption was analyzed. The simulation setup is depicted in Fig. 5. The input pulse width was set to 1 ns using a voltage pulse generator. A standard buffer was connected between the pulse generator and the input of the delay cell, and also at the output of the delay cell. The propagation delay was determined as the time interval between the rising edge of pulse at the input of the driving buffer and the rising edge of pulse at the output of the load buffer, at the level of half of the supply voltage. It is important to note that the obtained results for propagation delay are slightly different from those published in our previous work[8] because of different buffer designs. As a case study, we have done the analysis for the IHP's 130-nm bulk CMOS technology.

The transistor sizes for inverters and decoupling capacitors have been defined by varying the channel width of respective transistors. The inverters with driving strengths x1 and x2 have been used, where x2 inverters have twice larger channel widths than x1 inverters, while x1 inverters have four times larger channel widths than the standard x1 inverters in the investigated 130-nm library. For decoupling capacitors, the channel length was fixed to 1 μm, while the channel width was varied from 2 μm to 12 μm. The supply voltage was varied from 0.8 V (minimum supply voltage for the investigated technology) to 1.2 V (nominal supply voltage for the investigated technology), while the temperature was varied from -40°C to 125°C.

4.2. *Results and discussion*

Figure 6 shows the dependence of the propagation delay on the channel width of decoupling capacitors, for x1 and x2 inverters, and for positive and negative input pulses. It can be seen that the propagation delay increases linearly with the size of decoupling capacitors, which is in good agreement with relation (1). On the other hand, the increase in the size of the inverter leads to a decrease in the propagation delay. For the channel width from 2 μm to 12 μm for decoupling capacitors, and

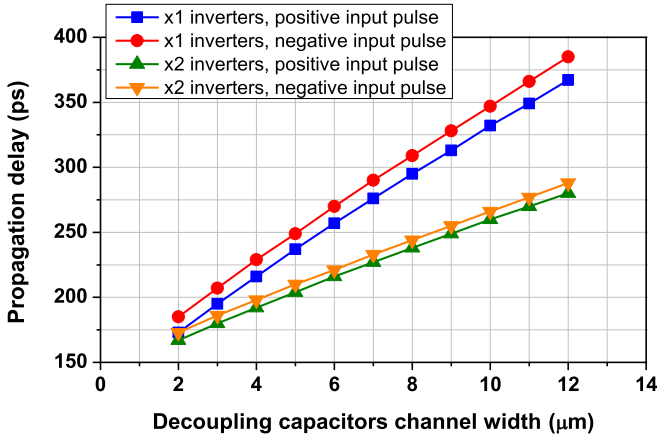

Fig. 6. Propagation delay as a function of decoupling capacitors channel width, for x1 and x2 inverters, and positive and negative input pulses.

positive input pulse, the propagation delay is from 173 ps to 367 ps with x1 inverters, and from 167 ps to 280 ps. Similar results are obtained if the channel length is varied, while the channel width is kept constant. Larger propagation delay can be obtained by increasing both channel width and length, but that was not analyzed in this study. The difference in the propagation delay for positive and negative input pulses is minor, and hence only the results for positive input pulse are discussed in the following.

In Fig. 7, the relation between the average power consumption and the propagation delay, in terms of transistor size, is illustrated. The results have been obtained for SDC_DECAP with x1 inverters and a nominal supply voltage of 1.2 V. As the

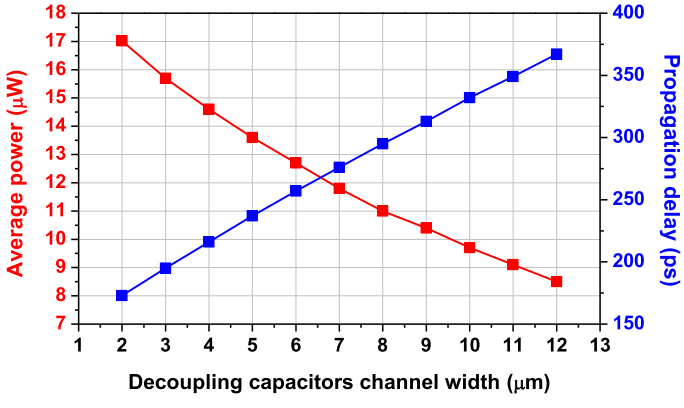

Fig. 7. Average power consumption and propagation delay as a function of decoupling capacitors channel width, for x1 inverters and supply voltage of 1.2 V.

main function of SDC_DECAP is to provide a given delay in a logic path, it is desirable to have minimum power consumption for a particular delay. The results in Fig. 7 show that the average power consumption decreases as the size of decoupling capacitors increases. Therefore, the cells with a larger propagation delay will have a smaller power consumption, but this comes at the cost of increased area.

The dependence of propagation delay on channel width of decoupling capacitors, for different supply voltages and temperature of 27°C, is illustrated in Fig. 8. As can be observed, the decrease in supply voltage leads to a significant increase in the propagation delay. For a given size of decoupling capacitors, the propagation delay increases linearly with the decrease in supply voltage, and the impact of supply voltage is more pronounced for larger decoupling capacitors. For decoupling cells with a channel width of 2 μm, the propagation delay increases for 266 ps (from 178 ps to 444 ps) when supply voltage decreases from 1.2 V to 0.8 V. On the other hand, for decoupling cells with channel width of 12 μm, the propagation delay increases by 496 ps (from 370 ps to 866 ps) when the supply voltage decreases from 1.2 V to 0.8 V.

Figure 9 depicts the variation of propagation delay in terms of channel width of decoupling capacitors, for different temperatures and a nominal supply voltage of 1.2 V. As the temperature increases from −40°C to 125°C, the propagation delay also increases, and the impact of temperature becomes more significant when the size of decoupling capacitors is increased. However, comparing the results in Fig. 8 shows that the impact of temperature is weaker than that of supply voltage. Namely, the propagation delay varies by a maximum of 40 ps over the investigated temperature range.

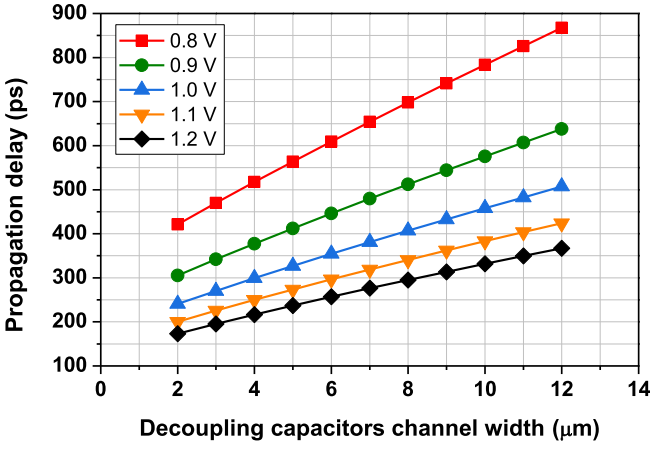

Fig. 8. Propagation delay as a function of decoupling capacitors channel width and supply voltage, for x1 inverters.

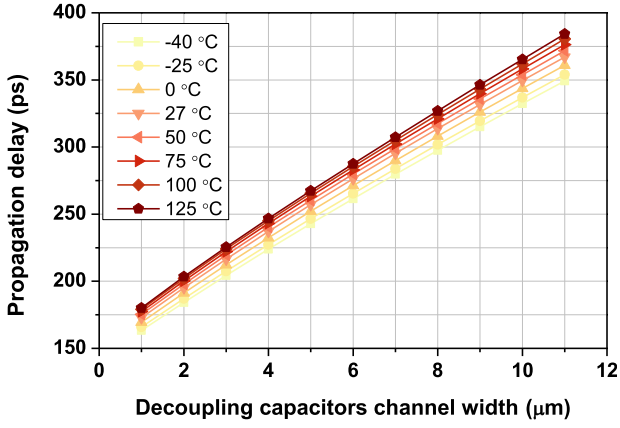

Fig. 9. Propagation delay as a function of decoupling capacitors channel width and temperature, for x1 inverters.

5. SET Robustness of SDC_DECAP

In this section, the SET robustness of SDC_DECAP in terms of design, operating and irradiation parameters is analyzed. The analysis is divided in two sections. Section 5.1 presents the analysis of the SET generation in SDC_DECAP, i.e., the sensitivity of SDC_DECAP to direct particle strikes. In Sec. 5.2, the SET propagation through SDC_DECAP, i.e., the ability of SDC_DECAP to attenuate the SET pulses arriving at its input, is analyzed.

5.1. *SET generation analysis*

5.1.1. *Simulation setup*

For the simulation of SET generation in SDC_DECAP cell, we have employed a standard current injection approach in Cadence Spectre simulations. The corresponding simulation setup is illustrated in Fig. 10. A fixed voltage level was set at the input of the delay cell through a minimum-sized driving buffer, and a buffer of the same size was used as a load buffer. A bias-dependent current source from Ref. 18 was employed to inject the current pulses successively into the two sensitive nodes (A and B) of SDC_DECAP. The current source was connected between the respective node and the ground terminal, and the direction of current flow was chosen in accordance with the voltage level across the node. The rise and fall time parameters of the current pulse were 10 ps and 100 ps, respectively. These values allow for reproducing the average SET pulse width for 130-nm technology, and they have been chosen based on the comparison of experimental results reported in Ref. 22 and our simulation results in Ref. 23. Due to the difference in buffer designs, there is a slight difference in the obtained results with respect to those presented in our previous work.[8] It is important to note that the rise and fall time parameters are actually

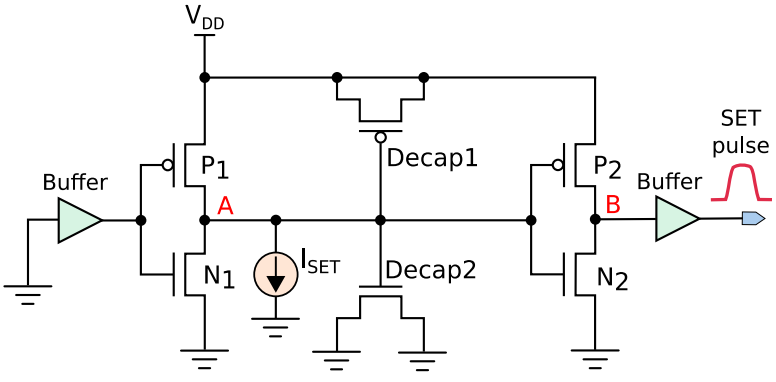

Fig. 10. Setup for simulation of SET generation.

variable, and they depend on technology and the strike profile (LET, angle of incidence, strike locations). Thus, for a real radiation environment, a distribution of SET pulses, i.e., a distribution of rise and fall time parameters, needs to be considered.

The SET generation was assessed in terms of two metrics: (i) threshold Linear Energy Transfer (LET_{TH}) and (ii) width of SET pulse generated at the output of delay cell. The value of LET_{TH} was obtained as the minimum LET which causes a SET pulse with amplitude beyond the half of supply voltage at the output of load buffer. To obtain the LET_{TH}, the value of LET was gradually increased during simulations, and for each value, the corresponding SET pulse width was observed. Similarly as for propagation delay analysis, the SET robustness metrics have been analyzed in terms of the size of decoupling capacitors and inverters, supply voltage and temperature.

5.1.2. *Results and discussion*

The LET_{TH} for node A (first inverter) and node B (second inverter), as a function of the size of decoupling cells, for two driving strengths of inverters (x1 and x2), is shown in Fig. 11. The LET_{TH} for node A increases almost linearly with the size of inverters and decoupling capacitors. By increasing the size of inverters and decoupling capacitors, the driving strength and total node capacitance increase, allowing faster dissipation of induced charge.[24] The LET_{TH} for node B also increases when the inverter is upsized (not shown here), while decoupling capacitors have no impact (as shown in Fig. 11).

The impact of LET and transistor sizes on SET pulse width is illustrated in Figs. 12 and 13. In Fig. 12, the SET pulse width as a function of LET, when the current pulse is injected successively in nodes A and B, for x1 and x2 inverters, and for decoupling capacitors with a channel width of 2 μm, is shown. In Fig. 13, the dependence of the SET pulse width on the size of decoupling capacitors and

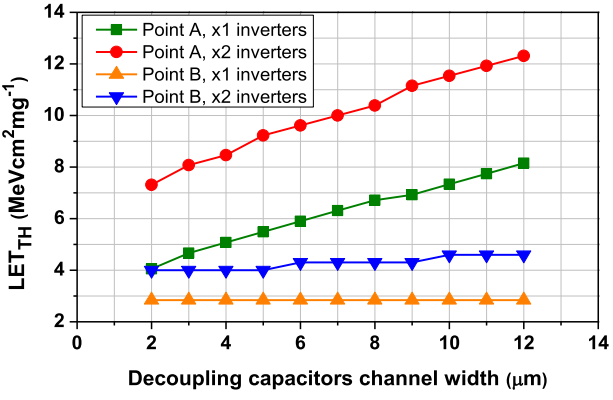

Fig. 11. Threshold LET as a function of decoupling capacitors channel width, for x1 and x2 inverters.

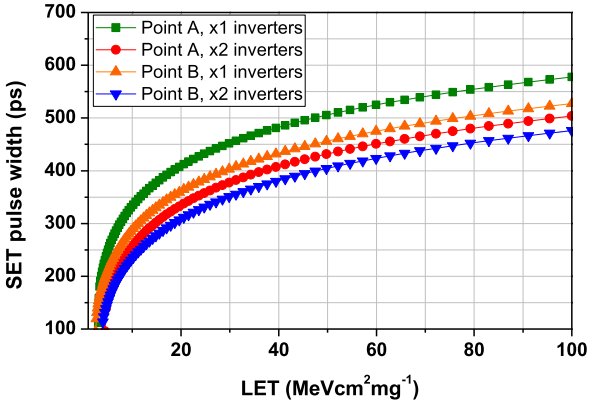

Fig. 12. SET pulse width as a function of LET, for x1 and x2 inverters and decoupling capacitors with channel width of 2 μm.

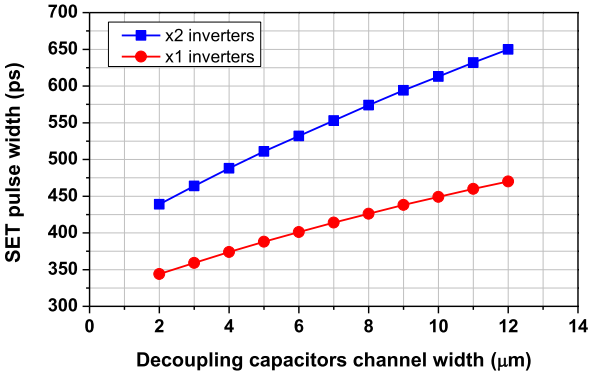

Fig. 13. SET pulse width as a function of decoupling capacitors channel width, for x1 and x2 inverters, when the current pulse with LET = 30 MeV·cm^2·mg^{-1} is injected in first inverter (node A).

inverters, when the current pulse with LET of 30 MeV·cm^2·mg^{-1} is injected in node A, is illustrated.

The SET pulse width in all cases increases with LET because the deposited charge is proportional to LET. For the same load capacitance across a given node (A or B), the SET pulse width due to strikes in x2 inverter is shorter than that for x1 inverter, because larger inverters are more robust to particle hits. However, increasing the size of decoupling capacitors across node A leads to an almost linear increase in the SET pulse width. This is due to the fact that larger load capacitance needs more time for charging/discharging when an amount of charge greater than the critical charge (LET_{TH}) is deposited, i.e., more time is needed to draw away a larger amount of charge induced by high-LET particles.[25] As a result of this phenomenon, node A with x2 inverter has the largest LET_{TH} but the corresponding pulse width is not the least.

Figure 14 illustrates the variation of SET pulse width as a function of the size of decoupling capacitors, for x1 inverters and different supply voltages, when the current pulse is injected in node A. As the supply voltage increases, the SET pulse width decreases. By increasing the supply voltage, the transistor's driving current is increased, allowing faster dissipation of particle-induced current, and consequently resulting in shorter SETs. It can be seen that the impact of supply voltage is more significant for larger decoupling capacitors. For instance, for decoupling cells with a 2 μm channel width, the SET pulse width change is around 300 ps over the analyzed supply voltage range. For the same supply voltage range, the change in SET pulse width is almost 500 ps for decoupling capacitors with 12 μm channel width.

In Fig. 15, the impact of temperature on the dependence between SET pulse width and the size of decoupling capacitors is depicted. As can be observed, the temperature variations cause a minor change in the SET pulse width for a given size of decoupling capacitors, and the impact of temperature slightly increases with the

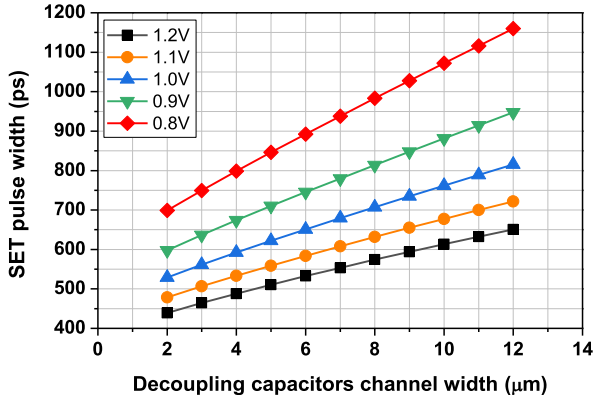

Fig. 14. SET pulse width as a function of decoupling capacitors channel width, for different supply voltages and x1 inverters, when the current pulse with LET = 30 MeV·cm^2·mg^{-1} is injected in first inverter (node A).

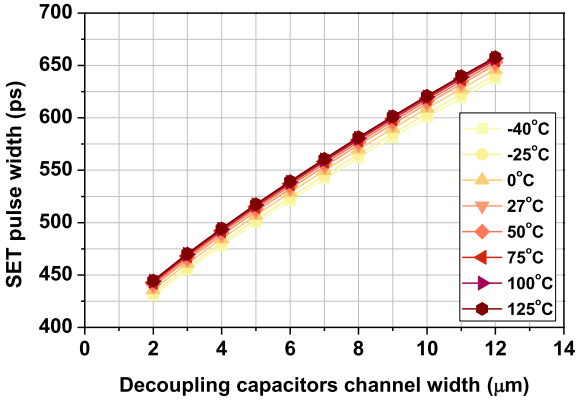

Fig. 15. SET pulse width as a function of decoupling capacitors channel width, for different temperatures and x1 inverters, when the current pulse with LET = 30 MeV·cm^2·mg^{-1} is injected in first inverter (node A).

increase in the size of decoupling cells. Overall, the SET pulse width changes by a maximum of 50 ps over the investigated temperature range, which is a 10-fold smaller change compared to that resulting from the supply voltage variations. Note that the temperature has a similar impact on the propagation delay (Fig. 9).

The dependence of SET pulse width on the size of decoupling capacitors, for different supply voltages and temperatures, when the current pulse is injected into node B, is illustrated in Figs. 16 and 17. In this case, the size of decoupling capacitors does not affect the SET pulse width. However, the SET pulse width increases with the decrease of supply voltage or increase of temperature. Similarly, as in the case of current injection in node A, the supply voltage variations lead to a greater change in

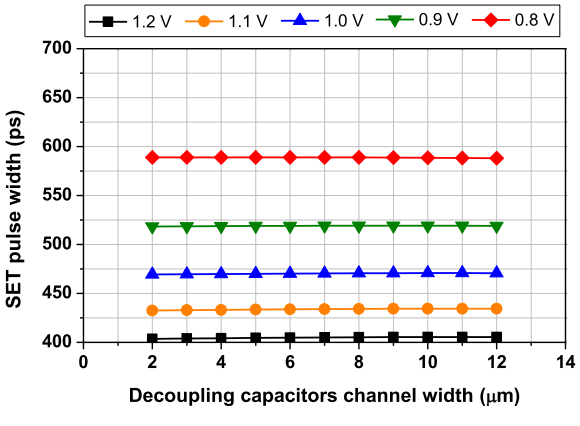

Fig. 16. SET pulse width as a function of decoupling capacitors channel width, for different supply voltages and x1 inverters, when the current pulse with LET = 30 MeV·cm^2·mg^{-1} is injected in second inverter (node B).

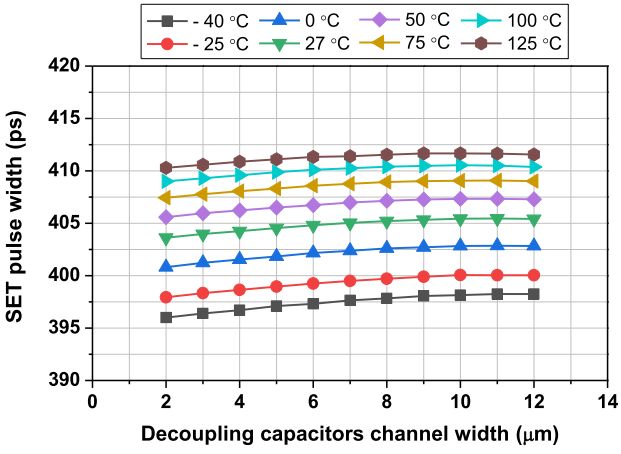

Fig. 17. SET pulse width as a function of decoupling capacitors channel width, for different temperatures and x1 inverters, when the current pulse with LET = 30 MeV·cm^2·mg^{-1} is injected in second inverter (node B).

SET pulse width than the temperature variations. Over the investigated supply voltage range, the SET pulse width varies by almost 200 ps. On the other side, the investigated temperature variations cause the variation in SET pulse width of around 20 ps.

5.2. *SET propagation analysis*

5.2.1. *Simulation setup*

For the simulation of SET propagation through the proposed SDC, the same setup as for the analysis of propagation delay was employed. The only difference is that the input pulse width was varied, and the range of input pulse width was in the order of tens to hundreds of picoseconds, which corresponds well to the real SET pulse widths.

Two metrics have been used to assess the SET filtering capacity of the proposed SDC: (i) filtered SET pulse width and (b) filtering window. The filtered SET pulse width is the maximum input SET pulse width that can be electrically masked, where a pulse is considered to be masked if its amplitude after propagation through the cell is reduced below the half of supply voltage. The filtering window is the difference between the propagation delay of the cell and the filtered pulse width, and it is an important metric to evaluate the trade-off between the benefit in terms of SET masking and the introduced delay overhead. Ideally, the filtering window should be as small as possible.

5.2.2. *Results and discussion*

Figure 18 illustrates the filtered SET pulse width and the filtering window as a function of the decoupling capacitor channel width. The simulations have been done

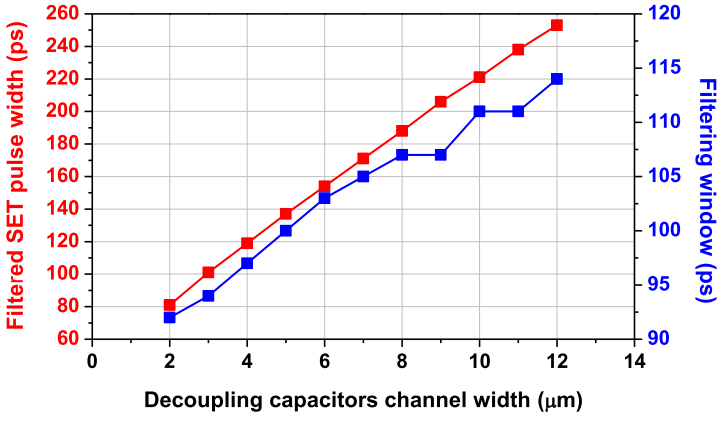

Fig. 18. Filtered SET pulse width and filtering window as a function of decoupling cells channel width.

for a supply voltage of 1.2 V and a temperature of 27°C. The values of both metrics increase linearly with the decoupling cell channel width. With the maximum investigated channel width of 12 μm, the delay cell can filter the SET pulse shorter than 250 ps. This indicates that the proposed SDC could be used for filtering short SETs in combinational paths. Note that the short SETs are induced by low-LET particles, which are most abundant in space. The filtered SET pulse width is directly determined by the propagation delay of the cell, because the propagation delay defines the minimum pulse width that can propagate through a cell. However, the increase in the filtering window with decoupling cell sizes indicates that the delay overhead would be larger when filtering longer SET pulses, which is not a desirable feature.

The dependence of filtered SET pulse width on supply voltage and temperature is similar to that observed for the propagation delay. As the supply voltage decreases from 1.2 V to 0.8 V, the width of the SET pulse that can be filtered increases by at least 100 ps, where the filtered SET pulse width is larger as the decoupling capacitor's size increases. On the other hand, the increase in temperature from −40°C to 125°C results in an increase in the filtered SET pulse width by at least 15 ps, and for larger decoupling cells, the increase in the filtered SET pulse width is larger.

In order to increase the SET pulse width that can be filtered with the proposed SDC, two approaches could be adopted. The first option is to cascade multiple cells, resulting in a linear increase in the filtered SET pulse width. The second approach is to redesign the cell by implementing more decoupling cells. The second approach retains the minimum number of sensitive nodes, since only the inverters will be sensitive. However, both approaches also lead to a linear increase in the propagation delay.

6. Design Considerations

Based on the simulation results presented in previous sections, the qualitative impact of the investigated parameters on the propagation delay and SET robustness of

Table 2. Impact of various parameters on propagation delay and SET robustness of SDC_DECAP.

Parameter variation (for nominal values of other parameters)	Impact on propagation delay	Impact on generated SET pulse width	Impact on threshold LET	Impact on filtered SET pulse width
Channel width of decoupling cells increases from 2 μm to 12 μm	Increases	Increases (for strike in node A) No impact (for strike in node B)	Increases (for strike in node A) No impact (for strike in node B)	Increases
Driving strength of inverters increases from x1 and x2	Decreases	Decreases	Increases	Decreases
LET increases from 1 MeV·cm^2·mg^{-1} to 60 MeV·cm^2·mg^{-1}	No impact	Increases	—	—
Supply voltage increases from 0.8 V to 1.2 V	Decreases	Decreases	Increases	Decreases
Temperature increases from -40°C to 125°C	Increases	Increases	Decreases	Increases

SDC_DECAP cell can be summarized as given in Table 2. The upsizing of inverters and decoupling capacitors increases the threshold LET, providing immunity to low-LET particle strikes. However, the SET pulse width due to strikes in the first inverter increases with the size of decoupling cells, but decreases with the size of inverters. In other words, SDC_DECAP cells would be more sensitive to high-LET particles. Though, it is important to note that since the low-LET particles are most abundant in the space environment, the protection from low-LET particles is crucial. On the other hand, the upsizing of inverters decreases the propagation delay, while the upsizing of decoupling capacitors increases the propagation delay. The increase in propagation delay is reflected in better SET filtering capability of the delay cell. Thus, SDC_DECAP with a larger propagation delay is more beneficial for SET filtering.

The increase in the supply voltage leads to a decrease in the propagation delay and an increase in the SET robustness (threshold LET increases, while SET pulse width decreases). The temperature increase leads to an increase in propagation delay and a decrease in SET robustness (threshold LET decreases, while SET pulse width increases). Overall, the impact of supply voltage variations is more critical for both propagation delay and SET robustness.

Thus, the design of SDC_DECAP cells for a radiation environment requires a compromise between the propagation delay and the SET robustness. As the size of inverters and decoupling capacitors has opposite impact on propagation delay and SET sensitivity, a trade-off in terms of transistor sizing is the most important design criterion. An optimal design of SDC_DECAP cell would be to have a small propagation delay per cell, because in that case the SET pulse width due to a particle strike would be shorter. The larger propagation delay could be achieved by cascading

multiple delay cells. For example, with x2 inverters and propagation delay of 200 ps, the SET pulse width at LET of 60 MeV·cm^2·mg^{-1} would be less than 550 ps, which could be filtered with conventional SET filtering logic.

7. Comparative Analysis

This section gives a brief comparison of the proposed SDC_DECAP design with alternative delay cells, SET filters and most common standard combinational cells.

7.1. *Comparison with alternative delay cell implementations*

In order to assess the SET robustness of the proposed SDC_DECAP cell with respect to alternative delay cells, a comparison with the SDC based on skew-sized inverters (SDC_SKEW) and two variants of SDC_SKEW cell based on duplication (SDC_PD and SDC_CD), has been performed. The results are presented in Tables 3 and 4. Table 3 shows the total number of transistors and the number of sensitive transistors for each design. In Table 4, the threshold LET and SET pulse width for most sensitive and most robust nodes in each SDC are compared. For the sake of fair comparison, all four SDC implementations have been designed to have approximately the same propagation delay.

The main advantages of SDC_DECAP over SDC_SKEW and SDC_PD are fewer sensitive transistors (only two) and better SET robustness (higher LET_{TH} and shorter SET pulse width). SDC_DECAP and SDC_CD have the same number of sensitive transistors (two), but due to different sizing, SDC_DECAP is more robust

Table 3. Comparison of number of sensitive nodes and number of transistors for SDC_DECAP and alternative delay cell implementations.

SDC variant	No. of sensitive nodes	No. of transistors per cell
SDC_SKEW	4	8
SDC_PD	4	18
SDC_CD	2	22
SDC_DECAP	2	6

Table 4. Comparison of SET robustness of four SDC implementations (SET pulse width results are obtained for LET = 60 MeV·cm^2·mg^{-1}).

	LET_{TH} (MeV·cm^2·mg^{-1})		SET pulse width (ps)	
SDC variant	Most robust node	Most sensitive node	Most sensitive node	Most robust node
SDC_SKEW	1.2	0.4	756	452
SDC_PD	1.21	0.8	634	486
SDC_CD	1.21	0.76	621	455
SDC_DECAP	17.41	1.25	597	423

to SETs. Note that SDC_DECAP cell has a total of 6 transistors, while SDC_SKEW, SDC_PD and SDC_CD cells have 8, 18 and 22 transistors, respectively. This indicates that the proposed SDC_DECAP design would be the best solution in terms of area and power consumption saving. By comparing the results for SDC_DECAP presented in previous sections with those for SDC_SKEW presented in our previous work,[7] it can be observed that the SDC_DECAP design is more robust to supply voltage and temperature variations. The main reason for this is the high sensitivity of skew-sized inverters to supply voltage and temperature variations.

7.2. *Comparison with alternative SET filters*

To evaluate the potential of SDC_DECAP as a SET filter, we have compared it with alternative SET filters, as given in Table 5. The most common SET filter used in rad-hard designs is based on a delay line and a guard gate,[19,20] where the delay line defines the filtered SET pulse width. Alternative SET filters reported in literature include transmission gates,[26,27] Schmitt trigger,[31,32] buffer,[28] cross-coupled inverters[29] and decoupling cells with cross-coupled transistors.[30] Since the SET masking capacity of each filter depends on transistor sizing, the comparison is done in terms of the number of transistors and the number of sensitive nodes. The filters with fewer transistors are preferable, in order to minimize the area overhead. In addition, the filters should have the least possible number of sensitive nodes. Based on these criteria, it can be seen that the proposed SDC_DECAP design is comparable to alternative SET filters. It is important to mention that SDC_DECAP has less transistors than the filter based on delay line and guard gate, and the Schmitt trigger. More detailed analysis can be performed to compare the area, power and delay overhead introduced for each filter.

7.3. *Comparison with standard combinational cells*

Table 6 compares the proposed SDC with the most frequently used standard combinational cells, considering the number of transistors per cell, the number of transistors sensitive to SETs, and the SET pulse width when a current pulse with

Table 5. Comparison of number of sensitive nodes and number of transistors for SDC_DECAP and alternative SET filters.

SET filter	No. of sensitive nodes	No. of transistors per cell
Delay line and guard gate[19,20]	2	8 or more (depending on required delay)
Transmission gates[26,27]	—	4–8
Schmitt trigger[31,32]	2	10
Buffer[28]	2	4
Cross-coupled inverters[29]	2	4
Decoupling cells with cross-coupled transistors[30]	2	4
SDC_DECAP	2	6

Table 6. Comparison of SET sensitivity of SDC_DECAP and standard combinational cells.

Cell type	No. of transistors	No. of sensitive nodes	SET pulse width (ps) for LET = 60 MeV·cm^2·mg^{-1}
INV	2	1	570
BUF	4	2	572
NAND2	4	2	593
NOR2	4	2	678
AND2	6	3	573
OR2	6	3	570
XOR2	10	4	694
XNOR2	10	4	700
SDC_DECAP	6	2	545

LET of 60 MeV·cm^2·mg^{-1} is injected in the output of the cell. The standard cells with the minimum available size have been used in this analysis. For SDC_DECAP, the channel width of 2 μm for decoupling capacitors and inverter with x1 size have been used. As can be seen, with two sensitive nodes and SET pulse width of 545 ps, the SDC_DECAP cell has better SET robustness (shorter SET pulse width) than other investigated standard cells. This is due to the fact that the size of inverters in SDC_DECAP is larger than the transistor sizes in minimum-sized standard cells.

8. Conclusion

The SET sensitivity of an SDC implemented with two inverters and two decoupling capacitors is investigated in this paper. The electrical simulations have been performed to analyze the dependence of propagation delay and SET sensitivity (threshold LET, generated SET pulse width and propagated SET pulse width) on transistor size, supply voltage and temperature. It has been shown that the proposed design is more tolerant to SETs than the SDC realized with skew-sized inverters, and introduces negligible area overhead compared to the hardened delay cells based on partial and complete duplication with a guard gate. Based on the simulation results, it has been shown that an optimal design can be achieved by considering a trade-off between propagation delay and SET robustness. An important finding is that the proposed delay cell could be utilized for filtering short SETs in combinational paths, and it is a very good alternative to existing SET filters due to low transistor count. It is also important to note that the proposed delay cell is more tolerant to SETs than other common standard combinational cells designed in 130-nm bulk CMOS technology. The simulation results indicate that the supply voltage variations have stronger impact on propagation delay and SET robustness than temperature.

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References

1. P. E. Dodd, M. R. Shaneyfelt, J. A. Felix and J. R. Schwank, Production and propagation of single event transients in high-speed digital logic ICs, *IEEE Trans. Nucl. Sci.* **51** (2004) 3278–3284.
2. N. N. Mahatme *et al.*, Comparison of combinational and sequential error rates for a deep submicron process, *IEEE Trans. Nucl. Sci.* **58** (2011) 2719–2725.
3. S. Hsueh, R. Huang and C. Wen, TASSER: A temperature-aware statistical soft error rate analysis framework for combinational circuits, *Proc. Int. Symp. Quality Electronic Design (ISQED)*, Santa Clara, USA, 2014, pp. 539–534.
4. S. Kiamehr, M. Ebrahimi, F. Firouzi and M. Tahoori, Chip-level modeling and analysis of electrical masking of soft errors, *Proc. IEEE VLSI Test Symp. (VTS)*, Berkeley, USA, 2013, pp. 1–6.
5. V. Srinivasan *et al.*, Single-event mitigation in combinational logic using targeted data path hardening, *IEEE Trans. Nucl. Sci.* **52** (2005) 2516–2523.
6. C. G. Zoellin, H.-J. Wunderlich, I. Polian and B. Becker, Selective hardening in early design steps, *Proc. IEEE European Test Symp. (ETS)*, Verbania, Italy, 2008, pp. 185–190.
7. M. Andjelkovic, O. Schrape, A. Breitenreiter, M. Krstic and R. Kraemer, Characterization of SET effects in standard delay cells, *Proc. IEEE Int. Conf. Electronics, Circuits and Systems (ICECS)*, Glasgow, UK, 2020, pp. 1–4.
8. M. Andjelkovic *et al.*, Standard delay cells with improved tolerance to single event transients, *Proc. Int. Conf. Microelectronics (MIEL)*, Nis, Serbia, 2021, pp. 329–332.
9. P. Adreani, F. Bingogiari, R. Roncella, R. Saletti and P. Terreni, A digitally controlled shunt capacitor CMOS delay line, *Analog Integr. Circuits Signal Process.* **18** (1999) 89–96.
10. M. Maymandi-Nejad and M. Sachdev, A digitally programmable delay element: Design and analysis, *IEEE Trans. Very Large Scale Integr. Syst.* **11** (2003) 871–878.
11. M. A. Abbas, G. Russell and D. J. Kinniment, Built-in time measurement circuits – A comparative design study, *IET Comput. Digit. Tech.* **1** (2007) 87–97.
12. Space ethernet physical layer transceiver (SEPHY), www.sephy.eu.
13. Export-free Rad-hard microcontroller for space applications (MORAL), www.moral.eu.
14. Rad-hard 16 Mbit multi-chip module SRAM for space applications (EuroSRAM4Space), https://redcatdevices.eu/?page_id=211.
15. Rad-hard octal 500 Mbps Bus low-voltage differential signaling (LVDS) repeater for space applications, https://www.arquimea.com/aerospace-and-defence/ip-ic-products/.
16. A. Simevski, P. Skoncej, C. Calligaro and M. Krstic, Scalable and configurable multi-chip SRAM for space applications, *Proc. IEEE Int. Symp. Defect and Fault Tolerance in VLSI and Nanotechnology (DFT)*, Noordwijk, Netherlands, 2019, pp. 1–6.
17. B. Heinemann *et al.*, SiGe HBT with fx/fmax of 505 GHz/720 GHz, *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, USA, 2016, pp. 3.1.1–3.1.4.
18. J. S. Kauppila *et al.*, A bias-dependent single-event compact model implemented into BSIM4 and a 90 nm CMOS process design kit, *IEEE Trans. Nucl. Sci.* **56** (2009) 3152–3157.

19. A. Balasubramanian, B. L. Bhuva, J. D. Black and L. W. Massengill, RHBD techniques for mitigating effects on single-event hits using guard-gates, *IEEE Trans. Nucl. Sci.* **52** (2005) 2531–2535.
20. R. L. Shuler *et al.*, The effectiveness of TAG or guard-gates in SET suppression using delay and dual-rail configurations at 0.35 μm, *IEEE Trans. Nucl. Sci.* **53** (2006) 3428–3431.
21. X. Meng, R. Saleh and K. Arabi, Layout of decoupling capacitors in IP blocks for 90-nm CMOS, *IEEE Trans. Very Large Scale Integr. Syst.* **16** (2008) 1581–1588.
22. B. Narasimham *et al.*, Characterization of digital single event transient pulse-widths in 130-nm and 90-nm CMOS technologies, *IEEE Trans. Nucl. Sci.* **54** (2007) 2506–2511.
23. M. Andjelkovic, J. Chen, A. Simevski, O. Schrape, M. Krstic and R. Kraemer, Monitoring of particle count rate and LET variations with pulse stretching inverters, *IEEE Trans. Nucl. Sci.* **68** (2021) 1772–1781.
24. Q. Zhou and K. Mohanram, Gate sizing to radiation harden combinational logic, *IEEE Trans. Comput.-Aided Des.* **25** (2006) 155–166.
25. Y. S. Dhillon, A. U. Diril, A. Chatterjee and A. D. Singh, Analysis and optimization of nanometer CMOS circuits for soft-error tolerance, *IEEE Trans. Very Large Scale Integr. Syst.* **14** (2006) 514–524.
26. J. Kumar and M. Tahoori, Use of pass-transistor logic to minimize the impact of soft errors in combinational circuits, *Proc. IEEE Workshop on Silicon Errors in Logic – System Effects (SELSE)*, 2005, pp. 67–74.
27. M. R. Choudhury, Q. Zhou and K. Mohanram, Soft error rate reduction using circuit optimization and transient filter insertion, *J. Electron. Test.* **25** (2009) 197–207.
28. M. Abufalgha, Reliability-energy-performance optimization in combinational circuits in presence of soft errors, PhD thesis, Newcastle University (2019).
29. H. S. Deogun, D. Sylvester and D. Blaauw, Gate-level mitigation techniques for neutron-induced soft error rate, *Proc. Int. Symp. Quality Electronic Design (ISQED)*, San Jose, USA, 2005, pp. 175–180.
30. M. Andjelkovic, M. Babic, Y. Li, O. Schrape, M. Krstic and R. Kraemer, Use of decoupling cells for mitigation of SET effects in CMOS combinational gates, *Proc. Int. Conf. Electronic Circuits and Systems (ICECS)*, Bordeaux, France, 2018, pp. 361–364.
31. Y. Sasaki, K. Namba and H. Ito, Soft error masking circuit and latch using schmitt trigger circuit, *Proc. IEEE Int. Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Arlington, USA, 2006, pp. 327–335.
32. A. L. Zimpeck, L. Artola, G. Hubert, C. Mainhardt, F. L. Kastensmidt and R. Reis, Circuit-level hardening techniques to mitigate soft errors in FinFET logic gates, *Proc. European Conf. Radiation Effects on Components and Systems (RADECS)*, Montepellier, France, 2019, pp. 1–4.