INTERNATIONAL CONFERENCE ON RADIATION IN VARIOUS FIELDS OF RESEARCH
RAD 10th Jubilee Spring Edition
June 13-17, 2022 | Herceg Novi | Montenegro
BOOK OF ABSTRACTS

Simulation of single event transient effects in CMOS circuits using open access tools and device models

Milos Marjanovic[1], Marko Andjelkovic[2], Milos Krstic[2,3], Goran Ristic[1]

1 Faculty of Electronic Engineering, University of Nis, Nis, Serbia
2 IHP – Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder), Germany
3 University of Potsdam, Potsdam, Germany

https://doi.org/10.21175/rad.spr.abstr.book.2022.27.8

Single Event Transients (SETs) are voltage glitches induced in electronic circuits as a result of the passage of high energy particles (e.g. heavy ions) through the sensitive transistors. If propagated to the sequential elements, the SETs may result in soft errors, leading to data corruption or even system failure. With the scaling of transistor size and supply voltage, and increase of operating frequency, the SET effects are becoming more critical. Besides the space applications, the SETs have become an important reliability concern also for terrestrial safety-critical applications such as automotive electronics. Therefore, it is important to address the SET effects in the design of reliable integrated circuits.

A typical approach for analysis of SET effects is based on computer-aided simulations. One of the most common techniques is the SPICE-based current injection. This approach allows to study the sensitivity of individual transistors and logic gates in the circuit. Based on the obtained information, appropriate SET mitigation solutions can be applied to improve the system robustness. In most cases, the SET simulations are done with commercial tools and proprietary device models, which may be a limiting factor for widespread adoption of SET analysis methodologies for educational purposed. For this reason, in this work we demonstrate how open access simulation tool LTSpice and open source Predictive Technology Model (PTM) library could be applied for the analysis of SET effects in scaled CMOS technologies.

As a case study, a CMOS inverter was analyzed. For simulation of SETs, a bias-dependent current source was connected to the output of inverter. The threshold Linear Energy Transfer (LET_{TH}) and SET pulse width have been analyzed for six process nodes: 130 nm, 90nm, 65nm, 45nm, 32nm, 22nm. The influence of supply voltage and temperature on the SET sensitivity of inverter has been investigated.