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Enhancing Device Performance with High Electron Mobility GeSn Materials

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As transistors continue to shrink, the need to replace silicon with materials of higher carrier mobilities becomes imperative. Group-IV semiconductors, and particularly GeSn alloys, stand out for their high electron and hole mobilities, making them attractive for next-generation electronics. While Ge *p*-channel devices already possess a high hole mobility, here the focus is on enhancing *n*-channel transistor performance by utilizing the superior electron mobility of GeSn as channel material. Vertical gate-all-around nanowire (GAA NW) transistors are fabricated using epitaxial GeSn heterostructures that leverage the material growth, in situ doping, and band engineering across source/channel/drain regions. It is demonstrated that increasing Sn content in GeSn alloys constantly improves the device performances, reaching a fivefold on-current improvement over standard Ge devices for 11 at.% Sn content. The present results underline the real potential of the GeSn alloys to bring performance and energy efficiency to future nanoelectronics applications.

1. Introduction

The field of electronics witnesses a continuous technological development via both novel materials and innovative devices. Today electronics are seamlessly integrated into our everyday lives via communications, entertainment artificial intelligence, and the Internet of Things (IoT), leading to an exponential increase in data transfer/processing and a high-power consumption.[1–3] Consequently, integrated circuits with faster speed, lower power consumption, and larger transistor integration density are a critical demand. With the classical scaling of Si-based complementary metal-oxide-semiconductor (CMOS) technology approaching its limit,[4] new semiconductors with higher carrier mobility[5] as well as novel device concepts[6–8] for low-power applications stand in the need for further nanoelectronics performance improvement.[9] By replacing the Si channel with high-mobility semiconductors lower applied voltage can be achieved without the device's performance loss.[6] Ge is the next group IV material investigated due to its high hole mobility and compatible processes with CMOS technology.[10–12] However, its low electron mobility and limited *n*-type doping concentration restrict its performance as *n*-channel metal-oxide-semiconductor field effect transistor (MOSFET).

Group IV semiconductor alloys include a large range of alloys, extending from the binaries SiGe and GeSn to the ultimate quaternary CSiGeSn alloy, each with its specific material characteristics. The attractiveness for epitaxial growth and the subsequent fabrication of devices from these alloys is driven by the prospect of monolithic integration across varied application domains, ranging from electronics[13–19] and photonics[20–26] to thermoelectric[27,28] and spintronics[29,30] on silicon substrates. A notable advancement is achieved through the incorporation of Sn atoms into the Ge lattice, which reduces the Γ-valley's energy in the conduction band below that of the *L*-valley. This modification transforms the material from an indirect to a direct bandgap semiconductor. Such an energy band shift underscores the alloy's significant potential in photonics applications, where a fundamental direct bandgap is a property necessary for efficient light emission and absorption processes.[5,31] Moreover, the tenfold lower effective mass of the Γ-valley electrons compared to those of the L-valley, provides direct bandgap GeSn alloys with enhanced electron mobility,[32] particularly advantageous as channel semiconductors for MOSFETs.[13] Moreover, superior mobility facilitates improved conductivity and faster switching speeds,

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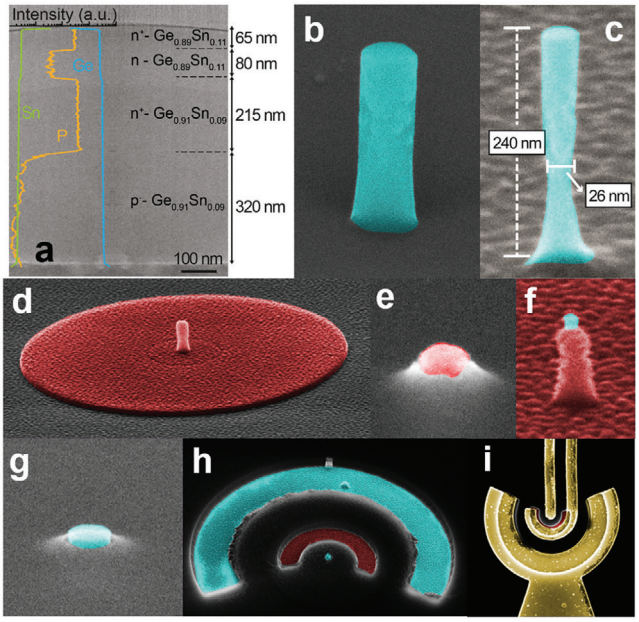

Figure 1. Device fabrication: a). TEM micrograph of one of the grown layer stacks overlaid with SIMS data showing the doping, as well as Sn and Ge contents. b) SEM image of a nanowire after RIE etching. c) SEM image of a nanowire before gate stack deposition. The nanowire's diameter is ≈25 nm. d) After gate stack deposition and patterning. e) Exposed NW top before gate stack removal. f) NW with exposed top. g) Exposed NW top before Ni deposition. h) After via etching for gate and bottom contacts. i) Top view of the finished device with deposited contact pads. (Images d–h with false colors. Cyan: GeSn, Red: TiN, Yellow: Ti/Al.).

essential for high-performance computing applications. A hole mobility of above 500 cm^2 Vs^{-1} for GeSn-channel devices outperforms Ge MOSFETs[33] and GeSn channel nanowires MOSFETs with a Sn content of only 5 at.% already led to an increase in electron mobility by a factor of 2.5 to the Ge channel device.[13] Despite promising results, most of the research on GeSn FETs has been focused on *p*-type devices, primarily because of the challenging epitaxial growth and device fabrication of high-Sn content *n*-type GeSn alloys. However, in the case of NW device architecture, the expected FET performance boost is somewhat reduced due to the limited area of the top contacts, which results in significantly high contact resistance.[34,35]

In this work, we address the previously mentioned challenges by analyzing and comparing the performance of vertical gate-all-around (GAA) nanowire (NW) *n*-type MOSFETs fabricated using direct bandgap GeSn alloys. We explore the impact of the Sn concentration on the transistor's figures-of-merit, focusing on GeSn alloys with 8 at.% Sn, marking the transition from indirect to direct bandgap, and 11 at.% Sn, which exhibits a direct bandgap.

2. Layer Growth and Device Fabrication

The device design, based on GeSn/Ge heterostructure presented in **Figure** 1a, benefits significantly from the vertical nanowire (NW) architecture, which offers several key advantages: i) the source, drain, and channel regions are defined through epitaxial growth that allows precise control over the Sn content, dopant concentration, and thickness of each region. By tuning the alloy composition, the electronic band structures of every region can be tuned for specific functional requirements. ii) The doping process can be accurately controlled in situ, eliminating the need for ion implantation that introduces crystal defects, thereby reducing the injection mobility. iii) The vertical configuration decouples the device footprint from the channel length and allows for an increased device integration density. iv) The vertical design mitigates the short-channel effects that negatively impact the device performance, enhancing the overall functionality and efficiency of the semiconductor device.

The GeSn/Ge heterostructures used for the vertical NW MOSFETs fabrication have been epitaxially grown on Ge buffered 200 mm Si wafers using an industrial CVD reactor. Details can be found elsewhere.[36–38] The structure consists of a highly *n*-type phosphorus (P) doped top layer (TL), an unintentionally low-doped middle layer (ML), and a highly *n*-doped bottom layer (BL), as summarized in **Table** 1. The unintentionally low-doped region defines the channel length of the device. One structure consists of constant composition $Ge_{0.92}Sn_{0.08}$ alloy for all source, drain, and channel regions. At this Sn-concentration the bandgap is almost at the transition from indirect to direct, meaning that the Γ- and *L*-valley are energetically aligned[39] (see inset **Figure** 2a). The second GeSn heterostructure consists of a 215 nm thick $Ge_{0.91}Sn_{0.09}$ alloy as BL (later source) and a $Ge_{0.89}Sn_{0.11}$ alloy as channel and top layer (later drain). Based on the band structure calculations this heterostructure presents a direct bandgap through the entire device length after patterning into NW. The *n*-type doping is achieved by in situ substitutional phosphorus incorporation during the GeSn epitaxy. A cross-section TEM image of the layer stack overlaid with the elemental distribution spectrum acquired via secondary ion mass spectrometry (SIMS) is shown in Figure 1a. The interface between the individual GeSn layers is free of dislocations or other crystalline defects demonstrating the high-quality of the epitaxial growth. The reference device used for comparison and for benchmarking purposes is fabricated on a n-i-n Ge homo-structure.

The GeSn NWs were fabricated using a top–down approach. First, the NWs were defined by e-beam lithography and etched by an anisotropic ICP-RIE process with a high degree of anisotropy using Cl_2/Ar gas. The resulting nanowire, Figure 1b, has a height of ≈210 nm and a diameter between 50 and 60 nm. To further reduce their diameter, the samples were subject to a cycle of oxide formation by plasma oxidation and oxide removal by HF etching. The self-limiting nature of the plasma oxidation assures high control of the diameter etching. NWs with a diameter of 25 nm were obtained as shown in the SEM image in Figure 1c.

The gate stack formation starts with the deposition of 1 nm Al_2O_3 by ALD. Subsequently, a plasma post-oxidation step led to the formation of a smooth $GeSnO_x$ layer underneath. Such a step has been shown to improve the quality of the interface and strongly reduce the interface trap density D_{it} in Ge.[40–42] The gate dielectric is completed by a 5 nm HfO_2 layer. As a metal gate 40 nm of sputtered TiN was used and the gate pads were subsequently patterned by lithography and ICP-RIE etching (Figure 1d).

The MOSFETs fabrication continues with a planarization step and subsequent etch-back that uncovered only the top of the NW (Figure 1e) for the removal of the TiN and the dielectric (Figure 1f). A second planarization step was performed to

Table 1. Parameters of the heterostructures used for device fabrication.

Device	Top layer material	Top layer doping [P cm^{-3}]	Channel [ML]	Bottom layer material	Bottom layer doping [P cm^{-3}]
Ge FET	Ge 100 nm	$\approx 2 \times 10^{19}$	Ge 130 nm	Ge 270 nm	$\approx 2 \times 10^{19}$
GeSn FET(8 at.% Sn)	$Ge_{0.92}Sn_{0.08}$ 80 nm	4×10^{19}	$Ge_{0.92}Sn_{0.08}$ 100 nm	$Ge_{0.92}Sn_{0.08}$ 200 nm	4×10^{19}
GeSn FET(11 at.% Sn)	$Ge_{0.89}Sn_{0.11}$ 65 nm	2.5×10^{19}	$Ge_{0.89}Sn_{0.11}$ 80 nm	$Ge_{0.91}Sn_{0.09}$ 215 nm	3.5×10^{19}

prepare the NW for top-contact formation (Figure 1g). For this purpose, 6 nm of Ni were deposited and annealed in a forming gas ambient N_2:H_2 to form NiGeSn metallic alloy contact. To finalize the device fabrication, vias for the gate and the bottom contacts were opened (Figure 1h) and a Ti/Al metal stack was deposited (Figure 1i).

3. Device Characterization

The vertical GAA NW FETs were evaluated using the bottom contact as the source and the top contact as the drain terminal. The drain current versus gate voltage (I_d–V_g) transfer characteristics of these devices, each with an NW diameter of 25 nm, are presented in **Figure** 3a–c. All devices demonstrate effective switching capabilities, characterized by a low subthreshold swing (SS) and a high on/off current ratio (I_{on}/I_{off}). The observed shift of the characteristic at a drain voltage V_d = 0.3 V compared to V_d = 0.1 V is primarily attributed to an increase in the off-current at increased voltages due to gate-induced drain leakage (GIDL). Additionally, an increase in the off-current (minimum drain current) was obtained for the higher Sn content device. These results are in agreement with the lower bandgap of the GeSn layer as the Sn content increases (see inset Figure 2a). The increase in off-currents is due to the bandgap's exponential influence on GIDL, mainly caused by band-to-band tunneling, indicating a smaller bandgap for layers with higher Sn content.

The incorporation of 8 at.% Sn into the device results in a 60% improvement in on-current, while an increase to 11 at.% Sn leads to a remarkable 410% enhancement in on-current compared to the reference Ge NW FET. This significant improvement is attributed to the enhanced electron mobility facilitated by the low effective mass of electrons in the Γ-valley, which becomes increasingly populated as the energy difference between the Γ- and *L*-valleys expands with rising Sn concentration (inset of Figure 2a). This is further proved by the transconductance (G_m) values, as illustrated in Figure 3d, which shows transconductance measurements of 30 µS µm^{-1} for Ge, and 52 µS µm^{-1} and 150 µS µm^{-1} for devices with 8% and 11% GeSn, respectively. The transition from a pure Ge device to a device with 11 at.% GeSn marks an approximately fivefold improvement in performance. The strong increase in transconductance highlights the improved mobility of the GeSn alloys compared to Ge. At a low $V_{d,}$ the maximum G_m is proportional to the intrinsic electron mobility μ_0 by:

$$G_{m.max} = \frac{WC_{ox}}{L}\,\mu_0 V_d \tag{1}$$

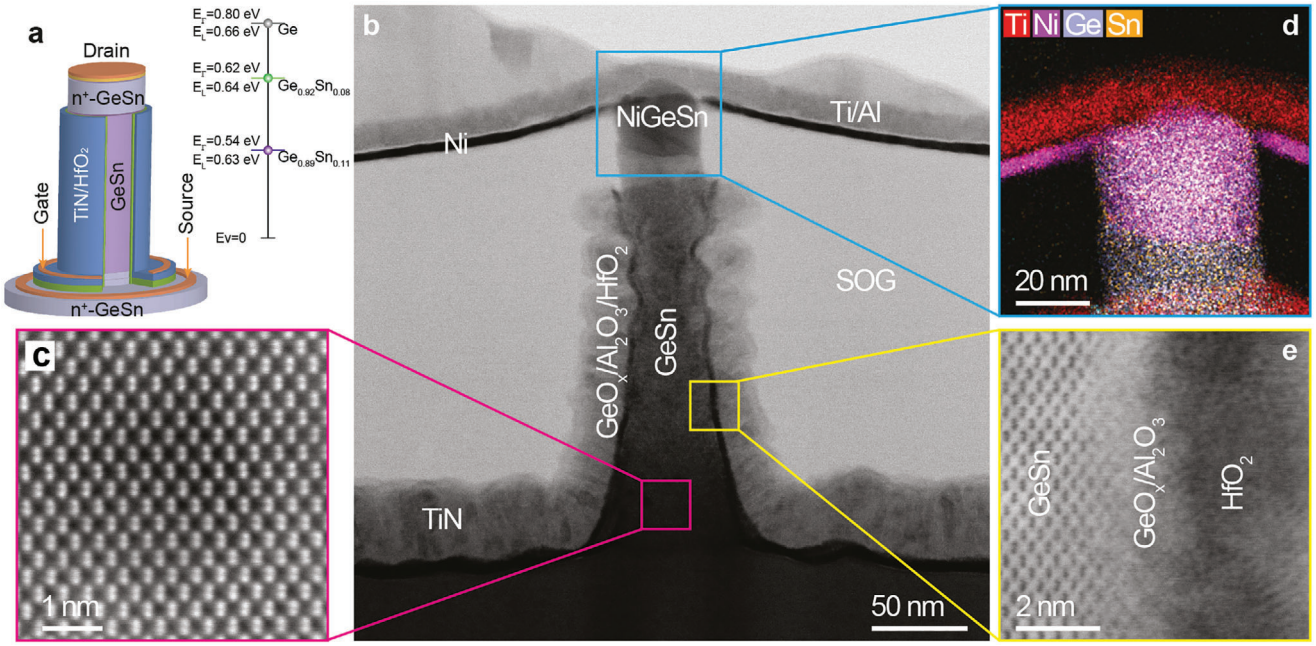

Figure 2. Device structure characterization. a) Schematic showing the vertical GAA GeSn NW FET architecture. The inset shows the band energy of the Γ- and *L*-valley at the conduction band. b) TEM micrograph of a finished device. The insets show HR-TEM micrographs of c) the lattice in the channel region, d) Elemental EDX analysis of the top part of the device underlining NiGeSn alloy on the GeSn NW, e) gate dielectric/GeSn channel interface.

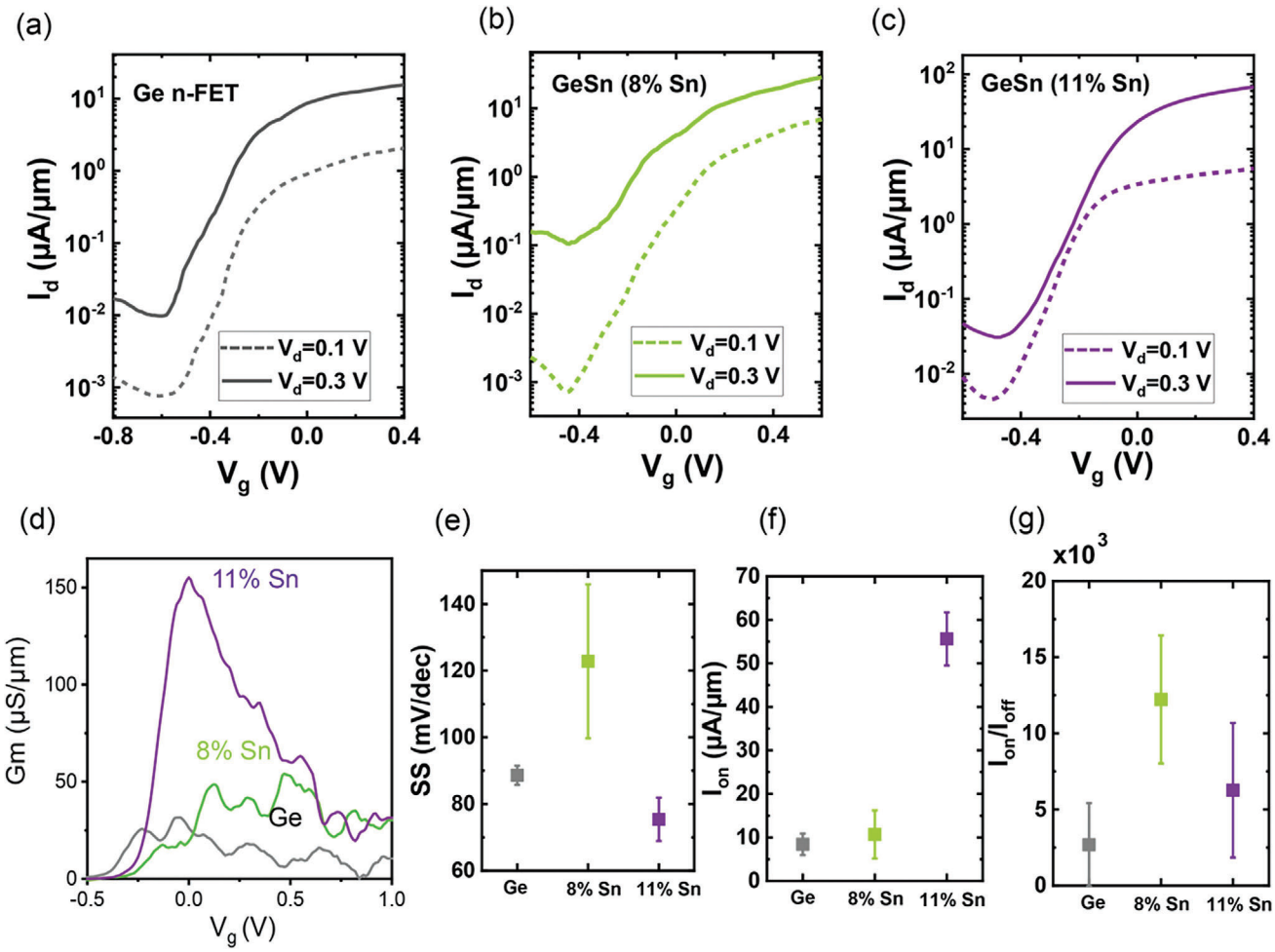

Figure 3. Vertical GAA GeSn NW characteristics: a–c) I_d–V_g transfer characteristics of three devices corresponding to channel materials of Ge, 8%-GeSn, and 11%-GeSn. d) Comparison of the transconductance (G_m) of the devices measured at V_d = 0.3 V. e–g) Comparison of subthreshold swing (SS), on-current (I_{on}) measured at V_g–V_{th} = 0.5 V, V_d = 0.3 V, and I_{on}/I_{off} (at V_d = 0.1 V) for all three channel material devices.

where W and L correspond to the gate width and length, C_{ox} is the gate capacitance. We suggest that C_{ox} and the device dimensions W and L are the same due to the use of the same process for all devices. Hence, the only factor left to explain the improvement is the mobility. Therefore, we can conclude that the intrinsic mobility (low field mobility) μ_0 for the 11% Sn device is fivefold of the reference Ge device, demonstrating a high mobility GeSn channel for n-FETs.

The key performance indicators for the devices are summarized in Figure 3e–g. A subthreshold swing (SS) of 68 mV dec^{-1} was recorded for a device featuring 11 at.% Sn content, closely approaching the theoretical room temperature minimum value of 60 mV dec^{-1}. The presence of $GeSnO_x$ at the gate dielectric/GeSn channel interface has been shown to reduce the density of interface states[9] which significantly enhances the device electrostatic screening, thereby contributing to a low SS value. This is further reflected by the drain-induced barrier lowering (DIBL) behavior shown in the pure Ge and 8% GeSn devices. The high density of interface states in these devices causes DIBL and larger SS. The decrease of the I_{on}/I_{off} ratio with the increase in the Sn content in the GeSn channel device is attributed to the larger GIDL due to the smaller GeSn bandgap.

Figure 4a shows the threshold voltage V_{th}. The V_{th} is negative for all three devices. The reason for the negativity of these three values is found in the epitaxy process. During the growth of the channel layer, the CVD chamber still contains residues of the doping precursor gas from the growth of the bottom layer, leading to the incorporation of *n*-type dopants in the channel layer (Figure 1a). This causes the device to be operated like a junctionless transistor. On the other hand, intrinsic GeSn are naturally slightly *p*-type, due to the presence of crystal defects like vacancies. This *p*-type doping counteracts the incorporated *n*-type dopants. Since GeSn is an alloy, the number of vacancies and therefore the level of natural *p*-type doping is expected to be considerably higher than for the higher Sn content GeSn layer. This leads to a stronger compensation of the unintentional *n*-type doping and thereby a higher V_{th}. Another aspect to be considered is the interface quality. Judging from the SS, the interface quality is higher for the 11% GeSn alloy than for Ge and 8% GeSn. The lower D_{it} also contributes to keeping

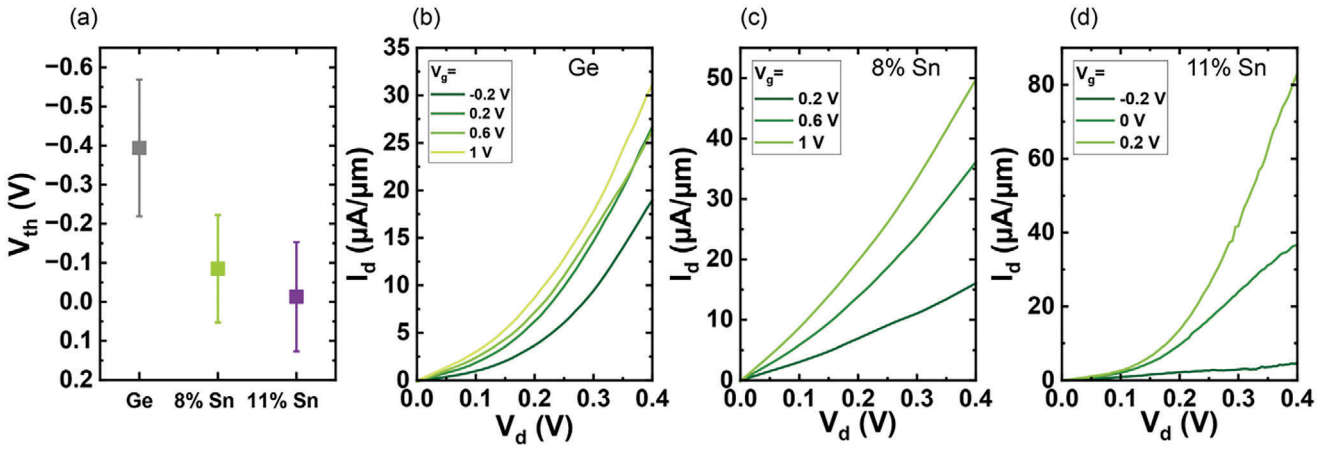

Figure 4. a) Comparison of the V_{th} of the three devices. b–d) V_d–I_d (output) curves of the three devices: b) Ge, c) 8% GeSn, d) 11% GeSn.

the V_{th} closer to zero. A third factor is the bandgap. Due to the smaller bandgap of 11% GeSn compared to Ge and 8% GeSn, a lower applied gate voltage is necessary to turn the device on. The device with 11% Sn content shows a threshold voltage close to zero, which could be suitable for low-voltage, low-power applications.

A well-known issue of *n*-type Ge(Sn) devices is the high contact resistivity and difficulty in forming Ohmic contacts. When metal is brought in contact with *n*-Ge(Sn), additional states are induced in the bandgap, so-called metal-induced gap states. In Ge(Sn), these states are very prominent close to the valence band.[43,44] In consequence, the Fermi level gets pinned close to the valence band, leading to a high Schottky barrier and a high contact resistivity on *n*-type GeSn. This phenomenon is largely independent of the work function of the metal. For vertical nanowires, the contact resistance is especially crucial, due to the extremely small size of the top contact.

Figure 4b–d shows the I_d–V_d output characteristics of the three devices. It is evident that all three devices exhibit superlinear behavior, a distinctive feature characteristic of a Schottky barrier FET. While the maximum achievable *n*-type doping level of Ge is limited by insufficient dopant activation,[45] this constraint is partially relaxed for GeSn, and higher active doping concentrations can be achieved. A higher doping level is beneficial to reduce the effective Schottky barrier since it decreases the thickness of the barrier and thereby facilitates tunneling. Hence, further research into devices with improved doping levels and contact formation methods is needed to tackle this problem.

4. Conclusion

In this work, we showcased the enhanced electron mobility in GeSn materials using vertical GAA NW nFETs, with significant performance gains achieved by increasing the Sn content in the channel. Specifically, $Ge_{0.89}Sn_{0.11}$ channel devices achieved over a fivefold increase in both I_{on} and G_m, primarily through mobility enhancement. Additionally, the $GeSnO_x$ layer at the GeSn interface contributed to a low density of interface states, achieving an SS near the theoretical minimum. The output curves still show some superlinearity, which is caused by the Schottky contact that should be addressed in future work. In conclusion, the great potential of GeSn for nanoelectronic applications is demonstrated by the results of this work. With the continued shrinking of devices, quantum confinement will play a role in widening the bandgap in extremely aggressively scaled devices, which would alleviate the problem of high leakage current due to GIDL.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

direct bandgap, electron mobility, GAA nanowire MOSFET, GeSn alloy, group-IV materials

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