Journal of Applied Physics

RESEARCH ARTICLE | AUGUST 05 2024

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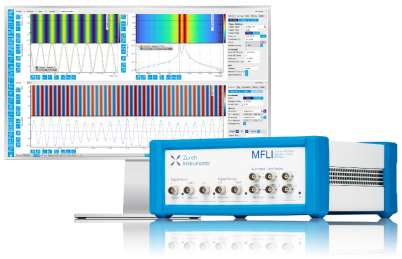
J. Appl. Phys. 136, 055303 (2024)
https://doi.org/10.1063/5.0218703



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Cite as: J. Appl. Phys. **136**, 055303 (2024); doi: 10.1063/5.0218703
Submitted: 13 May 2024 · Accepted: 22 July 2024 ·
Published Online: 5 August 2024

View Online Export Citation CrossMark

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ABSTRACT

$Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys are promising materials for future opto- and nanoelectronics applications. These alloys enable effective bandgap engineering, broad adjustability of their lattice parameter, exhibit much higher carrier mobility than pure Si, and are compatible with the complementary metal-oxide-semiconductor technology. Unfortunately, the equilibrium solid solubility of Sn in $Si_{1-x}Ge_x$ is less than 1% and the pseudomorphic growth of $Si_{1-x-y}Ge_ySn_x$ on Ge or Si can cause in-plane compressive strain in the grown layer, degrading the superior properties of these alloys. Therefore, post-growth strain engineering by ultrafast non-equilibrium thermal treatments like pulse laser annealing (PLA) is needed to improve the layer quality. In this article, $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.8}Sn_{0.06}$ thin films grown on silicon-on-insulator substrates by molecular beam epitaxy were post-growth thermally treated by PLA. The material is analyzed before and after the thermal treatments by transmission electron microscopy, x-ray diffraction (XRD), Rutherford backscattering spectrometry, secondary ion mass spectrometry, and Hall-effect measurements. It is shown that after annealing, the material is single-crystalline with improved crystallinity than the as-grown layer. This is reflected in a significantly increased XRD reflection intensity, well-ordered atomic pillars, and increased active carrier concentrations up to 4×10^{19} cm^{-3}.

I. INTRODUCTION

Currently, the industry's main production lines of integrated circuits (ICs) are predominantly based on group-IV materials such as silicon (Si), germanium (Ge), $Si_{1-x}Ge_x$, or silicon carbide (SiC). Two emerging newcomers in this class are tin (Sn) containing $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys. Adding Sn into Ge or $Si_{1-x}Ge_x$ lattice (i) modifies the band structure of the alloy and allows a transition from an indirect bandgap semiconductor to a direct bandgap semiconductor.[1–3] Such a band structure modification can be used to fabricate optoelectronic devices like light emitting diodes, lasers, and detectors.[2,4–6] Furthermore, these alloys showed the potential of superior mobilities of up to 6000 cm^2 V^{-1} s^{-1} for electrons and 4500 cm^2 V^{-1} s^{-1} for holes.[7–11] However, it requires a high material quality to achieve such performances. Typically, both alloys are epitaxially grown on Ge or Ge-buffered substrates by chemical vapor deposition (CVD)[1,12] or molecular beam epitaxy (MBE).[13,14] Ge is used since it is complementary metal-oxide-semiconductor (CMOS)-compatible, has a relatively large lattice parameter, and

allows post-growth thermal treatments under equilibrium conditions.[15] Unfortunately, pure Ge wafers are expensive and the more complex layer stack of Ge-buffered Si substrates complicates the fabrication and characterization of lateral ICs. Furthermore, for many device concepts, insulating substrates are desired.[16] Recently, the first GeSnOI substrates were fabricated by direct wafer bonding and etch-back approach[16–18] or by underetching and layer transfer to insulating substrates.[19] These methods are cost-intensive and technically challenging. A much simpler way to fabricate $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on an insulating platform would be the direct growth of these alloys on commercially available ultra-thin silicon-on-insulator (SOI) wafers. In the last few years, the feasibility of growing single-crystalline $Ge_{1-x}Sn_x$ directly on Si substrates[20–22] was shown, and defect densities of about $\sim 10^7\ cm^{-2}$ were estimated.[22] In this paper, we present the fabrication of $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on commercially available SOI substrates and apply non-equilibrium post-growth pulse laser annealing (PLA) to mediate between the highly lattice-mismatched alloys and the SOI substrate beneath. Nanosecond PLA helps us to improve the crystal structure of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys.

II. EXPERIMENTAL PART

A commercially available 300 mm-SOI wafer with a 20 nm-thick top Si and 100 nm-thick SiO_2 layer was used as a low-cost substrate. The wafer was diced into $35 \times 35\ mm^2$ pieces, and the native SiO_2 was removed by a 2.5% HF:DI etching for 15 s. Afterward, four SOI pieces were simultaneously inserted for each of the alloys into a solid-source MBE system with a base pressure of 1×10^{-10} mbar. The substrate was heated up to 700 °C with a ramp of about 30 °K min^{-1}. Then, the temperature was kept constant for 5 min to eliminate hydrogen dangling bonds on the Si surface created by HF etching.[23] After thermal stabilization, the MBE growth was performed at around 180 °C for $Ge_{0.94}Sn_{0.06}$ and 200 °C for $Si_{0.14}Ge_{0.80}Sn_{0.06}$. Both 20 nm-thick layers are *in situ* doped with Sb with a targeted concentration of $5 \times 10^{19}\ cm^{-3}$. The elements Ge, Sn, and Sb were evaporated using Knudsen effusion cells. Si was evaporated via electron beam. Post-growth PLA was performed under atmospheric conditions with single pulses. The PLA tool 'Coherent VarioLas ECO 308 5 × 5 for COMPexPro200' is equipped with a 308 nm wavelength XeCl excimer laser with a fixed pulse length of 28 ns. A 'MaxBlack EnergyMax Sensor' measured the laser energy from which the energy density for the homogeneously irradiated $5 \times 5\ mm^2$ area was calculated.

Cross-sectional high-resolution transmission electron microscopy (HR-TEM) imaging to evaluate the layer crystallinity was performed using an image-C_s-corrected Titan 80-300 microscope (FEI) operated at an accelerating voltage of 300 kV. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) imaging and spectrum imaging analysis based on energy-dispersive x-ray spectroscopy (EDXS) were performed at 200 kV with a Talos F200X microscope equipped with a Super-X EDX detector system (FEI). Before (S)TEM analysis, the specimen mounted in a high-visibility low-background holder was placed for 10 s into a Model 1020 Plasma Cleaner (Fischione) to remove potential contamination. Cross-sectional TEM lamellae preparation was done by *in situ* lift-out using a Helios 5 CX focused ion beam (FIB) device (Thermo Fisher, Eindhoven, Netherlands). For each sample, to protect its surface, a carbon cap layer was deposited beginning with electron-beam-assisted and subsequently followed by Ga-FIB-assisted precursor decomposition. Afterward, the TEM lamella was prepared using a 30 keV Ga-FIB with adapted currents. Its transfer to a 3-post copper Omniprobe lift-out grid was done with an EasyLift EX nanomanipulator (Thermo Fisher). To minimize sidewall damage, Ga ions with only 5 keV energy were used for final thinning of the TEM lamella to electron transparency. X-ray diffraction (XRD) was performed on a Rigaku SmartLab x-ray diffractometer system. The system is equipped with a copper (Cu) x-ray tube and a Ge (220) two-bounce monochromator. High-resolution XRD (HR-XRD) θ–2θ scans were carried out on the symmetrical 0 0 4 reflections. Reciprocal space maps (RSMs) were generated for the 0 0 4 and the asymmetrical 2 2 4 reflections by scanning ω and measuring the diffraction intensity in dependence of 2θ with the detector in 1D single-exposure mode. The samples were aligned by their 0 0 4 and 2 2 4 Si substrate reflections for these measurements. The lateral and vertical lattice parameters of the epitaxially grown layers were determined from the 2 2 4 RSM. Rutherford backscattering spectrometry (RBS) in random (RBS-R) and channeling (RBS-C) directions were performed using a 2 MV Van de Graaff accelerator. The used He^+ beam had an energy of 1.7 MeV and beam currents between 10 and 20 nA. An aperture with a diameter of about 1 mm was used. Each measurement was performed with a detector angle of 170°. The obtained RBS spectra were fitted with the software SIMNRA.[24] RBS-C was performed along the [001] crystal axis. Time-of-flight (ToF) secondary ion mass spectrometry (SIMS) measurements were conducted before and after annealing. The used IONTOF V tool is equipped with a ToF mass separator. The material was sputtered by Cs^+ with an energy of 500 eV and a sputter area of $400 \times 400\ \mu m^2$. The analysis was performed with Bi_1^+ having an energy of 15 keV and an area of $200 \times 200\ \mu m^2$. Variable-field Hall-effect measurements in van-der-Pauw configuration were performed at room temperature using an HMS 9709A system from LakeShore. Close to the sample corners, 50 nm-thick circularly shaped Ni contacts with a diameter of 1 mm were fabricated by lithography, 1% HF:DI oxide etching, thermal evaporation of Ni, and lift-off. The magnetic flux density was varied between −5 and 5 T.

III. RESULTS AND DISCUSSION

The microstructure of the as-grown $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI was investigated by TEM-based analyses, as presented in Fig. 1. The superimposed EDXS-based element distribution maps in Figs. 1(a) and 1(b) confirm the targeted layer stack with a relatively homogeneous distribution of Sn within $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$, respectively. As shown in Figs. 1(c) and 1(e), the microstructure of $Ge_{0.94}Sn_{0.06}$ appears to be partially crystalline, where only some of the defective grains grow up to the sample surface. The other layer regions are characterized by an amorphous microstructure. The presence of such amorphous inclusions indicates an epitaxial breakdown during the growth, which appears when the critical thickness of highly mismatched alloys is exceeded.[25] The $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layer in Figs. 1(d) and 1(f) is mainly single-crystalline but contains many stacking

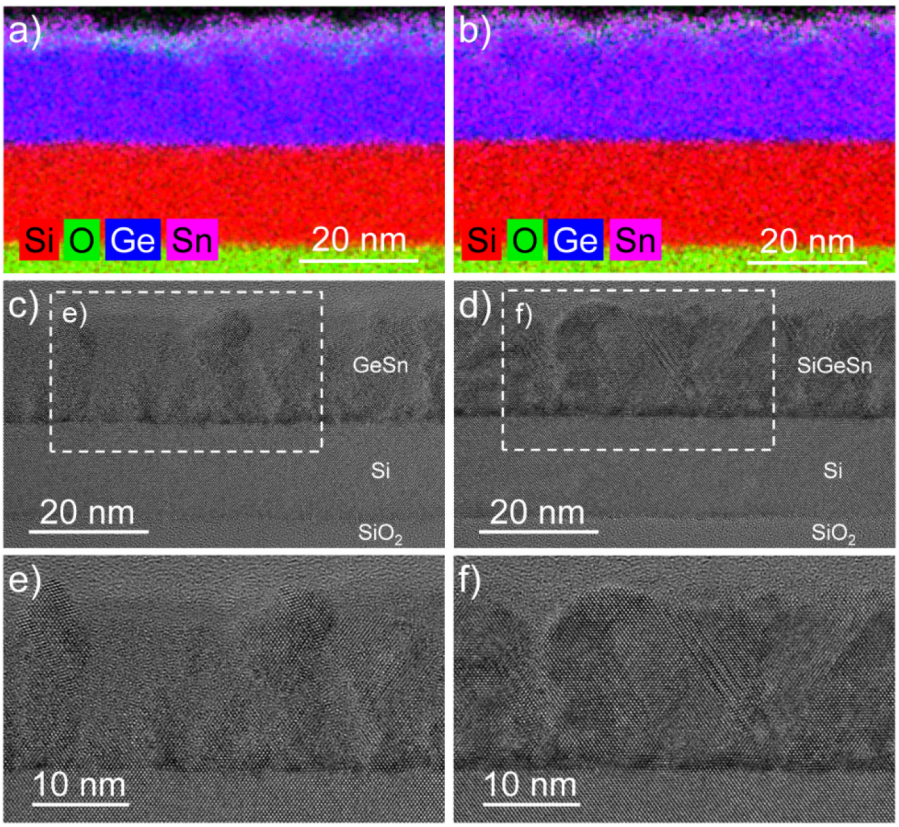

FIG. 1. TEM-based analysis of the as-grown $Ge_{0.94}Sn_{0.06}$ on SOI in (a), (c), and (e) and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI in (b), (d), and (f). The EDXS-based maps in (a) and (b) are the superimposed element distributions of Si (red), O (green), Ge (blue), and Sn (magenta). The HR-TEM images in (c) and (d) show from bottom to top: buried SiO_2, Si, and the grown $Ge_{0.94}Sn_{0.06}$ or $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layer. The white dashed rectangles in (c) and (d) correspond to the enlarged images in (e) and (f).

faults. The top surfaces of $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ have a native oxide layer and seem to be slightly rougher compared to the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$/Si interfaces, respectively. This suggests a "layer-by-layer" plus "three-dimensional island"-based (Stranski–Krastanov) growth with a small island spacing rather than the targeted "layer-by-layer" (Frank–van der Merwe) growth mechanism.[26] Since the microstructures of the as-grown alloys are defect-rich, post-growth annealing is required to improve the crystallinity. On the other hand, these Sn-containing alloys are metastable and would decompose during long thermal treatments above the growth temperature. Consequently, we decided to use ns-range PLA.

The microstructure after PLA with 0.20 J cm^{-2} ($Ge_{0.94}Sn_{0.06}$) or 0.25 J cm^{-2} ($Si_{0.14}Ge_{0.80}Sn_{0.06}$) is shown in Fig. 2. Both materials have a highly improved crystal structure compared to their as-grown states. The $Ge_{1-x}Sn_x$ sample is fully crystalline after PLA at 0.20 J cm^{-2} but shows local inhomogeneities in the $Ge_{1-x}Sn_x$ layer thickness [Figs. 2(c) and 2(e)]. The $Si_{0.14}Ge_{0.80}Sn_{0.06}$ sample PLA-treated at 0.25 J cm^{-2} also shows a single-crystalline structure with only few defects [see Figs. 2(d) and 2(f)]. The EDXS-based element distribution maps in Figs. 2(a) and 2(b) suggest an out-diffusion of Sn (particularly for $Si_{0.14}Ge_{0.80}Sn_{0.06}$ after PLA at 0.25 J cm^{-2}) and the formation of a thick Sn-containing oxide at the sample surface. Further details about the element redistribution can be found in Sec. C in the supplementary material. On the other hand, any formation of Sn clusters or filaments was not observed after PLA with low energy densities, which is significantly different compared to pulse laser melting results of $Ge_{1-x}Sn_x$.[27–29]

Since first local inhomogeneities and the out-diffusion of Sn are undesired processes, the PLA energy density E_d was systematically reduced, and the crystal structure evolution was investigated by XRD and RBS. Figures 3 and 4 show 2 2 4 RSMs for $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ samples annealed at different conditions, respectively. The as-grown state of $Ge_{0.94}Sn_{0.06}$ in Fig. 3(a) has a barely noticeable GeSn 2 2 4 reflection located close to the strain relaxation line at $q_z/2\pi \approx 7.0\,\mathrm{nm}^{-1}$. This weak diffraction is related to the mostly amorphous nature of the $Ge_{0.94}Sn_{0.06}$ layer. After PLA, the peak intensity increases significantly. Furthermore, the location of the reflection on the black dashed strain relaxation line confirms that the $Ge_{1-x}Sn_x$ layer is almost strain-relaxed on the SOI substrate. Converting the reciprocal in-plane q_x and out-of-plane q_z peak lattice parameters into the real space in-plane a_{II} and out-of-plane $a_\perp$ lattice parameters by Eqs. (1) and (2) leads to a relaxed lattice parameter $a_\perp \approx a_{II} \approx 0.57$ nm,

$$a_\perp = 4\,\frac{2\pi}{q_z}, \tag{1}$$

$$a_{II} = \sqrt{8}\,\frac{2\pi}{q_x}. \tag{2}$$

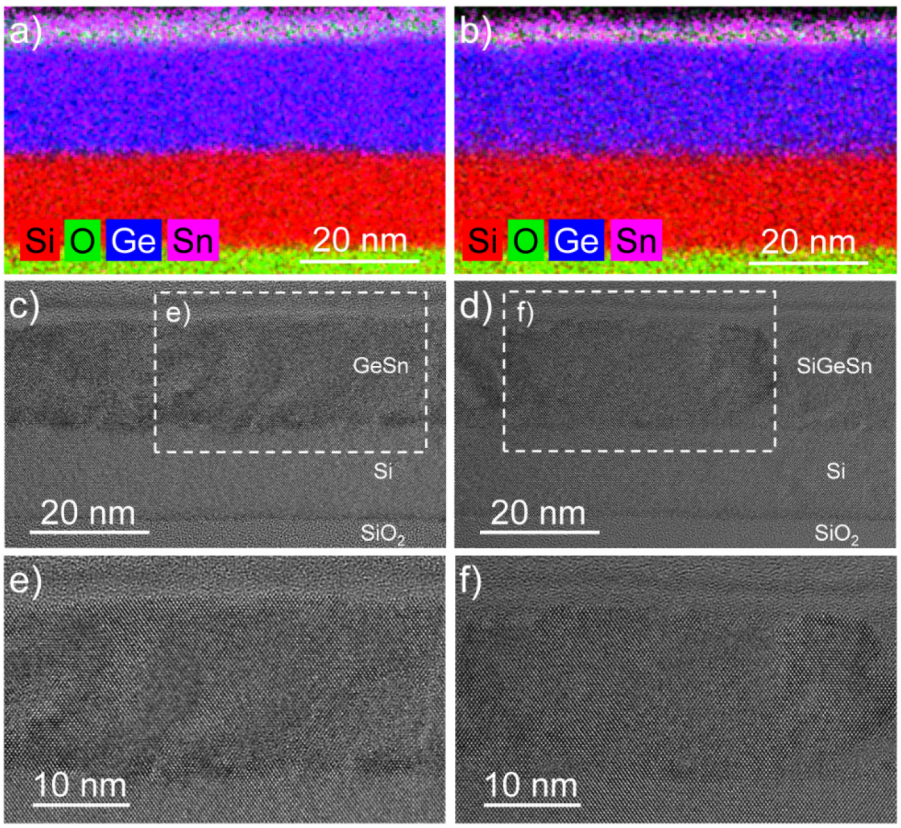

FIG. 2. TEM-based analysis of $Ge_{0.94}Sn_{0.06}$ on SOI after PLA at 0.20 J cm^{-2} in (a), (c), and (e) and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI after PLA at 0.25 J cm^{-2} in (b), (d), and (f). The EDXS-based maps in (a) and (b) are the superimposed element distributions of Si (red), O (green), Ge (blue), and Sn (magenta). The white dashed rectangles in (c) and (d) correspond to the enlarged images in (e) and (f).

Applying the bowing-parameter-corrected Vegard's law [see Eq. (3)],[30] where a_{Ge} is the lattice parameter of pure Ge, Δ_{GeSn} is the difference of the elemental Ge and Sn lattice parameters, and $\Psi_{GeSn} = 0.016$ nm[30] is the bowing parameter, allows to approximate the Sn concentration in $Ge_{1-x}Sn_x$ to $x \approx 5.97$ at.% after PLA. Since the Sb incorporation was not taken into account, the given Sn concentration should be taken as an estimate,

$$a_{Ge_{1-x}Sn_x} = a_{Ge} + \Delta_{GeSn}\, x + \Psi_{GeSn}\, x\,(1-x). \tag{3}$$

The 2 2 4 reflection of the as-grown $Si_{0.14}Ge_{0.80}Sn_{0.06}$ in Fig. 4(a) is located between the pseudomorphic and the strain relaxation lines. This suggests a strain distribution across the layer thickness from partially compressive-strained at the $Si_{0.14}Ge_{0.80}Sn_{0.06}$/SOI interface toward almost relaxed close to the surface. After PLA with 0.15 J cm^{-2}, the SiGeSn 2 2 4 reflection appears to be elongated in the q_z direction. While the portion with $q_z/2\pi \approx 7.0$ nm^{-1} reminds in location and intensity of the as-grown state, the contribution with the higher intensity at

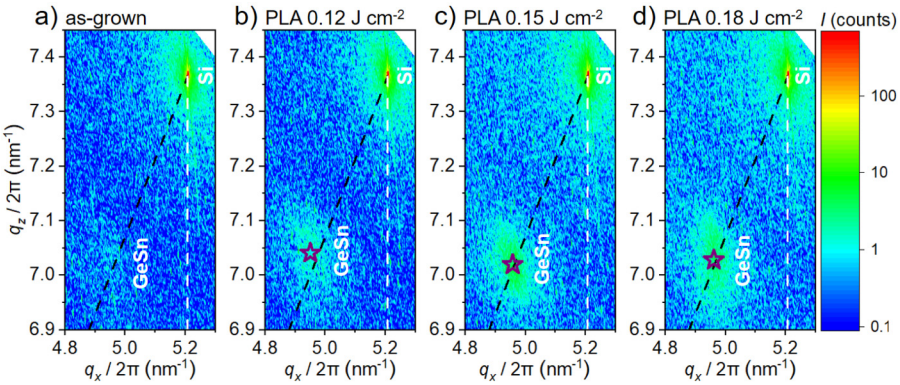

FIG. 3. 2 2 4 RSM of $Ge_{1-x}Sn_x$ on SOI in the as-grown state (a) and after PLA with $E_d = 0.12$ (b), 0.15 (c), and 0.18 J cm^{-2} (d). The black dashed line is the strain relaxation line, and the vertical white dashed line corresponds to the fully pseudomorphically grown state. The fitted maxima of the GeSn 2 2 4 reflections are indicated by the purple stars. The 2 2 4 RSM of $Ge_{1-x}Sn_x$ after PLA with $E_d = 0.20$ J cm^{-2} (see Fig. C3 in Sec. C in the supplementary material) is qualitatively similar to the result at $E_d = 0.18$ J cm^{-2}.

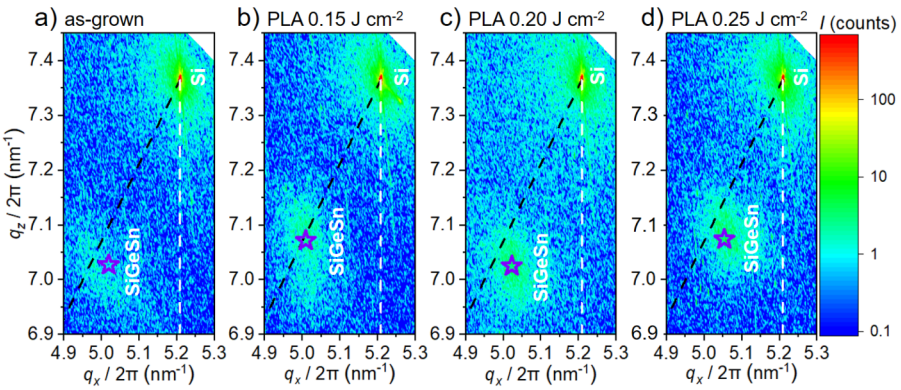

FIG. 4. 2 2 4 XRD-RSM of $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI in the as-grown state (a) and after PLA with $E_d = 0.15$ (b), 0.20 (c), and 0.25 J cm^{-2} (d). The black dashed line is the strain relaxation line, and the vertical white dashed line corresponds to the fully pseudomorphically grown state. The fitted maximum of the SiGeSn 2 2 4 reflection is indicated by the center of the purple star.

$q_z/2\pi \approx 7.1$ nm^{-1} appears to be slightly tensile-strained. This is related to a separation of the $Si_{1-x-y}Ge_ySn_x$ layer into an as-grown-like bottom layer and a slightly tensile-strained top-layer. This tensile strain might be caused by the thermal expansion coefficient differences between the alloy and the substrate, and the large temperature gradient during PLA. Tensile strain was observed earlier for Ge on Si[26,31] or $Ge_{1-x}Sn_x$ on Si[32] after thermal treatments. In the case of $Si_{0.14}Ge_{0.80}Sn_{0.06}$ annealed with $E_d = 0.20$ J cm^{-2} in Fig. 4(c), both reflections merged, and the SiGeSn 2 2 4 reflection has a similar q_x/q_z position as in the as-grown state. This is related to the increase in effectively heated volume with the increasing E_d of the PLA laser. PLA with $E_d = 0.25$ J cm^{-2} causes a shift of the SiGeSn 2 2 4 reflection parallel to the strain relaxation line towards the Si 2 2 4 substrate reflection [Fig. 4(d)]. This is a clear evidence of the out-diffusion of a significant amount of larger atoms since the strain conditions remain almost the same, and it correlates with the lower Sn contrast in the EDX-based element distribution map in Fig. 2(b).

The RBS-R/C results of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ on SOI before and after annealing are shown in Figs. 5 and 6, respectively. The obtained spectra contain Sn superimposed with Sb (1460–1510 keV), Ge (1325–1390 keV), and Si (<1000 keV). Since the Sb concentration is only about 0.1 at. %, the signal in the spectra is mainly related to Sn. The Si contribution of $Si_{0.14}Ge_{0.80}Sn_{0.06}$, located between 950 and 1000 keV, is merged with the pure Si signal of the SOI layer and the high-energy tail of the buried SiO_2.

The RBS-R spectra of the as-grown $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ states were fitted by SIMNRA and confirmed the expected layer compositions and thicknesses.

The RBS-C spectrum of the $Ge_{0.94}Sn_{0.06}$ as-grown state in Fig. 5 is similar to its RBS-R counterpart since the layer contains amorphous inclusions. Analog channeling results were also obtained for the mildly treated PLA 0.12 J cm^{-2} sample. Channeling effects in the Si, Ge, and Sn/Sb signals can be observed after PLA with 0.15, 0.18, and 0.20 J cm^{-2}.

The occurrence of channeling in Si, Ge, and Sn/Sb in the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown state in Fig. 6 confirms the epitaxial growth of $Si_{1-x-y}Ge_ySn_x$ on the SOI wafer. This matches the TEM results in Figs. 1(d) and 1(f). PLA of $Si_{0.14}Ge_{0.80}Sn_{0.06}$ with

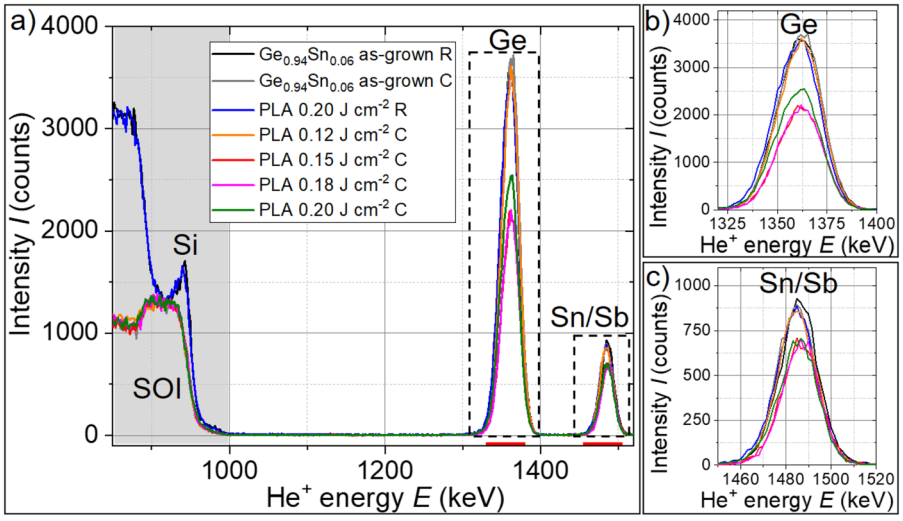

FIG. 5. RBS-R/C results of $Ge_{0.94}Sn_{0.06}$ on SOI in the as-grown state and after PLA with 0.12, 0.15, 0.18, and 0.20 J cm^{-2} (a). The marked dashed windows in (a) show the enlargements of the Ge (b) and Sn/Sb (c) contributions of $Ge_{1-x}Sn_x$. The spectra of Sn and Sb are superimposed, and the contributions from the SOI substrate are indicated by the gray background.

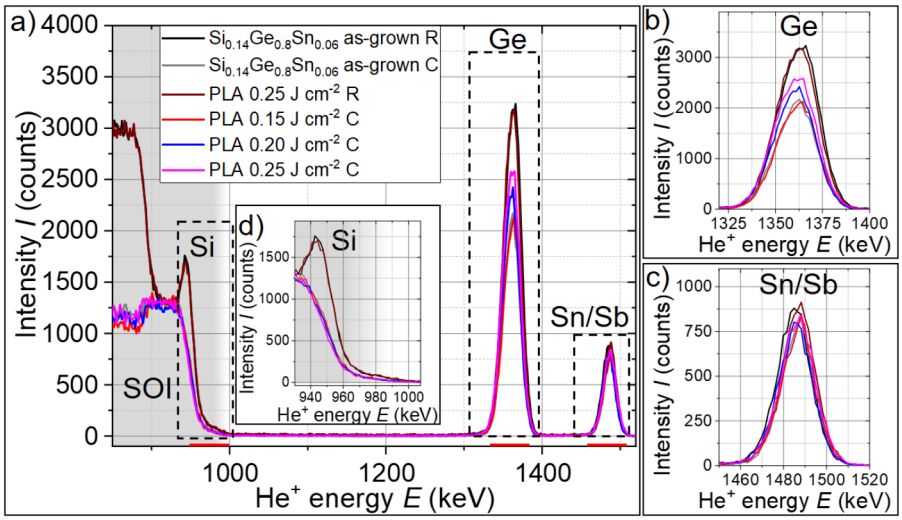

FIG. 6. RBS-R/C results of $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI in the as-grown state and after PLA with 0.15, 0.20, and 0.25 J cm^{-2} (a). The marked dashed windows in (a) show the enlargements of the Ge (b), the superimposed Sn/Sb (c), and the Si (d) contributions. The contributions from the SOI substrate, indicated by the grey background, superimpose the Si contribution from the $Si_{1-x-y}Ge_ySn_x$ layer.

$E_d \geq 0.15$ J cm^{-2} causes a slight de-channeling compared to the $Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown state.

The RBS-R/C spectra were quantitatively analyzed by calculating the channeling yield χ for Si, Ge, and Sn with Eq. (4), and the substitutional fraction ξ of Sn/Sb on Ge lattice sites $\xi_{Sn/Sb,Ge}$ by Eq. (5),

$$\chi = \frac{A_C}{A_R}. \tag{4}$$

Here, A_c is the integrated area under the channeling curve and A_R is the integrated area under the random curve,

$$\xi_{Sn/Sb,Ge} = \frac{(1-\chi_{Sn/Sb})}{(1-\chi_{Ge})}. \tag{5}$$

In general, the obtained χ_{Si}, χ_{Ge}, and $\chi_{Sn/Sb}$ of the fabricated $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ in Table I are relatively high because of (i) the observed defects in Figs. 1 and 2 can displace the atomic lattice positions, (ii) the superposition of crystal channeling with de-channeling events from surface defects, and (iii) the formation of the thicker $Ge_{1-x}Sn_x$- or $Si_{1-x-y}Ge_ySn_x$-oxide layer after PLA [see Figs. 2(a) and 2(b)]. The presence of this oxide layer might be avoidable if the PLA process is performed under an inert gas atmosphere or *in situ* in an MBE cluster tool. The $\xi_{Sn/Sb,Si}$ calculation results for the incorporation of Sn/Sb on Si substitutional sites are not presented since the superposition of the Si signal with the top Si and SiO_2 tail regions of the SOI causes errors in the χ_{Si} result.

The appearance of channeling in the $Ge_{1-x}Sn_x$ microstructure and the SOI beneath suggest epitaxial recrystallization or regrowth during the PLA process. The lowest channeling yields in Table I were achieved after PLA with 0.15 and 0.18 J cm^{-2} with $\chi_{Ge} \approx 60\%$ and $\chi_{Sn/Sb} \approx 75\%$. Additionally, the occupation of Sn/Sb on Ge lattice sites with $\xi_{Sn/Sb,Ge} = 59.6\%$ and 66.4% also suggests a reasonable amount of incorporated/activated Sn/Sb atoms on substitutional lattice sites. However, further increasing the PLA to $E_d = 0.20$ J cm^{-2} causes de-channeling in Ge and Sn/Sb. For $Si_{0.14}Ge_{0.80}Sn_{0.06}$, the best channeling properties were observed for the as-grown state. However, the direct comparison of Figs. 1(f) and 2(f) clearly shows an improved crystal structure. Hence, the channeling in $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ is most likely systematically overestimated due to the earlier-mentioned de-channeling effects (oxide layer, and surface defects).

The dopant concentration and distribution in dependence of the PLA E_d were investigated by SIMS and Hall-effect measurements. The SIMS results in Figs. 7 and 8 show the element depth distribution before and after annealing. All *in situ*-doped $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ on SOI samples have a relatively homogeneous Sb intensity profile despite the surface-related

TABLE I. RBS analysis results of $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layers on SOI in the as-grown and PLA-treated states. The minimum channeling yield for Si χ_{Si}, Ge χ_{Ge}, and Sn/Sb $\chi_{Sn/Sb}$, as well as the substitutional fraction of Sn/Sb on Ge lattice sites $\xi_{Sn/Sb,Ge}$ is calculated by Eqs. (4) and (5). The integration intervals are marked with red horizontal section lines in Figs. 5(a) and 6(a) and are between 950 and 1000 keV for Si, 1340 and 1390 keV for Ge, and 1465 and 1515 keV for Sn/Sb.

Sample	χ_{Si} (%)	χ_{Ge} (%)	$\chi_{Sn/Sb}$ (%)	$\xi_{Sn/Sb,Ge}$ (%)
$Ge_{0.94}Sn_{0.06}$ as-grown	…	100.0	97.8	0
$Ge_{1-x}Sn_x$ PLA 0.15 J cm^{-2}	…	60.6	76.5	59.6
$Ge_{1-x}Sn_x$ PLA 0.18 J cm^{-2}	…	58.9	72.7	66.4
$Ge_{1-x}Sn_x$ PLA 0.20 J cm^{-2}	…	71.2	79.6	70.7
$Si_{0.14}Ge_{0.80}Sn_{0.06}$ as-grown	48.2	58.8	80.5	47.2
$Si_{1-x-y}Ge_ySn_x$ PLA 0.15 J cm^{-2}	52.2	63.1	84.3	42.7
$Si_{1-x-y}Ge_ySn_x$ PLA 0.20 J cm^{-2}	53.4	71.6	87.4	44.2
$Si_{1-x-y}Ge_ySn_x$ PLA 0.25 J cm^{-2}	52.4	79.0	93.7	30.0

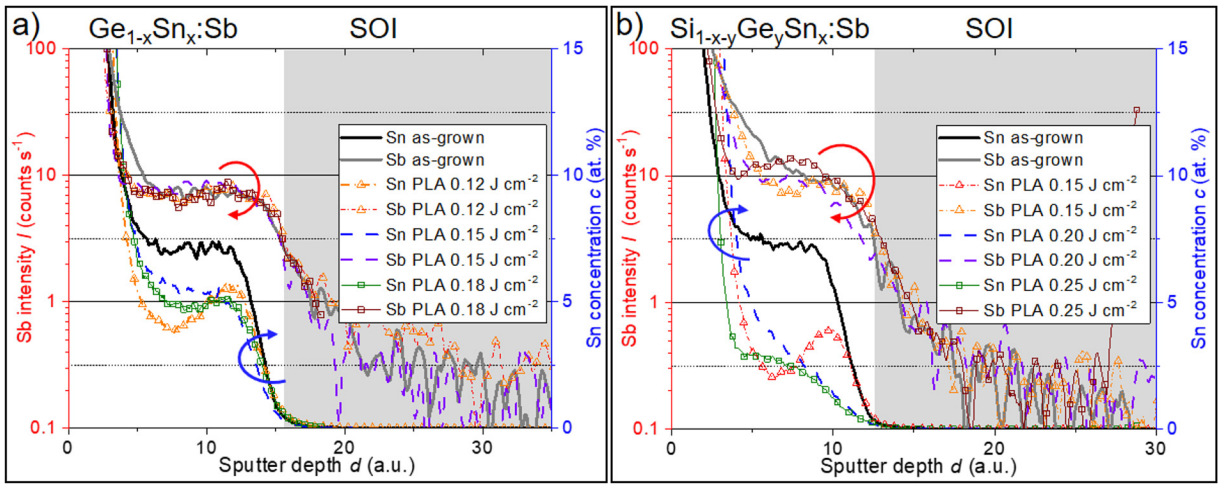

FIG. 7. Sb and Sn depth distributions of $Ge_{1-x}Sn_x$ on SOI (a) and $Si_{1-x-y}Ge_ySn_x$ on SOI (b) in the as-grown state and after PLA measured by TOF-SIMS. The Si layer beneath the alloy is colored in gray. The sputter depth was aligned to the Ge and Si crossover at the alloy/SOI interface shown in Fig. 8. A relative error within the given Sn concentration of ±1 at. % is expected.

amplitude (see Fig. 7). Unfortunately, the Sn concentration appears as slightly reduced after PLA.

The Si and Ge profiles of the $Ge_{1-x}Sn_x$ samples in Fig. 8(a) are relatively homogenous, but the $Si_{1-x-y}Ge_ySn_x$ layers show a redistribution of Ge and Si after PLA in Fig. 8(b). Furthermore, the PLA 0.15 J cm^{-2} state shows a small kink close to the SOI interface. This kink is related to the almost PLA-unaffected $Si_{1-x-y}Ge_ySn_x$ layer, which correlates with the weak intensity signal below the main SiGeSn 2 2 4 reflection in Fig. 4(b). The sample annealed with 0.20 J cm^{-2} shows a relatively constant Ge concentration while Sn increases and Si decreases toward the surface. The slightly varying chemical composition across the layer thickness and the different crystal qualities influence the sputter yield and might reduce the accuracy in the quantitative SIMS analysis. This could be the reason for the slightly overestimated Sn concentration in the as-grown states in Fig. 7. After annealing with 0.15 and 0.25 J cm^{-2},

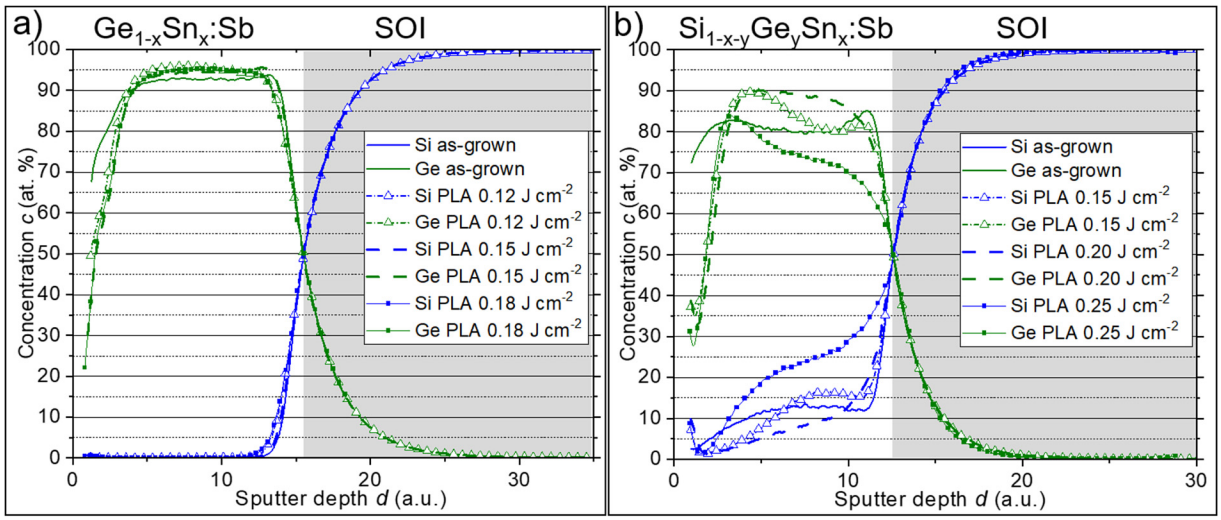

FIG. 8. Ge and Si depth distribution of $Ge_{1-x}Sn_x$ on SOI (a) and $Si_{1-x-y}Ge_ySn_x$ on SOI (b) in the as-grown state and after PLA measured by TOF-SIMS. The Si layer beneath the alloy is colored in gray. The sputter depth was aligned to the Ge and Si crossover at the alloy/SOI interface.

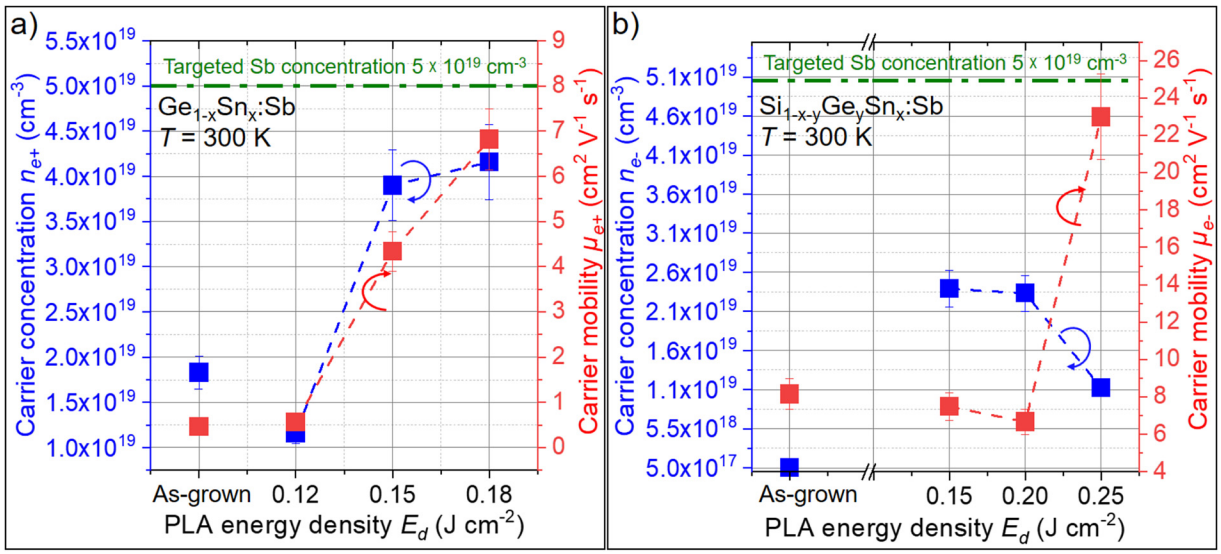

FIG. 9. Active electron concentrations n_{e-} and mobilities μ_{e-} of $Ge_{1-x}Sn_x$ (a) and $Si_{1-x-y}Ge_ySn_x$ (b) determined by Hall-effect measurements at 300 K for the as-grown states ($E_d = 0$ J cm^{-2}) and after post-growth PLA with different energy densities E_d.

a redistribution of Si toward the SOI interface and a Ge diffusion toward the surface is visible.

The Hall-effect results of the $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ layers before and after post-growth PLA are shown in Fig. 9. The carrier concentrations in the as-grown states are 1.8×10^{19} cm^{-3} ($Ge_{0.94}Sn_{0.06}$) and 5.1×10^{17} cm^{-3} ($Si_{0.14}Ge_{0.80}Sn_{0.06}$). After PLA with $E_d \geq 0.15$ J cm^{-2}, a significant amount of Sb could be activated in both alloys. In the case of $Ge_{1-x}Sn_x$, active carrier concentrations of 3.9×10^{19} cm^{-3} (0.15 J cm^{-2}) and 4.2×10^{19} cm^{-3} (0.18 J cm^{-2}) were determined, which are close to the targeted absolute Sb concentration of 5×10^{19} cm^{-3}. Additionally, the carrier mobility increased from 0.5 cm^2 V^{-1}s^{-1} in the $Ge_{0.94}Sn_{0.06}$ as-grown state to 6.8 cm^2 V^{-1}s^{-1} after PLA with 0.18 J cm^{-2}. The simultaneous increase of n_{e-} and μ_{e-} after PLA is related to the higher crystal quality. In the $Si_{1-x-y}Ge_ySn_x$ case, n_{e-} could be increased up to 2.3×10^{19} cm^{-3} ($E_d = 0.15$ J cm^{-2}). However, a too high PLA energy density reduces the active carrier concentration, as shown for $Si_{1-x-y}Ge_ySn_x$ with $E_d = 0.25$ J cm^{-2}. On the other hand, the reduced n_{e-} increased μ_{e-} from 6.7 cm^2 V^{-1}s^{-1} (PLA with $E_d = 0.20$ J cm^{-2}) to 23.0 cm^2 V^{-1}s^{-1} after PLA with $E_d = 0.25$ J cm^{-2} due to a deactivation of dopants.

IV. CONCLUSION

The studied $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ films grown on SOI substrates are almost strain-relaxed and contain many defects since the layer thickness exceeds the critical thickness for plastic strain relaxation. Partially replacing Ge by Si reduces the lattice mismatch between the alloy and the Si substrate from about 5.3% ($Ge_{0.94}Sn_{0.06}$) to about 1.9% ($Si_{0.14}Ge_{0.80}Sn_{0.06}$) and helps us to improve the crystal structure. Post-growth PLA improves the layer quality significantly and activates up to 80% of the Sb-donors. However, annealing under ambient conditions generates an Sn-containing oxide on the surface and slightly redistributes Si, Ge, and Sn, especially for the ternary $Si_{1-x-y}Ge_ySn_x$ alloy.

Overall, it can be concluded that the $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ grown directly on SOI layers contain many defects, which is a challenge for their application as an active component in opto- or nanoelectronic devices. Hence, it is suggested to use a post-growth treatment to mediate between the large lattice mismatch of the alloy and the substrate. Such a treatment should be performed in an inert atmosphere or vacuum to avoid oxide formation. The results show that PLA of Sn-containing group-IV alloys on SOI wafers is an efficient way to fabricate $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ alloys compatible with CMOS technology on an insulating platform.

SUPPLEMENTARY MATERIAL

See the supplementary material for supplements that support the presented XRD findings. Section A discusses a possible tilt between the top silicon and the Si carrier substrate of the SOI wafer. Section B shows and explains additional 0 0 4 HR-XRD results, which support the discussed 2 2 4 XRD-RSM data. Furthermore, vertical EDXS line scans of $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ in the as-grown state and after PLA are presented in Sec. C.

ACKNOWLEDGMENTS

This work was partially supported by the Bundesministerium für Bildung und Forschung (BMBF) under the project "ForMikro": Group-IV heterostructures for high-performance nanoelectronic devices (SiGeSn NanoFETs) (Project-ID: 16ES1075). We gratefully

acknowledge the HZDR Ion Beam Centre for their support with RBS. The authors thank Annette Kunz for TEM specimen preparation. Furthermore, the use of the HZDR Ion Beam Center TEM facilities and the funding of TEM Talos by the Bundesministerium für Bildung und Forschung (BMBF), Grant No. 03SF0451, in the framework of HEMCP are acknowledged. We thank Dr. Olav Hellwig and his group at HZDR for providing access to the x-ray diffractometer.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

O. Steuer: Conceptualization (equal); Formal analysis (equal); Investigation (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **D. Schwarz:** Writing – review & editing (supporting). **M. Oehme:** Writing – review & editing (supporting). **F. Bärwolf:** Data curation (supporting); Formal analysis (supporting); Investigation (supporting); Validation (supporting); Writing – review & editing (supporting). **Y. Cheng:** Investigation (equal). **F. Ganss:** Data curation (equal); Formal analysis (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **R. Hübner:** Data curation (supporting); Formal analysis (supporting); Validation (supporting); Visualization (equal); Writing – review & editing (supporting). **R. Heller:** Formal analysis (supporting); Writing – review & editing (supporting). **S. Zhou:** Formal analysis (supporting); Supervision (supporting); Validation (supporting); Writing – review & editing (supporting). **M. Helm:** Supervision (supporting); Writing – review & editing (supporting). **G. Cuniberti:** Supervision (supporting). **Y. M. Georgiev:** Funding acquisition (equal); Project administration (equal); Supervision (equal); Visualization (supporting); Writing – review & editing (supporting). **S. Prucnal:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Supervision (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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