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Optimization of technology processes for enhanced CMOS-integrated 1T-1R RRAM device performance

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Abstract. Implementing artificial synapses that emulate the synaptic behavior observed in the brain is one of the most critical requirements for neuromorphic computing. Resistive random-access memories (RRAM) have been proposed as a candidate for artificial synaptic devices. For this applicability, RRAM device performance depends on the technology used to fabricate the metal–insulator–metal (MIM) stack and the technology chosen for the selector device. To analyze these dependencies, the integrated RRAM devices in a 4k-bit array are studied on a 200 mm wafer scale in this work. The RRAM devices are integrated into two different CMOS transistor technologies of IHP, namely 250 nm and 130 nm and the devices are compared in terms of their pristine state current. The devices in 130 nm technology have shown lower number of high pristine state current devices per die in comparison to the 250 nm technology. For the 130 nm technology, the forming voltage is reduced due to the decrease of HfO_2 dielectric thickness from 8 nm to 5 nm. Additionally, 5% Al-doped 4 nm HfO_2 dielectric displayed a similar reduction in forming voltage and a lower variation in the values. Finally, the multi-level switching between the dielectric layers in 250 nm and 130 nm technologies are compared, where 130 nm showed a more significant number of conductance levels of seven compared to only four levels observed in 250 nm technology.

1 Introduction

The emergence of artificial intelligence and the Internet of Things has resulted in a drastic increase in the amount of data that needs to be handled by computers, which places specific constraints on computing and energy efficiency. The von Neumann architecture is efficient for linear and sequential data processing. However, this does not prove to be efficient for programs that are dependent on frequent access to memory [1]. The efficiency is limited because the processing unit is separated from the memory unit, resulting in the memory wall phenomenon, where data-intensive computations need frequent memory access, and this physical limitation increases the time taken to access data and, consequently, the power consumption [2,3]. To overcome this challenge, neuromorphic computing is proposed as a solution inspired by the working functionality of the human brain's low power consumption in handling vast amounts of data [4]. It involves replicating the parallel network architecture of neurons and synapses observed in the brain, with neurons being the computing elements and memory elements behaving as the synapses [5]. In this regard, synaptic plasticity is a substantial prerequisite that needs to be fulfilled by artificial synapses [6]. Other requisites include non-volatile memory storage, low operation voltage, endurance of up to 10^{10} cycles, and high integration density [7–9].

Resistive random-access memory (RRAM) devices comply with most of the requirements mentioned for synaptic devices. Apart from the CMOS-compatible materials used for RRAM devices, their simple Metal-Insulator-Metal (MIM) structure makes them easier to integrate into CMOS technology, enabling a continuous scaling and increased device density [10]. Another requisite fulfilled by RRAM technology is its ability to

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store multiple bits in a single RRAM cell, enabling the required synaptic plasticity [11,12]. Due to these inherent advantages, RRAM technology has garnered attention in various computing applications such as artificial neural networks, scientific computing, and image processing [13]. Commercial foundries such as TSMC that offer RRAM in their technology platforms for automotive applications further emphasize the growing interest in implementing RRAM at an industrial scale [14].

To realize an array of memristive devices for neuromorphic computing applications, it is essential that each cell can be individually selected and be unaffected by the sneak path currents. Hence, a transistor is connected in series to each cell to prevent the sneak path current and have the most negligible effect on the operation of the device [15]. Choosing the right transistor technology is essential for RRAM-related computing applications since the transistor also acts as a selector device and sets the limits of write current through the device. The dimensions of the transistor technology chosen also determine the 1T-1R device dimensions and, finally, the maximum achievable area of the array [16,17]. Within the MIM stack, the device properties, such as operation voltage range, reliability, endurance, multi-level switching, device-to-device variations, memory window, etc., are influenced by the choice of the metal electrodes and the dielectric layer [18–20].

This study investigates the RRAM device performance dependence on the transistor technology chosen and the influence of the dielectric layer's thickness and doping. The obtained device performance characteristics are essential for its application as synaptic devices in neuromorphic computing. The fabrication of the RRAM devices in the corresponding CMOS technology and the parameters of electrical characterization are detailed in Sect. 2. Section 3 discusses the performance results comparing the two of IHP's CMOS technologies, 250 nm and 130 nm, based on the pristine state currents of the devices, forming voltages and multi-level switching capabilities. This section also briefly mentions the fabrication steps modified to obtain improved characteristics of MIM stack in the memristor device. Section 4 summarizes the results of this study.

2 Methods

2.1 Fabrication

The RRAM devices utilized in this study are integrated into a 4k-bit memory array. These devices are fabricated according to the 250 nm and 130 nm technologies of the IHP's CMOS fabrication line. Each RRAM device in the array consists of a NMOS transistor (1T) whose drain contact is connected in series to a MIM (1R) structure. The dimensions of the transistor are L = 240 nm and W = 1,140 nm for 250 nm technology and L = 130 nm and W = 1000 nm for 130 nm technology. The MIM structure is integrated between the Metal 2 and Metal 3 levels, consisting of TiN/dielectric layer/Ti/TiN stack. The bottom and top metal (TiN) electrodes are 150 nm thick and were deposited by magnetron sputtering. A 7 nm thick titanium (Ti) layer acting as a scavenging layer was deposited above the dielectric using magnetron sputtering. The dielectric layers studied here are HfO_2 and aluminum-doped HfO_2 (Al:HfO_2). The thickness of the dielectric layer varied among 8 nm, 6 nm, and 5 nm, whereas the aluminum doping percentages varied among 5% and 10%. All dielectric layers were deposited using atomic layer deposition (ALD) at 300 °C. Hafnium tetrachloride ($HfCl_4$), and water (H_2O) were used as the precursors to deposit HfO_2. Aluminum doping of the HfO_2 layers was achieved by pulsing trimethylaluminum (TMA) at specific intervals during the HfO_2 deposition process. Cross-sectional TEM images of 1T-1R devices in 250 nm and 130 nm technologies are shown in Fig. 1.

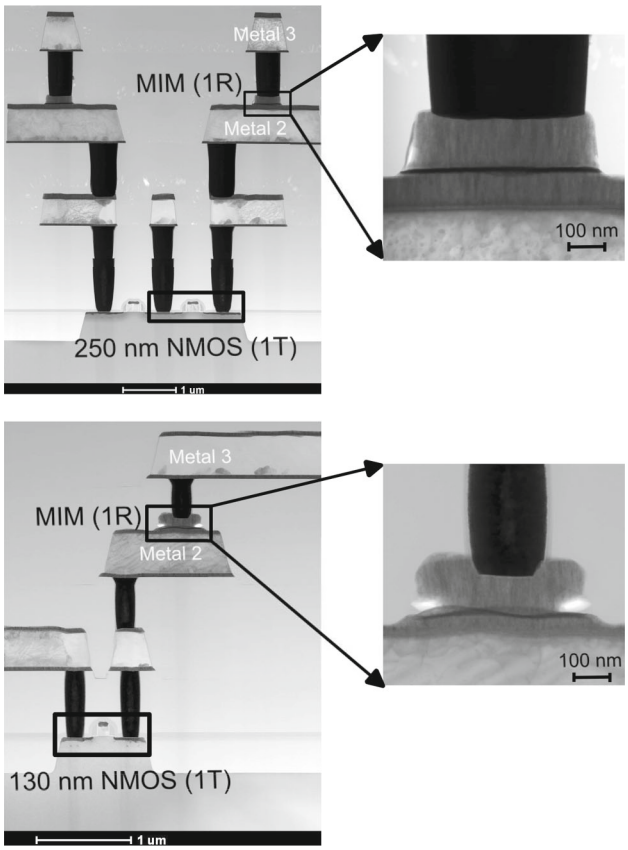

Fig. 1 Cross-sectional TEM images of 1T-1R devices along with magnified images of MIM stack in 250 nm technology (above) and in 130 nm technology (below)

2.2 Electrical characterization

The 4k-bit memory arrays were measured on 200 mm wafers. A schematic representation of the 1T-1R cell indicating the respective source line (SL), word line (WL), and bit line (BL) terminals is shown in Fig. 2. The wafers consisting of 8 nm HfO_2 and 6 nm Al:HfO_2 10% of Al as the dielectric layer had 61 dies each. The

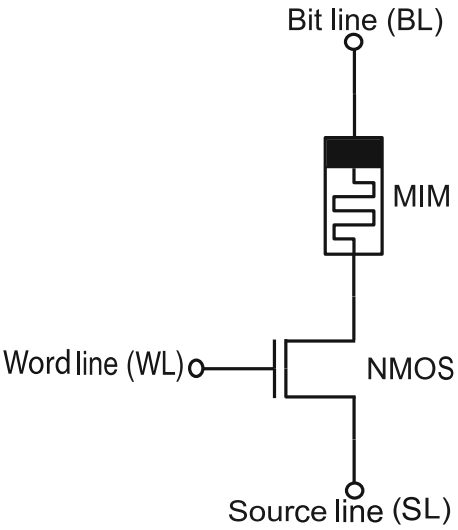

Fig. 2 Schematic representation of a 1T-1R cell integrated into the 4k-bit array

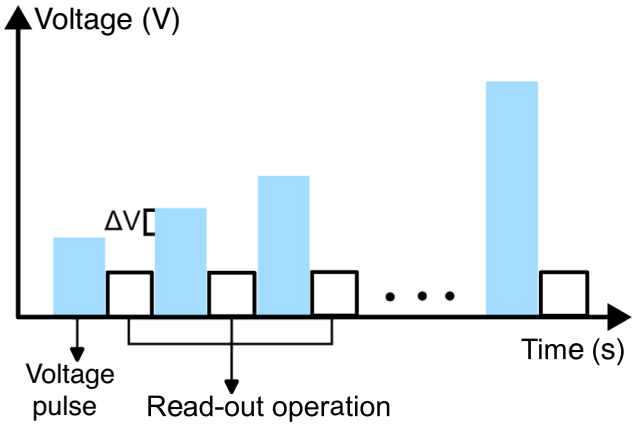

Fig. 3 Schematic of the ISPVA algorithm

wafers consisting of 5 nm HfO_2 and 4 nm Al:HfO_2 5% of Al as the dielectric layer, fabricated in 130 nm technology had 91 dies each.

Initially, the pristine state current of the MIM devices in each die was measured by performing a read-out operation at 0.2 V. The forming, reset and set operations were performed using the Incremental Step Pulse with Verify Algorithm (ISPVA), which has been shown to reduce device-to-device variability and obtain reliable multi-level switching [21]. The algorithm consists of a sequence of input voltage pulses in increasing amplitude for a constant predefined time duration defined as pulse width (PW). The input voltage pulses are applied until the threshold current (TC) is reached or if the specified maximum input voltage is reached. After each step of incremental input voltage, a read-out operation is performed at 0.2 V. The voltage applied at the WL terminal defines the current compliance. The combination of WL voltage and TC defines the resistance state programmed. A schematic of the ISPVA algorithm is shown in Fig. 3. The sequence of voltage pulses is applied at the BL terminal for forming and set operations. In contrast, it is applied at the SL terminal for the reset operation. The measurement conditions used for each operation are summarized sequentially in Table 1 for 250 nm technology and Table 2 for 130 nm technology. The tables describe the input voltage applied at SL, WL, and BL terminals as well as the TC and PW values during each measurement operation.

The usage of compact models that can accurately predict the behavior of device switching characteristics obtained from the electrical characterization is significant for their implementation in the process design kits for fabrication purposes. The device models used to simulate the device characteristics are explained in detail for 250 nm technology in [22] and for 130 nm technology in [23].

3 Results and discussion

3.1 Dependence of RRAM device performance on the fabrication technology

The pristine state current of the RRAM devices was the initial parameter chosen to compare the difference between the two RRAM technologies. This is an important parameter for assessing the device performance since the current in the pristine state determines both the number of leaky devices and the forming voltages of the device [24]. It has been observed that high pristine state currents lead to low breakdown voltages in MIM devices [25]. The pristine state currents above 1 μ A is considered as leaky. The percentage of leaky devices is calculated for each die, and a wafer map is created, indicating the percentage of the leaky devices.

Figure 4 depicts the wafer maps representing the percentage of leaky devices in 250 nm technology and 130 nm technology with 8 nm HfO_2 as the dielectric layer. It can be observed that there is a strong reduction of the number of leaky devices in 130 nm technology compared to 250 nm technology. Out of 61 dies, 30 show more than 20% of leaky devices per die in 250 nm technology; in contrast, all dies in 130 nm technology have below 20% of leaky devices per die. Figure 5 shows similar wafer maps for 6 nm Al:HfO_2 10% of Al as the dielectric layer. In this case too, there is a similar trend of great improvement in terms of leaky devices in 130 nm technology compared to 250 nm technology, as observed for 8 nm HfO_2. These results indicate that irrespective of the dielectric layer chosen, the percentage of leaky devices per die is significantly lower in 130 nm technology. Therefore, the use of the 130 nm technology to integrate the RRAM devices is a significant improvement compared to 250 nm technology. Besides the reduced number of leaky devices, the shorter transistor gate length also provides an additional advantage of reduced device area footprint, an essential requirement for hardware-level applications.

After the pristine state current measurement, the forming operation was performed on the devices that

Table 1 Measurement conditions used for characterizing devices in 250 nm technology

Operation	SL (V)	WL (V)	BL (V)	PW (μ s)	TC (μ A)
Pristine state current	0	1.7	0.2	1	–
Forming	0	1.6	2.0–5.0 (ΔV = 0.01)	10	40
Reset	0.2–3.5 (ΔV = 0.1)	2.7	0	1	5
Set LRS1	0	1.2	0.2–3.5 (ΔV = 0.1)	1	20
Set LRS2	0	1.4	0.2–3.5 (ΔV = 0.1)	1	30
Set LRS3	0	1.6	0.2–3.5 (ΔV = 0.1)	1	40

Table 2 Measurement conditions used for characterizing devices in 130 nm technology

Operation	SL (V)	WL (V)	BL (V)	PW (μ s)	TC (μ A)
Pristine state current	0	1.35	0.2	1	–
Forming	0	1.35	2.0–3.5 (ΔV = 0.01)	10	60
Reset	0.5–2.0 (ΔV = 0.1)	2.3	0	1	5
Set LRS1	0	0.7	0.5–2.0 (ΔV = 0.1)	1	10
Set LRS2	0	0.8	0.5–2.0 (ΔV = 0.1)	1	20
Set LRS3	0	0.85	0.5–2.0 (ΔV = 0.1)	1	30
Set LRS4	0	0.95	0.5–2.0 (ΔV = 0.1)	1	40
Set LRS5	0	1.05	0.5–2.0 (ΔV = 0.1)	1	50
Set LRS6	0	1.25	0.5–2.0 (ΔV = 0.1)	1	60

were non-leaky. Forming is the most crucial step since it defines the formation of the conductive filaments for the first time in a device. These filaments are broken and formed again using reset and set operations by switching the device into a High Resistance State (HRS) and Low Resistance State (LRS) respectively [26,27]. Figure 6 shows the cumulative distribution functions (CDFs) of the forming voltages for the dielectric layers used in 250 nm and in 130 nm technology (none of the devices formed for 6 nm Al:HfO_2 10% of Al in 130 nm technology). The two types of dielectric layers in 250 nm technology (8 nm HfO_2 and 6 nm Al:HfO_2 10% of Al) show similar behavior where the forming voltages of the devices are distributed between 2.7 V and 5.0 V in an approximately linear trend. Although the forming voltage distribution is similarly varied for 8 nm HfO_2 in 130 nm technology, namely, between 3.1 V - 5.0 V, the CDF trend is much steeper, indicating lower dispersion of the forming voltage values for at least 80% of the devices within the range of 3.1 V - 4.0 V.

Once the forming operation of the devices was complete, the first reset and set operations were performed to segregate the devices that did not switch back to the HRS. Yield was calculated as a percentage of the devices that switched to the LRS during the first set cycle out of all the successfully formed devices during the forming operation. Table 3 shows the yield of devices in both technologies, indicating that the better choice for the 8 nm HfO_2 dielectric layer is the 130 nm technology.

Apart from the possible effect of changing the transistor when changing the technology, the approach used to fabricate MIM also plays a significant role for improved RRAM device performance, as studied in [25]. One of the standard approaches to fabricating the MIM stack once the layers of the stack are deposited was to pattern the top electrode and subsequent resist removal and dry etch steps to pattern the dielectric layer. Followed by the deposition of the $Si_xN_yO_z$ encapsulation layer, patterning and etch steps are followed to obtain a fully patterned MIM stack. This approach was modified by accommodating the spacers for the sidewalls of the top electrode before etching the dielectric layer. A schematic of the two types of fabrication approaches is shown in Fig. 7. MIM devices fabricated using the spacer and encapsulation approach have lower pristine state currents than devices fabricated with only an encapsulation layer. They also tend to have lower variations in forming voltages, set voltages and higher memory windows after cycling. This improvement in device characteristics is attributed to the reduced oxidation (prevented formation of the Ti-containing polymers) on the side walls of the top electrode, thus causing lower pristine state currents in MIM devices [25].

3.2 Optimization of the dielectric layer

According to the results in Fig. 6, the voltages for the forming operation in HfO_2 (8 nm) are beyond the specified voltage values for 130 nm technology. The forming voltage values are even higher according to the yield obtained in Al:HfO_2 in 130 nm technology. Therefore, the recipes of the dielectric had to be optimized. Figure 8 shows the wafer maps of the percentage of leaky devices in each die for 5 nm HfO_2 and 4 nm Al:HfO_2 5% of Al dielectric layers in 130 nm technology. The wafer maps for 8 nm HfO_2 and 6 nm Al:HfO_2 10% of Al in 130 nm technology are shown in Figs. 4 and 5, respectively. In line with the wafer maps of leaky devices per die observed in 130 nm technology, here, the percentage

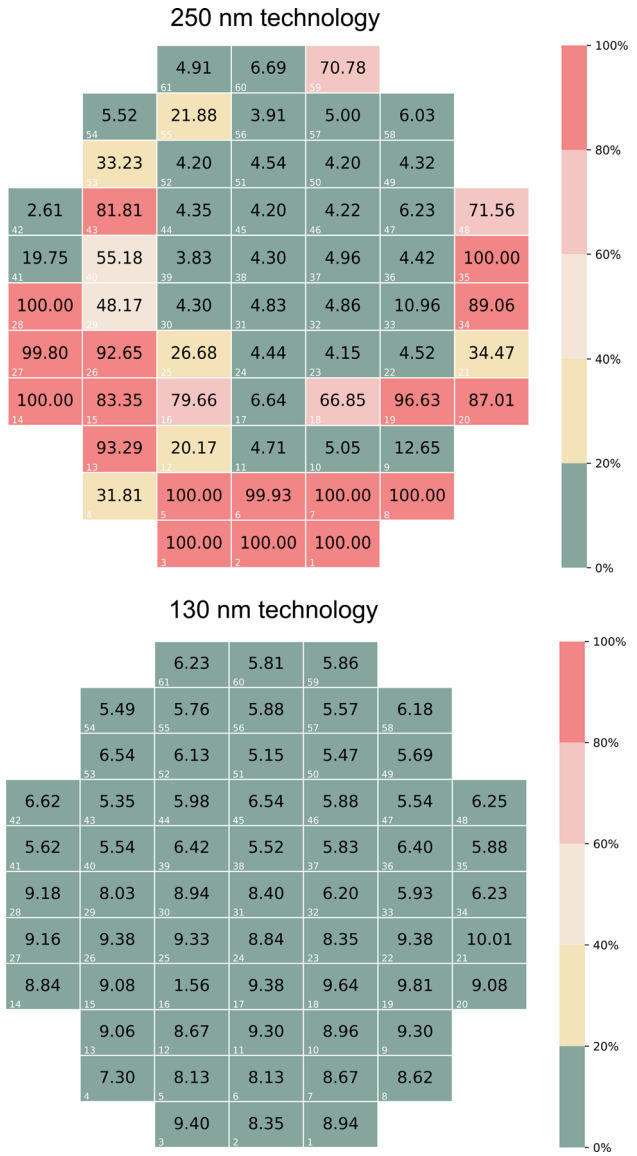

Fig. 4 Wafer maps representing the percentage of leaky devices in each die for the wafers consisting of 8 nm HfO_2 as the dielectric layer in 250 nm technology (above) and in 130 nm technology (below)

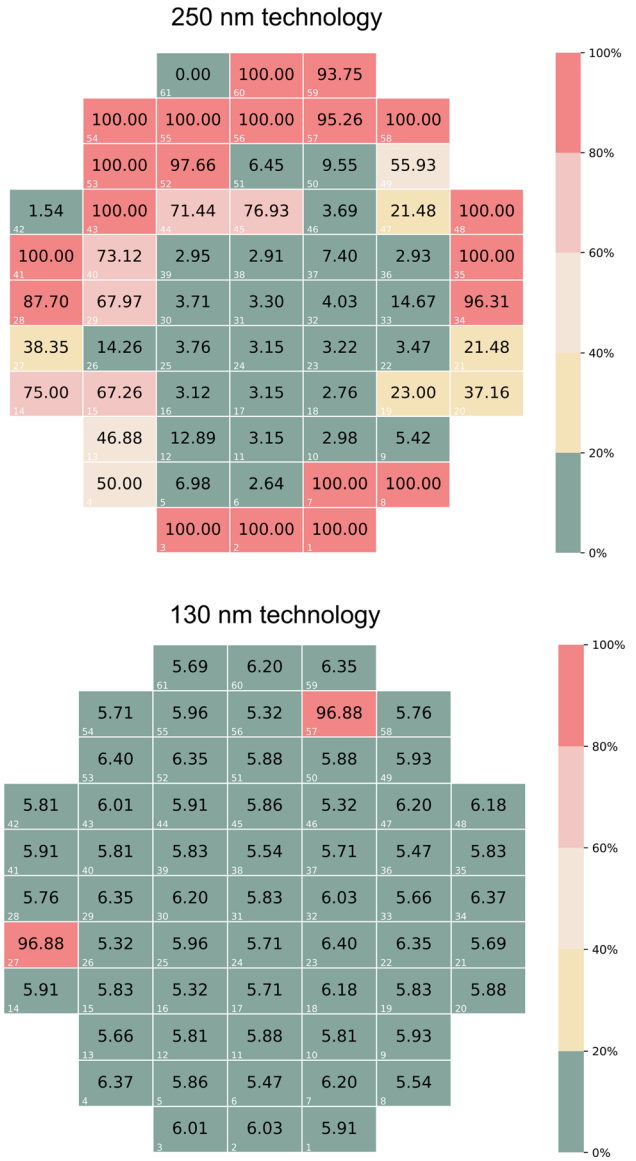

Fig. 5 Wafer maps representing the percentage of leaky devices in each die for the wafers consisting of 6 nm Al:HfO_2 10% of Al as the dielectric layer in 250 nm technology (above) and in 130 nm technology (below)

of leaky devices is also below 20% in each die for both variants of the dielectric layer.

The CDFs of forming voltages for the three different dielectric layers in 130 nm technology are shown in Fig. 6. It is distinctly observed that the forming voltage distribution of 8 nm HfO_2 is higher than the thinner dielectric layers. This is because the average forming voltage decreases due to the reduction in dielectric breakdown strength as the dielectric layer thickness decreases [28]. Although the CDFs of forming voltage are similar between 5 nm HfO_2 and 4 nm Al:HfO_2 5% of Al, the trend is steeper for the latter, indicating lower variability. The forming voltage distribution reaching up to 5.0 V compromises the performance of the 130 nm NMOS, which is related to the decision to reduce the thicknesses in both recipes (HfO_2 and Al:HfO_2). Table 4 summarizes the yield calculated for the various dielectric layers in 130 nm technology. An outstanding yield of 99% is achieved by reducing the HfO_2 thickness and doping the layer with 5% aluminum.

3.3 Multi-level switching

Multi-level switching is a prominent advantage for RRAM application as a synaptic device since synaptic plasticity is achieved due to this phenomenon [6]. Hence, assessing the number of conductance levels achievable in a device is essential. The multi-level switching in RRAM devices was studied using the parameters specified in Tables 1 and 2 for 250 nm and

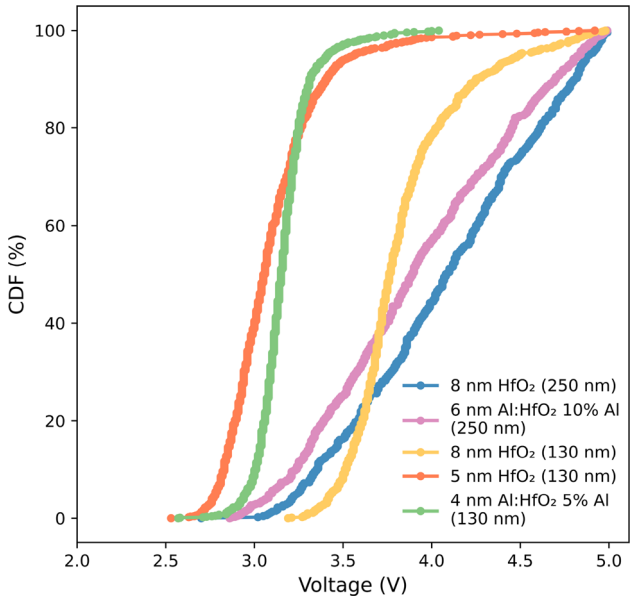

Fig. 6 CDFs of forming voltages in 250 nm and 130 nm technologies

Table 3 Yield comparison for 250 nm and 130 nm technologies

	250 nm	130 nm
8 nm HfO_2	58%	84%
6 nm Al:HfO_2 10% Al	85%	No devices formed

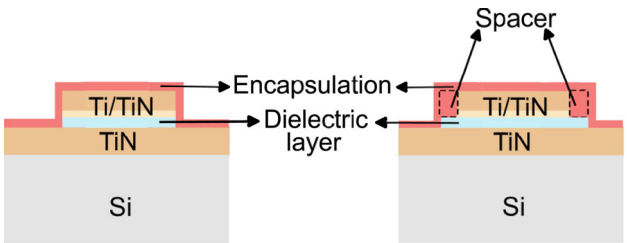

Fig. 7 Schematic of MIM device without encapsulation (left) and with spacer and encapsulation (right)

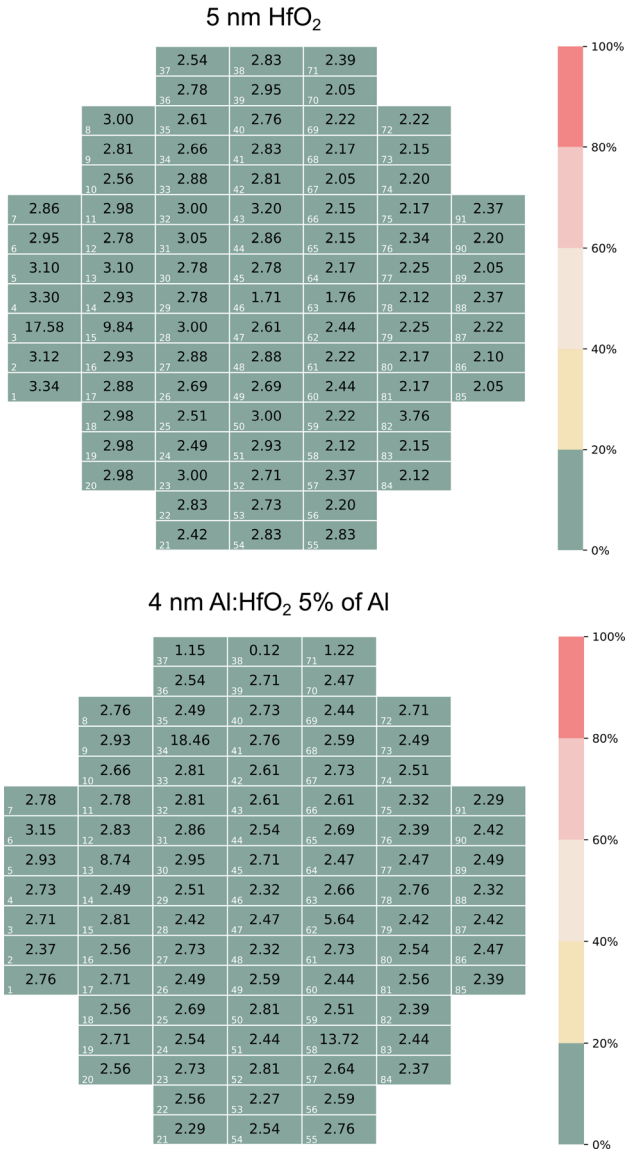

Fig. 8 Wafer maps representing the percentage of leaky devices in each die for the wafers consisting of 5 nm HfO_2 (above) and 4 nm Al:HfO_2 5% of Al as the dielectric layers in 130 nm technology

130 nm technologies, respectively. The read-out currents for the devices are measured after switching (AS) to respective conductance levels and after the end of algorithm (EA). Figure 9 shows the CDFs of read-out currents from devices in 250 nm technology for 8 nm HfO_2 and 6 nm Al:HfO_2 10% of Al. Four conductance levels are achieved: HRS, LRS1, LRS2, and LRS3 in the case of both the dielectric layers. The transition to each level is possible due to the interdependence of conductive filament size on the compliance current [29]. There is just a small overlap of conductance levels for both types of dielectric layers. However, the overlap is much more pronounced in the case of the HRS level. A drastic improvement in the number of conductance levels is achieved by transitioning to 130 nm technology, as shown in Fig. 10. Seven conductance levels are obtained for both dielectric layers (5 nm HfO_2 and 4 nm Al:HfO_2 5% of Al) with much less overlap in conductance levels compared to 250 nm technology. The HRS level seems much closer to ideal behavior in the case of 4 nm Al:HfO_2 5% of Al, which could be attributed to the fact that the conductive filaments formed due to oxygen vacancies are better controlled in the presence of dopants in the layer [30].

4 Conclusion

This study focused on studying the effect of the technology on RRAM device performance based on the param-

Table 4 Summary of yield for dielectric layer variants in 130 nm technology

Dielectric layer	Yield
8 nm HfO_2	84%
6 nm Al:HfO_2 10% Al	No devices formed
5 nm HfO_2	94%
4 nm Al:HfO_2 5% Al	99%

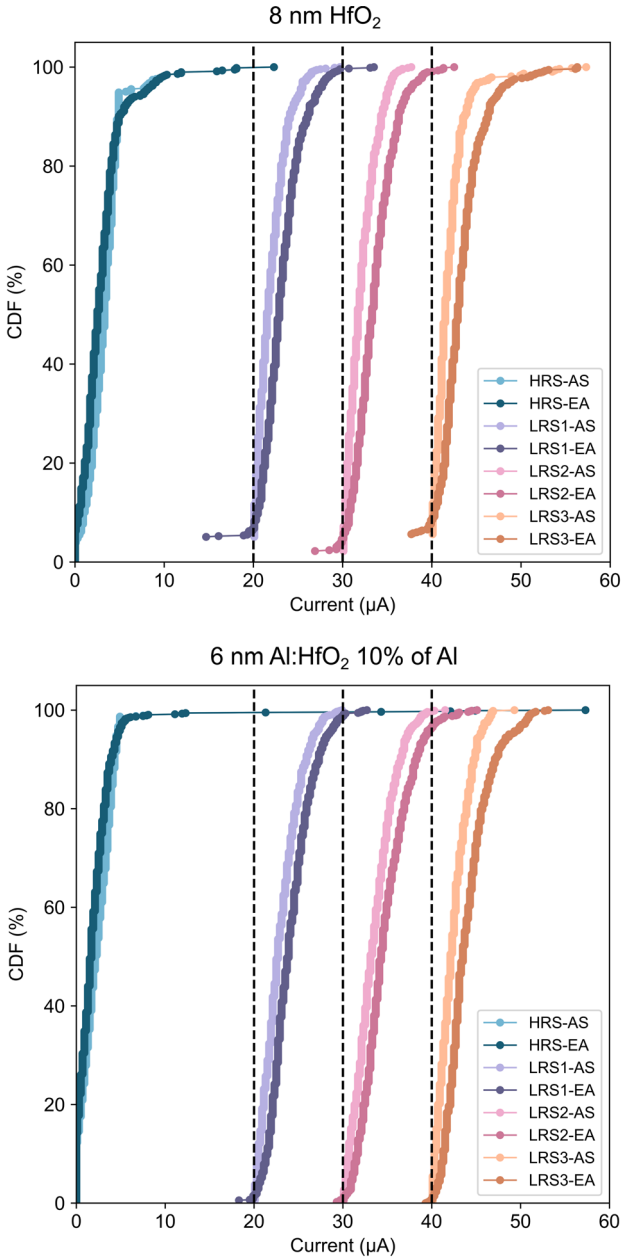

Fig. 9 CDFs of read-out currents measured after switching transition (AS) and at the end of the ISPVA algorithm (EA) for devices in 250 nm technology

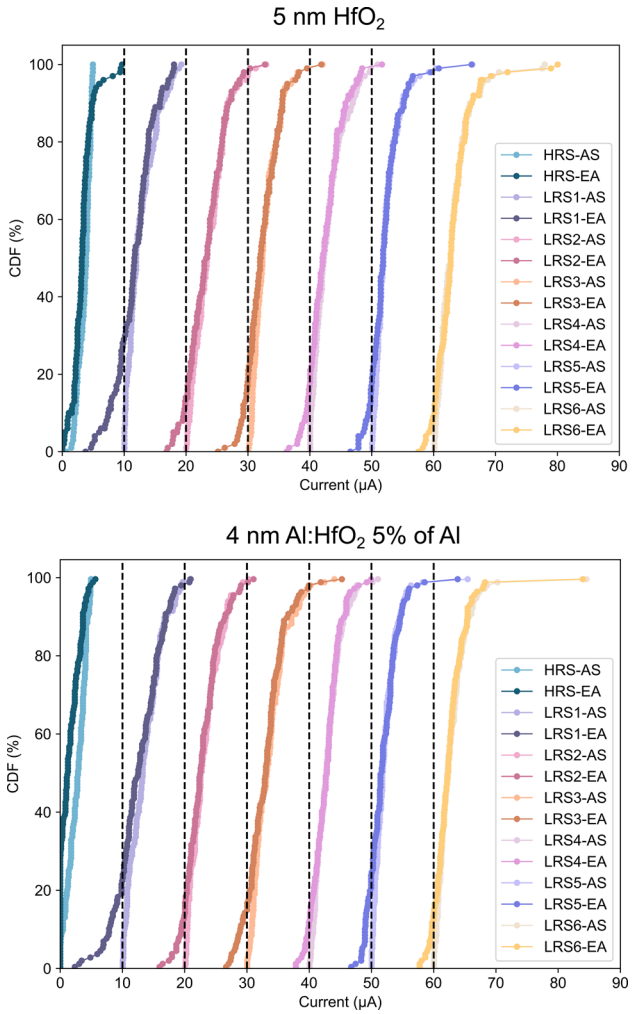

Fig. 10 CDFs of read-out currents measured after switching transition (AS) and at the end of the ISPVA algorithm (EA) for devices in 130 nm technology

eters of pristine state currents, forming voltages, yield and the ability to obtain multiple levels of switching, which are considered to be imperative for its application as synaptic devices. The 4k bit array devices used in this study were fabricated in 250 nm and 130 nm technologies. The technologies were compared using two different dielectric layers (8 nm HfO_2 and 6 nm Al:HfO_2 10% of Al) by assessing the pristine state currents of devices in each die. The 130 nm technology proved to be the better technology due to the lower percentage of leaky devices observed per die compared to 250 nm. The observation was similar, irrespective of the dielectric layers used in MIM. The forming voltage of the devices confirms the observation of 130 nm technology being better since devices in 130 nm had a steeper distribution in CDFs compared to devices in 250 nm technology. The number of devices that could switch to reset and set state after the forming step increased by 26% for 130 nm technology when compared to 250 nm technology. Further, by comparing four different dielectric layers in 130 nm technology (8 nm HfO_2, 6 nm

Al:HfO_2 10% of Al, 5 nm HfO_2, and 4 nm Al:HfO_2 5% of Al), it was seen that the forming voltage of the devices decreased when the thickness of the dielectric is reduced due to the reduction in dielectric breakdown strength easing the process of filament formation. Doping the HfO_2 dielectric with aluminum reduced the variation of forming voltage among the devices, and the CDF distribution was steeper than 5 nm HfO_2. Finally, multi-level switching between the technologies was studied. The 130 nm technology is advantageous since seven conductance levels were observed compared to four in 250 nm. Among the dielectric variants in 130 nm technology, the 4 nm Al:HfO_2 5% of Al performs better in the HRS state than 5 nm HfO_2 due to its steeper CDF distribution.

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Author contributions

Conceptualization: CW, EP and KDSR; electrical characterization: EP and AB; fabrication of devices: SM, MF, MKM, ML and KDSR; data visualization: KDSR; writing–original draft: KDSR; writing–review and editing: KDSR, EP, CW, MKM and AM; supervision: EP, CW, and AM.

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Data Availability Statement The data supporting this study will be made available upon reasonable request from the corresponding author.

Code Availability Statement Not applicable.

Declarations

Conflict of interest The authors have no relevant financial or non-financial interests to disclose.

Ethics approval and consent to participate Not applicable.

Materials availability Not applicable.

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