

# Wideband 240-GHz Transmitter and Receiver in BiCMOS Technology With 25-Gbit/s Data Rate

Mohamed Hussein Eissa<sup>1b</sup>, Andrea Malignaggi, Ruoyu Wang, Mohamed Elkhoully, Klaus Schmalz<sup>2b</sup>,  
Ahmet Cagrı Ulusoy<sup>3b</sup>, and Dietmar Kissinger, *Senior Member, IEEE*

**Abstract**—In this paper, a fully integrated wideband 240-GHz transceiver front-end, supporting BPSK modulation scheme, with on-chip antenna is demonstrated in SiGe:C BiCMOS technology with  $f_T/f_{\max} = 300/500$  GHz and local backside etching option. Within the transmitter, the upconversion is provided by fundamental mixing using a modified Gilbert cell mixer driven by a multiplier-by-eight local oscillator (LO) chain. The transmitter achieves a 3-dB RF bandwidth of 35 GHz with a saturated output power of  $-0.8$  dBm. The down converter is equipped with a mixer first architecture. The mixer is designed utilizing a transimpedance amplifier as load for enhanced noise and bandwidth performance. For dc-coupled receiver, two dc offset cancellation loops are implemented within the receiver chain. It achieves a 3-dB RF bandwidth of 55 GHz, minimum single-sideband noise figure (SSB NF) of 13.4 dB, and a gain of 32 dB with 25-dB gain control. A wideband on-chip double-folded dipole antenna and an on-board optical lens are utilized to demonstrate a wireless link achieving 20- and 25-Gb/s data rates at bit error rates (BERs) of  $6.3 \times 10^{-6}$  and  $2.2 \times 10^{-4}$ , respectively, across a distance of 15 cm. The transmitter and receiver consume 375 and 575 mW, respectively, which correspond to power efficiencies of 15 pJ/bit for the transmitter and 23 pJ/bit for the receiver. They occupy a silicon area of 4.3 and 4.5 mm<sup>2</sup>, respectively.

**Index Terms**—Broadband circuits, broadband communication, ultra wideband communication.

## I. INTRODUCTION

THE wide and available bandwidths above 200 GHz open a lot of opportunities for very high data rate communication solutions. Such frequency range might be optimal for applications that require very high data rates for short ranges such as chip to chip, board to board or rack to rack communication in data centers. At these frequencies, the wavelength is in the millimeter range. Hence, on-chip antenna is one of the efficient solutions to deliver the power out of the chip, alleviating the need for expensive off-chip

alternatives and packaging techniques. With the continuous enhancement of  $f_T/f_{\max}$ , silicon-based technologies are proven as candidates to realize fully integrated transceiver solutions, reducing the effort, cost, and time to market required for on board solutions, especially at such extremely high frequencies. Technological options such as local back side etching (LBE) offer also potential solution for enhancing the on-chip antenna gain and the system efficiency. While implementing systems at sub-terahertz frequencies, different challenges rise on the system and circuit levels. The degraded maximum available gain (MAG) at such frequencies results in low-power efficiency transmitters and frequency generation circuits. On top of that, the relatively high minimum noise figure (NF) ( $NF_{\min}$ ) allows only for receivers with limited sensitivity. These factors, together with the high path loss, result in a very challenging link budget analysis. In order to overcome these challenges, circuits and system techniques need to be implemented to enable efficient solutions.

To achieve high system dynamic range, receiver NF is to be minimized while maximizing the transmitter output power and maximizing the receiver gain to cover such dynamic range. This can be reached by cascading more stages at the RF side [low noise amplifiers (LNA)+Mixer], which limits the achievable bandwidth, or by implementing high gain baseband chains, which is challenging in direct conversion receivers because of the dc coupling of the different stages. In some embodiments, this has been solved by decoupling the stages with bulky series capacitors. Although being a simple solution, it adds a tradeoff between the area consumption and the achievable low-cutoff frequency of the receiver.

Several transmitter and receiver architectures and building blocks at such high frequencies have been presented in the literature and some presented data transmission experiments, implementing either non-coherent detection for ON-OFF keying (OOK) modulation scheme [1], [2] or coherent detection for phase-shift keying (PSK) and quadrature-amplitude modulation (QAM) schemes [3]–[8].

In this paper, a fully integrated receiver and transmitter chip-set with on-chip antennas are presented, implementing circuits and system techniques to maximize RF bandwidth, system dynamic range, and power efficiency. Fig. 1 shows the block diagrams of the direct conversion transmitter and receiver chips, supporting BPSK modulation scheme. DC-offset cancellation loops (dc OCLs) are used within the receiver to guarantee consistent performance across process variations and achieve low-cutoff frequency. The complete system is characterized by wireless data transmission. The paper is organized

Manuscript received February 20, 2018; revised April 30, 2018; accepted May 13, 2018. Date of publication June 6, 2018; date of current version August 27, 2018. This paper was approved by Associate Editor Hossein Hashemi. This work was supported by the European project WORTECS under Grant 761329. (Corresponding author: Mohamed Hussein Eissa.)

M. H. Eissa, A. Malignaggi, K. Schmalz, and D. Kissinger are with the Circuit Design Department, Leibniz-Institut für innovative Mikroelektronik, 15236 Frankfurt (Oder), Germany (e-mail: eissa@ihp-microelectronics.com).

R. Wang and M. Elkhoully were with the Circuit Design Department, Leibniz-Institut für innovative Mikroelektronik, 15236 Frankfurt (Oder), Germany.

A. C. Ulusoy is with the Electrical and Computer Engineering Department, Michigan State University College of Engineering, East Lansing, MI 48824 USA.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2018.2839037

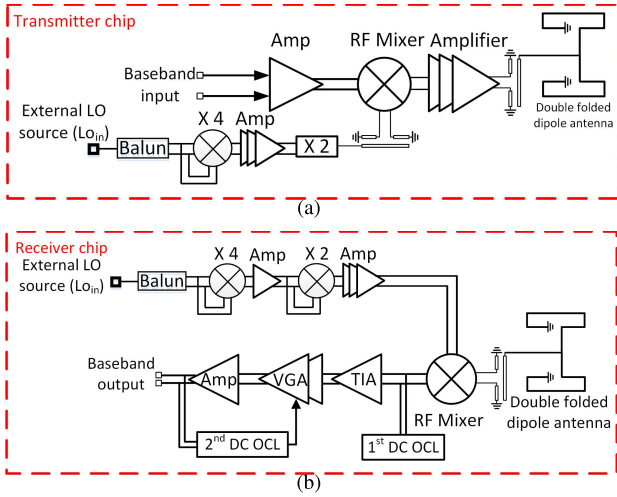


Fig. 1. (a) Transmitter and (b) receiver block diagrams.

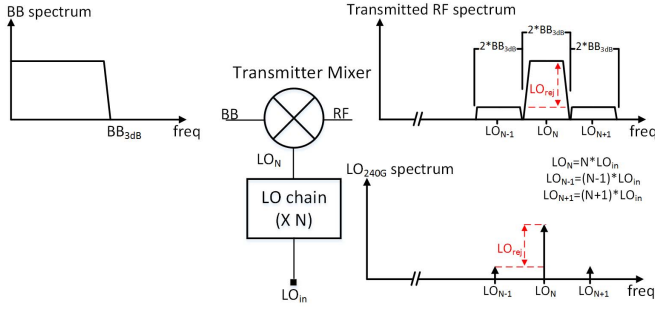


Fig. 2. Transmitted spectrum in relation with LO frequency and spurious rejections.

as follows: the system aspects considered for choosing the local oscillator (LO) frequency are presented in Section II. The transmitter and receiver design details and measurements are discussed in Section III and Section IV, respectively. Section V provides a summary of the antenna design. The measurement results of the wireless link demonstrator are then presented in Section VI and Section VII concludes the paper.

## II. LO FREQUENCY GENERATION

A frequency multiplying chain is utilized to generate the on-chip sub-terahertz carrier frequency  $LO_N$ , centered at 240 GHz. Although low-frequency signals are easier to generate and route on board with low losses. The choice of the input frequency  $LO_{in}$  and the multiplication factor  $N$  is crucial in communication systems, as it defines the frequency spacing between the desired signal and any other spurious signal. To visualize the effect of the LO spurs and the spacing between them on the system specifications, Fig. 2 shows how the spurious tones of the LO signal,  $LO_{N-1}$  and  $LO_{N+1}$ , attenuated by a ratio of  $LO_{rej}$  from the fundamental signal  $LO_N$ , create undesired spurious versions of the data. Hence,  $LO_{in}$  should be at least equal to twice the targeted baseband bandwidth to guarantee minimum interference on top of the desired signal from parasitic up and down conversions. This will guarantee that this parasitic harmonics will not degrade

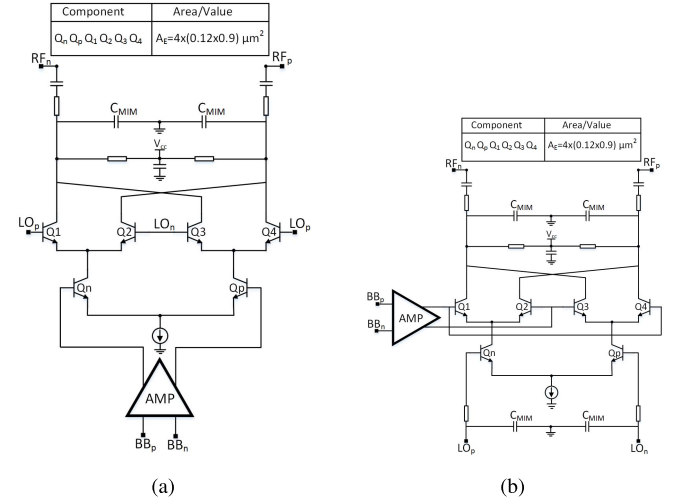


Fig. 3. Schematic of (a) conventional upconversion Gilbert cell mixer and (b) proposed mixer.

the signal quality. It is worth mentioning that lower  $LO_{in}$  is still possibly utilized, but in cost of more stringent requirements on the spurious harmonics rejection. For the system presented here, a baseband signal bandwidth of 15 GHz is targeted, so an LO frequency of 30 GHz is multiplied by eight through a multiplication chain.

In the transmitter chip, as shown in Fig. 1(a), a single-ended 30-GHz input LO signal is converted to a differential one through an edge-coupled spiral Marchand balun. The balun drives a Gilbert cell-based quadrupler, optimized to maximize the fourth harmonic at its output. The resulting 120-GHz signal is then amplified by a three-stage cascode amplifier, which acts also as a filtering stage to cancel out the unwanted harmonics. The signal is then multiplied by two through a push-push frequency doubler. As the output of such frequency doubler is single ended, a 240-GHz Marchand balun is utilized to feed the mixer's LO port differentially [9], [10]. In the receiver chip, the doubler was implemented differentially using a Gilbert cell-based frequency doubler, as shown in Fig. 1(b), followed by a broadband amplifier to drive the mixer. The LO multiplication chain is presented in detail in [11].

## III. WIDEBAND 240-GHz TRANSMITTER

The transmitter chip is shown in Fig. 1(a). The baseband signal is amplified by a resistively loaded common emitter amplifier. The differential input is resistively matched through a 100-Ω resistor. The baseband signal is then upconverted through a fundamental mixer. The broadband amplifier presented in [11] is used as power amplifier following the mixer to increase the output power radiated through a double-folded dipole on-chip antenna.

In conventional Gilbert cell mixers, as shown in Fig. 3(a), the LO signal drives the switching quad transistors ( $Q_1$ – $Q_4$ ), while the baseband signal is fed into the transconductance ( $g_m$ ) stage ( $Q_n$ – $Q_p$ ). In this paper, as shown in Fig. 3(b), this configuration was modified in order to maximize the mixer conversion gain and bandwidth [12]. Because of the limited

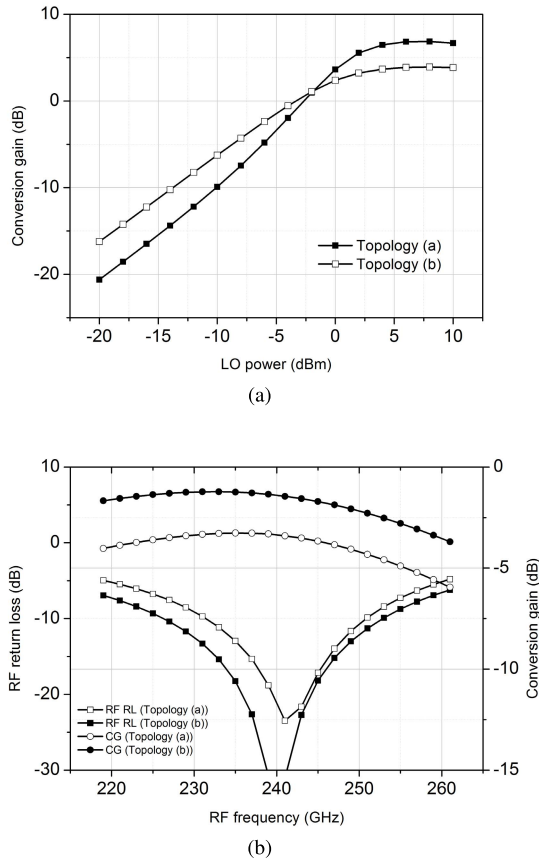


Fig. 4. Comparison between mixer topologies. (a) In terms of conversion gain across LO power, conversion gain and (b) RF return loss with LO = 240 GHz, LO power = -5 dBm, and  $P_{in} = -10$  dBm.

power at 240 GHz, the LO signal was fed into the  $g_m$  stage instead of the switching quad. As now the LO driver is loaded by half the number of transistors, the input impedance in this case is typically doubled compared to the conventional connection. This allows for lower loss matching networks and higher voltage swing at the LO port and so better switching. To validate this analysis, both topologies have been simulated in the same matching conditions. Transistors are equally sized in order to keep all of them in the optimum  $f_T$  biasing conditions. Simulation results showed the input impedance at the LO port for topology (a) is  $8.6-j*12$  while that for topology (b) is  $18-j*15$ . As shown in Fig. 4(a), the conversion gain of the modified topology [topology (b)] is higher than the conventional topology [topology (a)] till a certain level of LO power after which the LO power is high enough to perform better switching. Moreover, because of the higher input impedance in topology (b), the impedance matching ratio is lower, which leads to less lossy matching networks. Another advantage of topology (b) is the higher RF output impedance, being nearer to the 100- $\Omega$  differential impedance, which promises for wider RF bandwidth.

The conversion gain and RF return loss of both mixer topologies are simulated for LO power of -5 dBm; this LO power level was chosen to account for future in-phase and quadrature-phase mixer implementation, where the LO signal will be equally divided and experiences the losses of the

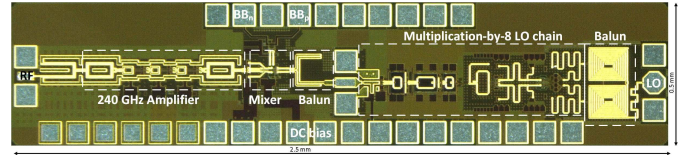


Fig. 5. Transmitter die photo for on-wafer characterization.

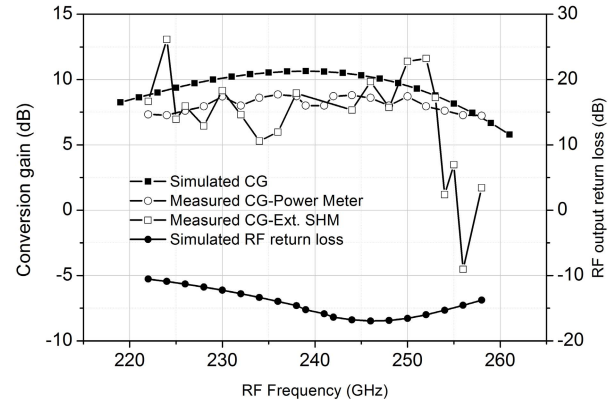


Fig. 6. Transmitter conversion gain across RF frequency (LO = 240 GHz).

90° passive hybrid. It is clear from Fig. 4(b) that the proposed LO-baseband configuration offers higher conversion gain and wider RF bandwidth under the same LO and baseband conditions.

#### A. Transmitter Performance

To evaluate the performance of the transmitter, a breakout circuit was manufactured without the on-chip antenna. The breakout circuit, shown in Fig. 5, was measured on wafer. The 30-GHz LO signal is provided in a single-ended fashion through an external source, while the baseband signal is provided differentially through an external hybrid broadband balun. The high frequency output is then probed using a WR3.4 waveguide probe with insertion loss of 3 dB. At first, an external waveguide subharmonic mixer (SHM), connected to a spectrum analyzer was utilized to inspect both the spectrum of the upper sideband (USB) and lower sideband (LSB) independently, and the LO-to-RF leakage. In Fig. 6, the baseband frequency was swept at a constant LO frequency of 240 GHz and low input power to guarantee linear operation. The measured results shows RF 3-dB bandwidth of more than 35 GHz. The ripple in the conversion gain is expected to be a result of inaccurate external SHM calibration table. In order to measure the LO-to-RF rejection, the LO frequency was swept at a constant baseband input frequency of 1 GHz. As shown in Fig. 7, the leakage is less than -23 dBc across the 3-dB bandwidth.

In order to measure the output power and the conversion gain more accurately and omit the inaccuracies in the external SHM losses calibration table, a PM4 calorimeter-based power detector was used to measure the output power directly at 240 GHz. In such setup, there is no way to differentiate between USB and LSB so they are assumed to be equal. First,



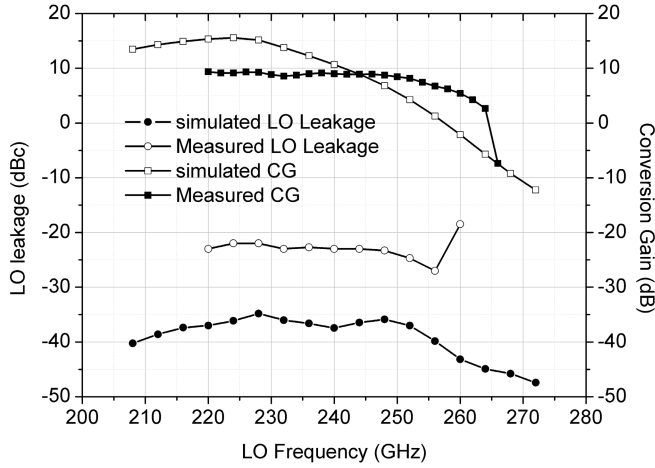


Fig. 7. Transmitter conversion gain and LO-to-RF leakage across LO frequency (RF = 241 GHz).

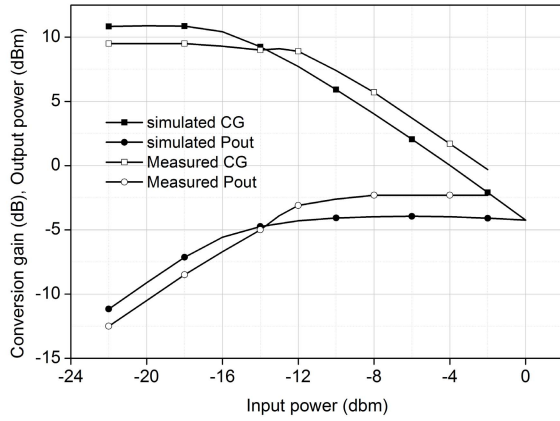


Fig. 8. Transmitter conversion gain and output power across input power.

the baseband frequency is swept. With respect to the SHM based measurement, the conversion gain in linear operation, plotted in Fig. 6, shows better agreement with its simulated values. Then, the baseband input power was swept. As shown in Fig. 8, a  $-2.3$ -dBm saturated output power along with an output 1-dB compression point (OP1dB) of  $-3$  dBm and a conversion gain of 9 dB were measured. Considering the output pad losses of 1.5 dB, the saturated output power in the transmitter version with on-chip antenna is expected to be  $-0.8$  dBm. The transmitter consumes a total power of 375 mW.

#### IV. WIDEBAND 240-GHz RECEIVER

As the operation frequency increases approaching the transistor  $f_T$  frequency, the transistor  $NF_{min}$  increases significantly, while the MAG decreases. In Fig. 9,  $NF_{min}$ , MAG, and stability factor of a single-stage cascode amplifier, widely adopted configuration for amplifier designs at such frequency ranges [13], with transistor-emitter area of  $4 \times 0.12 \times 0.9 \mu m^2$  are plotted across the transistor collector bias current. In the schematic level, a MAG of 15 dB and an  $NF_{min}$  of 10 dB were simulated in stable conditions. Obviously, the MAG and the

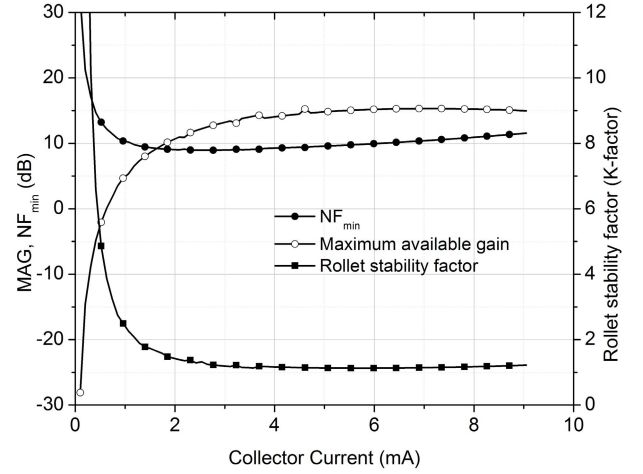


Fig. 9. MAG and minimum NF of a single-stage HBT cascode amplifier.

$NF_{min}$  performances will be even worse after electromagnetic simulations of amplifier core and matching networks.

To elaborate more on the frequency dependence of the NF, the expression of the HBT's shot noise is reported in (1) and (2) [14], where  $q$  is the charge,  $B$  the bandwidth of interest,  $V_T$  thermal voltage,  $I_C$  the transistor bias current,  $Z_S$  the source impedance, and  $\beta(\omega)$  the transistor frequency-dependent current gain. The term  $N_{CE}$  considers the shot noise added by the collector-emitter junction while the term  $N_{BE}$  corresponds to the one injected by the base-emitter junction. The base contact resistance is neglected here

$$V_{in}^2 = 2Bq(N_{BE} + N_{CE}) \quad (1)$$

$$N_{BE} = \frac{V_T^2}{I_C}, \quad N_{CE} = \frac{Z_S^2 I_C}{\beta(\omega)}. \quad (2)$$

It is clear that as the frequency increases, the current gain  $\beta(\omega)$  decreases and so the input referred noise increases. The relatively high NF achievable by LNA at such frequency ranges makes its benefit for the link budget analysis marginal. This motivates the idea of omitting the LNA and go for a mixer-first architecture, if the mixer design can be optimized to achieve NF comparable to the LNA NF. This will also promise for better linearity and larger bandwidth because of reducing the number of cascaded stages in the chain. In this paper, a mixer-first architecture is proposed as shown in Fig. 1(b).

##### A. Downconversion Mixer With first dc Offset Cancellation Loop

In a conventional Gilbert cell mixer design at such sub-millimeter-wave frequencies, the  $g_m$  stage is the first noise contributor followed by the switching quad transistors. At the same time, the  $g_m$  stage acts as an amplification stage prior to the switching quad stage, reducing its noise contribution. Nevertheless, due to the reduced achievable MAG, at this high frequency, this benefit is limited. Hence, it was found, as shown in Fig. 10 and further explained in [10], that by omitting the  $g_m$  stage lower mixer NF can be achieved. While the RF signal is fed directly to the emitters of the switching quad transistors ( $Q_1$ – $Q_4$ ). Another advantage of feeding the RF

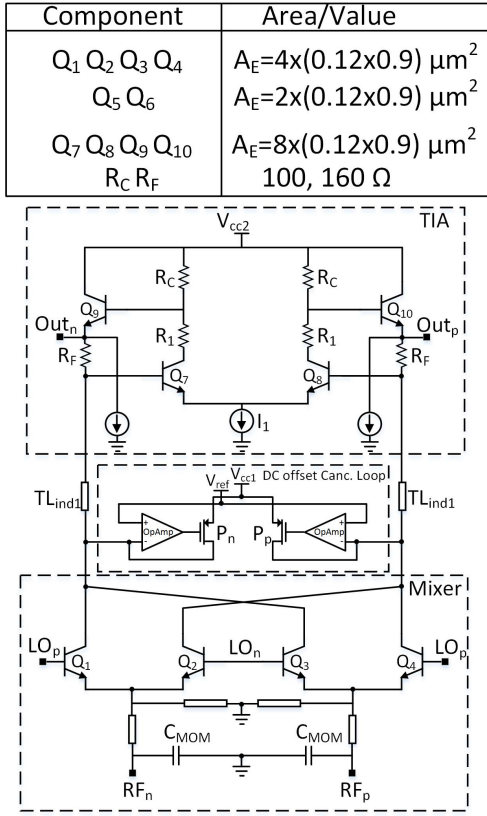


Fig. 10. Schematic of mixer, TIA, and first dc OCL.

signal into the emitters rather than the base is the lower input impedance, being nearer to the 100  $\Omega$  differential impedance, which leads to lower loss matching structures. As the size of ( $Q_1$ – $Q_4$ ) decreases, their capacitive loading decreases, but their base resistance ( $r_{bb}$ ) increases, boosting the Johnson noise contribution of the switching quad transistors. Hence, the quad sizing is driven by a compromise between capacitive loading, driving capability, and noise contribution.

Although omitting the  $g_m$  stage enhances the NF, it limits the conversion gain. Increasing the conversion gain through increasing the load resistance in conventional Gilbert cell mixer compromises the achievable bandwidth. Hence, to further enhance the mixer conversion gain without sacrificing the bandwidth, a transimpedance amplifier (TIA) is implemented at the mixer load to translate the switching quad output current signal into a voltage signal. Normally, the drawback of such implementation is the need for high-voltage headroom and so high supply voltage. In this paper, as shown in Fig. 10, a dc bias servo loop is proposed where a pair of pMOS devices ( $P_n$ – $P_p$ ) is used as dc current source to bias the switching quad. The pMOS devices are controlled by two operational amplifiers (OPAMPs) sensing the switching quad collectors' dc voltage and comparing it to an on-chip reference voltage ( $V_{ref}$ ). This setup ensures that only the ac signal flows across the resistor  $R_F$  and not the dc current, not requiring any higher supply voltage. In such case, the sizing of the  $R_F$  and the TIA parameters are irrelevant to the mixer bias, adding a lot of flexibility to the design and avoiding sub-optimal realizations. The bias servo loop also acts as a dc OCL

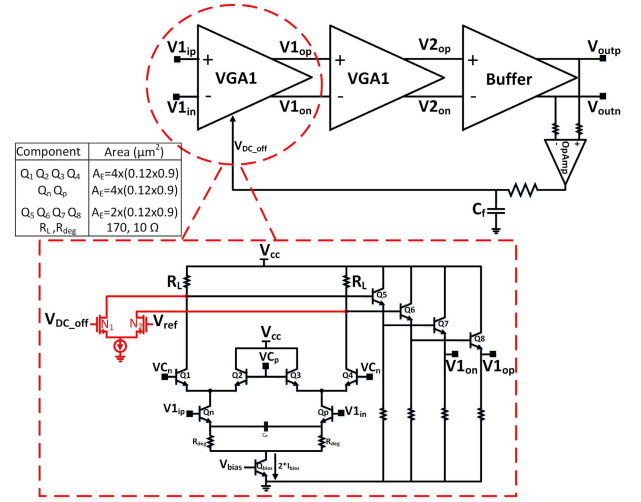


Fig. 11. Schematic of cascaded VGAs and output buffer with second dc OCL.

compensating for any dc offsets arising from the LO leakage of mixer's devices mismatches. In order to further enhance the achieved bandwidth, a slight inductive peaking is implemented between the mixer and the TIA ( $TL_{ind1}$ ) to compensate for the switching quad parasitic capacitance and the TIA input capacitance, taking care of the group delay variations across the targeted bandwidth [15].

### B. Cascaded VGAs With Second DC-Offset Cancellation Loop

To achieve sufficient output swing, for bit error rate (BER) measurements, cascaded variable gain amplifiers (VGA) are used after the mixer. The current steering VGA topology, shown in Fig. 11, was implemented with capacitive peaking at the emitter. An output buffer is utilized to drive the 100- $\Omega$  differential output. The second dc OCL is implemented in a series–shunt feedback topology where the differential output dc voltages ( $V_{outp}$ ,  $V_{outn}$ ) are sensed and compared within a differential-to-single-ended OPAMP. The output of the OPAMP is then compared to an internally generated reference voltage ( $V_{ref}$ ) through a current steering nMOS differential pair ( $N_1$ ,  $N_2$ ) delivering the current difference to the resistive load of the first VGA as shown in Fig. 11. Such a dc OCL is crucial in dc-coupled cascaded amplification stages since it avoids any gain drop across process variations due to the saturation of the different stages.

### C. Receiver Performance

In order to test the performance of the baseband chain including first and second dc OCLs, a test cell, whose die photo is shown in Fig. 12, was manufactured. On-wafer differential S-parameter measurements show a transimpedance gain of 68 dB  $\Omega$  in maximum gain setting across a 3-dB bandwidth of 46 GHz with maximum group delay variation of  $\pm 5$  psec as shown in Fig. 13(a). The baseband chain achieves a low-cutoff frequency 3-dB bandwidth of 8 MHz which can be reduced further by simply adding off-chip capacitors, this does not affect the RF performance unlike the usage of dc

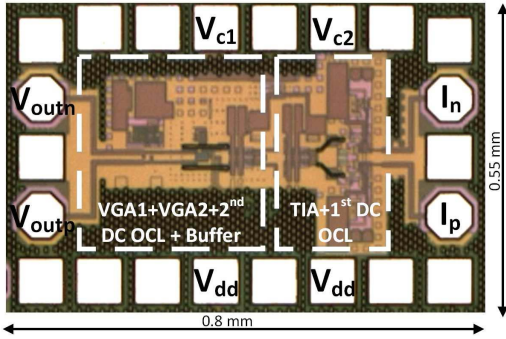


Fig. 12. Baseband chain test structure die photo.

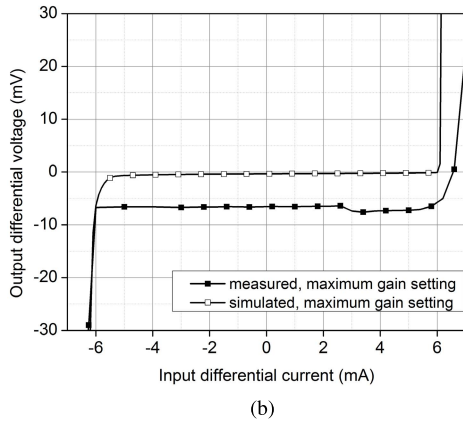
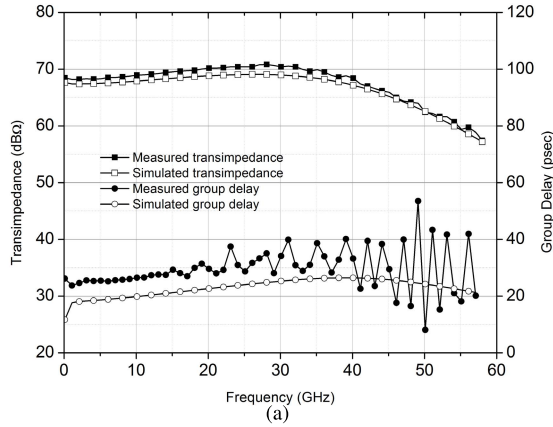


Fig. 13. (a) Baseband chain's transimpedance and group delay across frequency and (b) differential output voltage across differential input current.

blocking capacitors within the signal path. The operation of the two dc OCLs was tested by inserting a differential dc current at the input ( $I_p$ ,  $I_n$ ), to mimic the mismatches generated from the LO leakage or due to devices mismatches, while monitoring the output dc voltage ( $V_{outp}$ ,  $V_{outn}$ ). As shown in Fig. 13(b), the two dc OCLs operate across an input dc current of  $\pm 5.5$  mA with only 6-mV output dc offset voltage in maximum gain. In order to characterize the full receiver including the mixer and the LO multiplication chain, the test structure shown in Fig. 14 was manufactured and measured on wafer. The RF frequency was swept at a constant LO

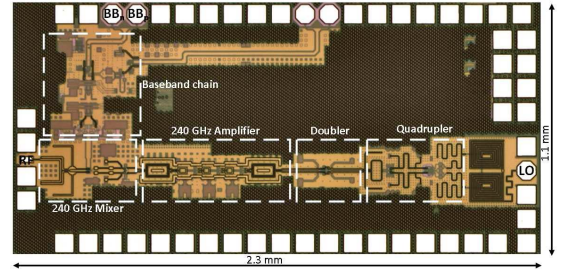


Fig. 14. Integrated receiver die photo for on-wafer characterization.

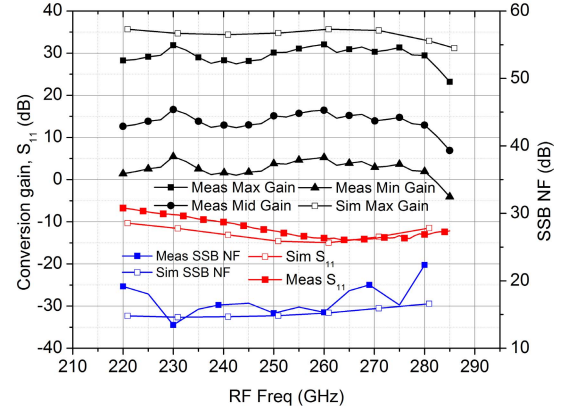


Fig. 15. Receiver conversion gain, input return loss, and SSB NF across RF frequency.

frequency of 240 GHz as shown in Fig. 15. A maximum conversion gain of 32 dB was measured with gain tuning range of 25 dB across a RF 3-dB bandwidth of 55 GHz in linear operation. An input return loss better than  $-7$  dB was measured across the 3-dB bandwidth (without the input pad, the input return loss was simulated to be better than  $-10$  dB). Noise measurements have been conducted using the gain method. The single-sideband (SSB) NF was calculated in maximum gain to be 16.5 dB averaged across the band with a minimum value of 13.4 dB at 230 GHz. The enhanced RF matching, the higher LO power and the higher TIA gain are the reasons why the presented receiver shows lower SSB NF compared to the one presented in [10]. In addition, better results are expected without the input RF pad. As discussed earlier, the LO multiplication chain generates not only the desired LO signal of  $8 \times 30$  GHz = 240 GHz but also undesired seventh and ninth harmonics at 210 and 270 GHz, respectively. In order to quantify the distortion caused by these spurious emissions, the resulting down-converted signals at  $210 - GHz - F_{RF}$  and  $270 - GHz - F_{RF}$  were measured. The rejection for two LO frequencies of 235 and 240 GHz are plotted in Fig. 16, showing a worst case rejection of 30 dBc at RF frequency of 230 GHz.

To characterize the receiver linearity, the RF input power was swept at a constant LO frequency of 240 GHz and RF frequency of 250 GHz ( $IF = 10$  GHz) for three different gain states. The input power sweep, shown in Fig. 17, shows an input 1-dB compression point (IP1dB) of  $-28.5$  dBm for a gain of 30.5 dB in maximum gain setting at 240 GHz.



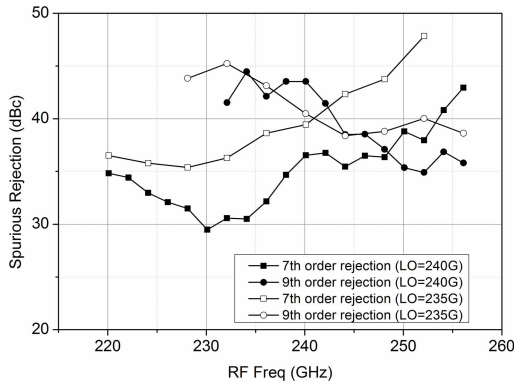


Fig. 16. Receiver spurious rejection to the seventh and ninth LO harmonics.

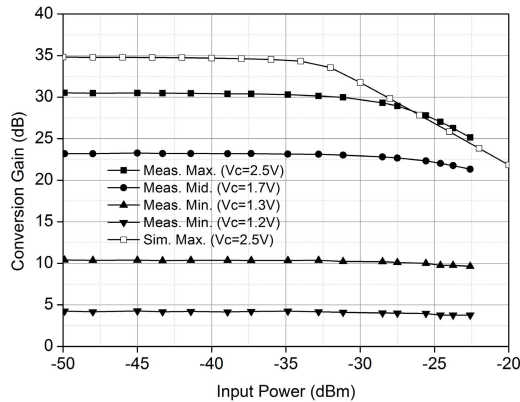


Fig. 17. Receiver conversion gain across input power at different gain states (LO = 240 GHz, IF = 10 GHz).

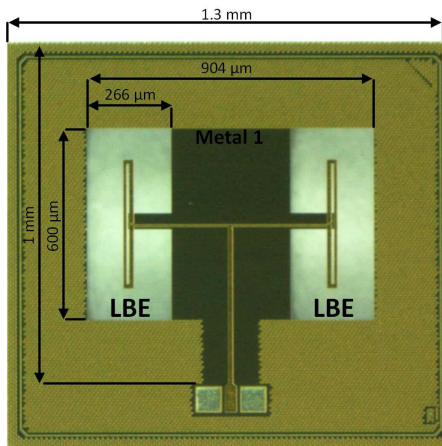


Fig. 18. Antenna test structure die photo.

The close proximity between the measured data and the simulated ones results from the full electromagnetic simulation of the high-frequency components and passives together with the RC extraction of the broadband circuit ones.

## V. BROADBAND ON-CHIP ANTENNA AND LENS

The IHP LBE technology allows for high antenna efficiency by removing the high-loss silicon substrate beneath the antenna radiator. The double-folded dipole antenna presented here and shown in Fig. 18 is an optimized version of the antenna presented in [16] for larger RF bandwidth.

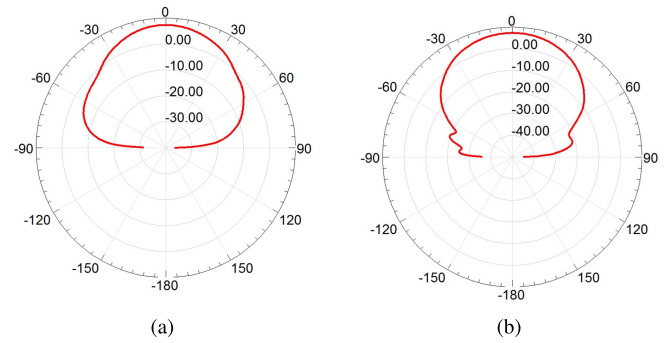


Fig. 19. Antenna simulated radiation pattern at 240 GHz in (a) *E*-plane and (b) *H*-plane.

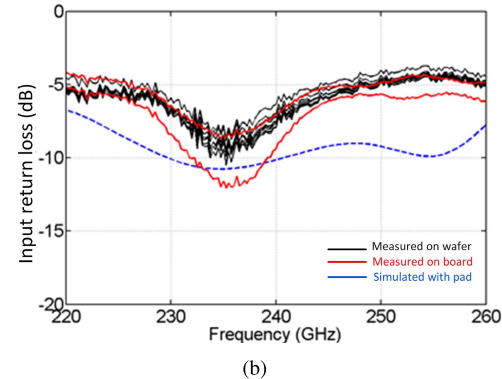
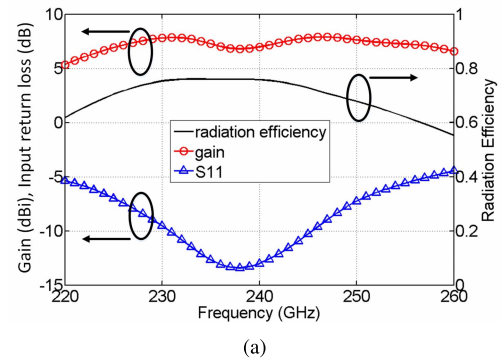


Fig. 20. Antenna simulation results (without pad) and measurement results for (a) two chips on PCB and (b) eight chips on-wafer and simulation results with pad.

The radiator is manufactured on the uppermost metal layer (TM2) with the board below the chip serving as reflector in the final implementation. The silicon substrate height is thinned to 200  $\mu\text{m}$ . The simulated antenna gain is 7.5 dBi with  $\pm 25^\circ$  beamwidth as shown in Fig. 19 and a 1-dB bandwidth of 33 GHz from 225 to 258 GHz as shown in Fig. 20(a), with a maximum simulated efficiency of 70%. These simulation results do not include the input pad structure. The antenna test structure shown in Fig. 18 was measured on wafer, using the metal chuck of the probe station as reflector. Then, the antenna test structure was diced and glued on the ground plane of a printed circuit board (PCB) in order to compare the performance. The measured results of eight antennas measured on wafer and two antennas measured on PCB together with

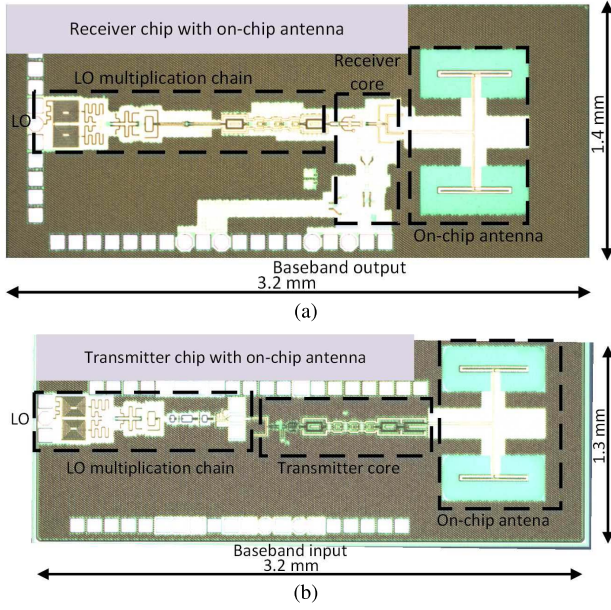


Fig. 21. (a) Transmitter and (b) receiver chips with on-chip antenna.

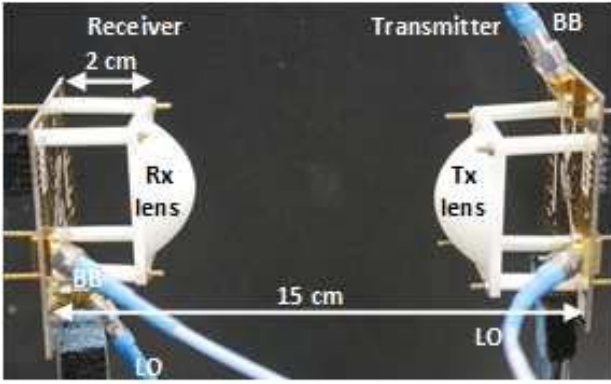


Fig. 22. Wireless link setup.

the simulated input return loss including the pad can be observed in Fig. 20(b). The difference between the simulated and measured data might originate from the tolerance of the LBE process or the thinning process, for the glued version the height of the glue also plays a role, and above at such frequencies the probe tip over travel shows variations in the return losses. To further improve the radiated power, a 40 mm × 40 mm lens made of high-density polyethylene with a relative permittivity of 2.32 is utilized. The lens has a plano-convex type with two refracting surfaces and a focal length of 25 mm. The gain of the lens combined with the effective gain of the on-chip antenna depends on the link distance as presented in [17].

## VI. WIRELESS DATA LINK EXPERIMENTAL RESULTS

Die photos of the transmitter and receiver chips with on-chip antennas are shown in Fig. 21. The chips were thinned to 200  $\mu\text{m}$  based on the optimization of the antenna design with the LBE option. The receiver and transmitter chips have been bonded as a die-on-board with the optical lens fixed at a

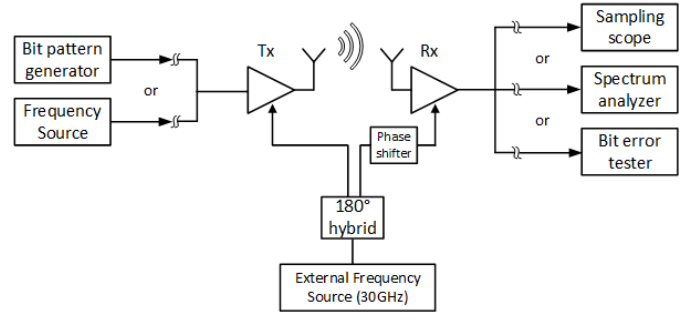


Fig. 23. Measurement setup block diagram.

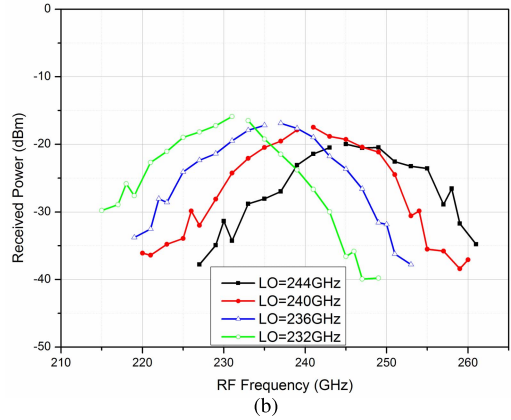
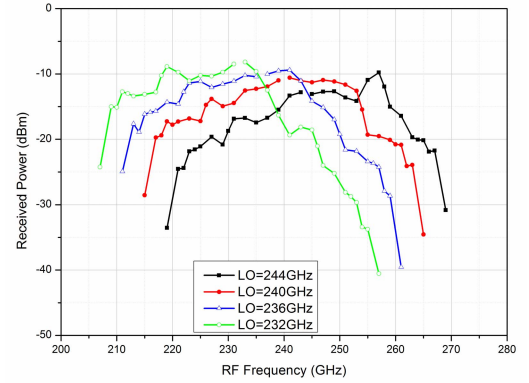


Fig. 24. Received power across RF frequency with transmitter (a) in saturation and (b) in 8-dB back-off.

distance of 2 cm from the PCB surface, as shown in Fig. 22. The radiation occurs from the top side of the chip while the board metallization behaves as reflector. A Rogers3003 material is used on top of an FR4 layer for the board production to route with low losses the LO signal while maintaining robust board handling. The dc connections have been routed at the backside of the PCB to avoid unwanted coupling between the transmitter and the receiver. The measurement setup depicted in Fig. 23 shows that the same frequency source, with a specified phase noise of  $-145\text{dBc/Hz}$  at 10-MHz offset which dominates the noise performance of the 240 GHz frequency source, have been used to drive the LO of both boards to guarantee frequency and phase synchronization as



TABLE I  
PERFORMANCE COMPARISON OF WIRELESS LINKS AT SUB-MILLIMETER-WAVE FREQUENCIES

Parameter	[1]	[4]	[18]	[2]	[3][5]	[7]	This Work
Technology	65 nm CMOS	130 nm SiGe	130 nm SiGe	40 nm CMOS	65 nm CMOS	130 nm SiGe	130 nm SiGe
$f_T / f_{\max}$ (GHz)	—	350/550	350/550	—	—	300/500	300/500
Frequency (GHz)	260	240	240	210	240	190	240
Receiver Integration Level	OOK demod. LO gen. @ 180 GHz	LNA, IQ mixer LO gen.	LNA, IQ mixer LO gen.	LNA power detector	IQ mixer, BB chain LO gen.	LNA, Mixer, VG BB chain, LO driver	Mixer, VG BB chain, LO gen. DC offset canc. loops
Transmitter Integration Level	OOK mod.	BB Amp., IQ mixer LO gen.	BB Amp., IQ mixer LO gen.	OOK mod., PA	IQ mod., tripler PRBS gen.	LO driver, Mixer	BB Amp., Mixer, PA LO gen.
RF Rx 3dB Linear BW (GHz)	15	28	23	—	14	35	55
RF Tx 3dB Linear BW (GHz)	—	40 <sup>1</sup>	35	—	—	60	35
TRX 6-dB Saturated RF BW (GHz)	—	26	30	—	—	40 <sup>Φ</sup>	35
TRX 6-dB Linear RF BW (GHz)	—	—	—	—	—	—	20
Modulation type	OOK	QPSK/BPSK	QPSK/BPSK	OOK	QPSK/BPSK	BPSK	BPSK
Detection type	non-coherent	coherent	coherent	non-coherent	coherent	coherent	coherent
LO architecture	60GHz VCO+x 3	x 16	x 16	VCO+x 3	Injection locked VCO+x 3	not integrated	x 8
EIRP <sup>2</sup> (dBm)	+5	31.86	35	6.8	1	-1	13.2
$R_x$ Gain (dB), IP1dB (dBm)	17, —	11, —	21, —	LNA:20, — PA:20, -15	25, —	27-47, -45	7-32, -28.5 <sup>*</sup>
$T_x$ Gain (dB), IP1dB (dBm)	—, —	—, —	—	—	—, —	-6, -1	10.5 <sup>**</sup> , -12 <sup>**</sup>
$NF_{SSB}$ (dB)	19	15 <sup>+</sup>	9.5	10 <sup>3</sup>	15	10.7	16.5 <sup>++</sup> , 13.4 <sup>+</sup>
$T_x P_{sat}$ (dB)	—	6	8.5	-1.3	0	-6	-0.8 <sup>**</sup>
$R_x$ Area (mm <sup>2</sup> )	3	1.5	1.6	0.8	2	—	4.5
$T_x$ Area (mm <sup>2</sup> )	3	1.6	1.5	1.9	2	—	4.16
Antenna type	Leaky wave	Ring antenna with silicon lens	Ring antenna with silicon lens	Modified dipole	Slotted loop antenna	Monopole	Double folded dipole with plastic lens
Antenna gain (dBi)	4.5	26.5 <sup>2</sup>	26.5 <sup>2</sup>	-0.1	0.72	5	14 <sup>2</sup>
Range (cm)	4	70	100	1	2	0.6	15
Symbol rate (GHz)	10	12.5	35 <sup>Ψ</sup>	10.7	5, 8	50 <sup>Φ</sup>	20, 25
Demonstrated data rate (Gbit/s)	10 OOK	25 QPSK (PRBS9)	35 <sup>Ψ</sup> BPSK (PRBS9) 65 <sup>Ψ</sup> QPSK (PRBS9)	10.7 OOK (PRBS31)	10, 16 QPSK (PRBS15)	50 <sup>Φ</sup> BPSK (PRBS15)	20, 25 BPSK (PRBS31)
Stream length	—	—	—	—	—	—	—
BER @ data rate (Gbit/s)	—	—	—	1x10 <sup>-12</sup> @ 10.7	≤ 10 <sup>-6</sup> @ 10, ≤ 10 <sup>-4</sup> @ 16	3.5x10 <sup>-3</sup> @ 50	6.3x10 <sup>-6</sup> @ 20, 2.2x10 <sup>-4</sup> @ 25
EVM(%)	—	30	30	—	—	—	—
$R_x P_{dc}$ (mW)	485	866	1000	—	260	122 <sup>Δ</sup>	575
$T_x P_{dc}$ (mW)	688	1033	960	—	220	32 <sup>Δ</sup>	375
Total $P_{dc}$ (W)	1.173	1.9	1.96	421	480	0.154 <sup>Δ</sup>	0.95
Transmitter efficiency (pj/bit)	68.8	41	14.7	—	23, 14	0.64 <sup>ΔΦ</sup>	18.75, 15
Receiver efficiency (pj/bit)	48.5	34.6	15.3	—	26, 16	2.44 <sup>ΔΦ</sup>	28.75, 23
Transceiver efficiency (pj/bit)	117.3	75.6	30	39.3	49, 30	3 <sup>ΔΦ</sup>	47.5, 38

<sup>1</sup> In saturated conditions. <sup>2</sup> Including antenna and lens gain. <sup>3</sup> At maximum gain setting. <sup>\*\*</sup> Compensated for output pad.

<sup>+</sup> Minimum single side band noise figure. <sup>++</sup> Average single side band noise figure

<sup>\*</sup> LNA noise figure. <sup>Φ</sup> Probed baseband input and output. <sup>Δ</sup> with no LO generation circuitry. <sup>Ψ</sup> With real time scope post processing including adaptive channel equalizer and amplitude limiting

coherent detection is approached. A broadband hybrid balun is utilized as a power splitter to drive the transmitter and the receiver. An analog phase shifter is also connected in the path of the transmitter LO to further tune the phase shift if needed to approach the maximum signal to noise ratio.

In order to quantify the wireless link bandwidth including all cascaded blocks till the board connector level, single-tone measurements were conducted. The input baseband signal frequency was swept at a constant LO frequency while the output signal was monitored using a spectrum analyzer. This sweep was performed for different LO frequencies to evaluate its effect on the performance. As shown in Fig. 24(a), a 6-dB bandwidth of 35 GHz was measured at LO of 240 GHz when the transmitter is in saturation, while in 8-dB back-off conditions a 20-GHz RF bandwidth was measured, as shown in Fig. 24(b). To test the wireless link capabilities, data transmission was tested using a bit pattern generator to create a broadband BPSK signal at the transmitter input and a sampling scope at the receiver output for analyzing the received data. For BPSK modulation scheme, no back-off power is required and the transmitter operates in saturation. Eye diagrams for different data rates of 8, 16, 20, and 25 Gb/s with a 32-bit long pseudorandom binary sequence (PRBS31) and no post processing are shown in Fig. 25. In order to quantify the link

performance further, a BER tester was connected in place of the sampling scope. The bath tub curves depicted in Fig. 26 show that 20 and 25 Gb/s data rates are achieved with BERs of  $6.3 \times 10^{-6}$  and  $2.2 \times 10^{-4}$ , respectively, which allows to perform forward error correction algorithms. A link range of 15 cm was kept in this experiment because of the setup physical limitations arising from sharing the LO signal. The effective isotropic radiated power (EIRP) was calculated from the on-wafer transmitter saturated output power of -0.8 dBm and the measured combined antenna and optical lens gain of 14 dBi to be 13.2 dBm.

Various communication links have been presented in the literature. Table I summaries the main performance parameters of the mostly related works. The integration level and the packaging level strongly affect the performance parameters. In this paper, the modified mixer architecture and optimized design allows the current paper to achieve the largest receiver bandwidth of 55 GHz with high gain enabling the BER measurements with no external amplifiers or post processing. The presented symbol rate and system bandwidth outperform the previously published work at carrier frequencies above 200 GHz, except of [18] which utilizes signal post-processing, doing adaptive channel equalization and amplitude limiting, and [7] which operates at a carrier frequency of 190 GHz

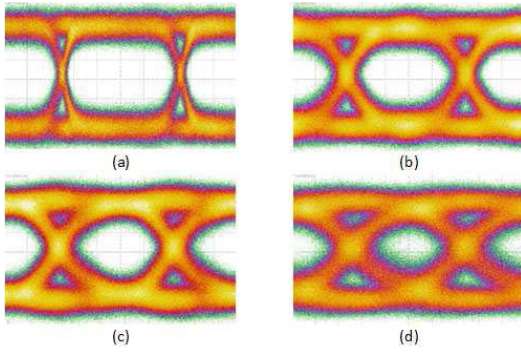


Fig. 25. Eye diagrams for PRBS31 and 50 mV/div at (a) 8 Gbit/s (25 psec/div), (b) 16 Gbit/s (12.5 psec/div), (c) 20 Gbit/s (10 psec/div), and (d) 25 Gbit/s (8 psec/div).

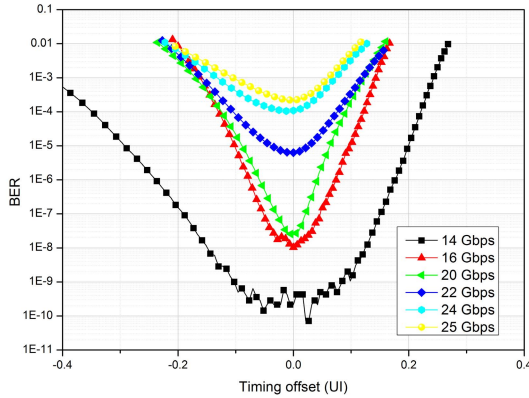


Fig. 26. Measured bath tub curves for different bit rates.

and utilizes on-wafer probing for the baseband input and output signals. Although the presented data rate is the output performed by [18] and [19] which also utilizes waveguide horn antenna, due to the usage of high modulation schemes, the linearity specification of the current paper allows it to utilize also higher modulation schemes by extending it to IQ system without losing of power efficiency. On the other hand, the implementation of the automatic dc OCLs, implemented for the first time for sub-millimeter-wave frequencies transceivers, allows the presented transceiver to be utilized in applications that require low low-cutoff frequency and to use longer PRBS data streams.

## VII. CONCLUSION

In this paper, a fully integrated transmitter and receiver chip-set, supporting BPSK modulation scheme, with on-chip antenna has been presented. Wideband design techniques are used to maximize the system bandwidth. The transmitter and receiver achieve a 3-dB RF bandwidth of 35 and 55 GHz, respectively. The chips have been mounted on-board together with an optical lens in order to demonstrate a wireless transmission. Single tone measurements show that the system achieves a 6-dB RF bandwidth of 35 GHz. Hence, data communication across a 15 cm distance was shown reaching 25 Gb/s with a BER of  $2.2 \times 10^{-4}$ . The transmitter consumes 375 mW and occupies 4.2 mm<sup>2</sup> silicon area. The receiver consumes 575 mW and occupies a silicon area of 4.5 mm<sup>2</sup>. With these specification, the presented chip-set achieves the highest

bandwidth among the state of the art for fully integrated solutions above 200 GHz, demonstrating very high symbol and data rates with no post-processing and long bit streams of 32.

## ACKNOWLEDGMENT

The authors would like to thank the engineers in IHP, J. Schäffner and F. Popiela, for their continuous support in manufacturing the demonstrator boards and bonding the chips.

## REFERENCES

- [1] J.-D. Park, S. Kang, S. V. Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," in *Proc. IEEE Symp. VLSI Circuits Dig.*, Jun. 2012, pp. 48–49.
- [2] S. Moghadami, F. Hajilou, P. Agrawal, and S. Ardan, "A 210 GHz fully-integrated OOK transceiver for short-range wireless chip-to-chip communication in 40 nm CMOS technology," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Sep. 2015, pp. 737–741.
- [3] S. V. Thyagarajan, S. Kang, and A. M. Niknejad, "A 240 GHz fully integrated wideband QPSK receiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2268–2280, Oct. 2015.
- [4] N. Sarmah, P. R. Vazquez, J. Grzyb, W. Ferster, B. Heinemann, and U. R. Pfeiffer, "A wideband fully integrated SiGe chipset for high data rate communication at 240 GHz," in *Proc. 11th Eur. Microw. Integr. Circuits Conf.*, Oct. 2016, pp. 181–184.
- [5] S. Kang, S. V. Thyagarajan, and A. M. Niknejad, "A 240 GHz fully integrated wideband QPSK transmitter in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2256–2267, Oct. 2015.
- [6] N. Sarmah *et al.*, "A fully integrated 240-GHz direct-conversion quadrature transmitter and receiver chipset in SiGe technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 562–574, Feb. 2016.
- [7] D. Fritsche, P. Stärke, C. Carta, and F. Ellinger, "A low-power SiGe BiCMOS 190-GHz transceiver chipset with demonstrated data rates up to 50 Gbit/s using on-chip antennas," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 9, pp. 3312–3323, Sep. 2017.
- [8] J. Eisenbeis, F. Boes, B. Goettel, S. Malz, U. Pfeiffer, and T. Zwick, "30 Gbps wireless data transmission with fully integrated 240 GHz silicon based transmitter," in *Proc. Topical Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, Jan. 2017, pp. 33–36.
- [9] K. Schmalz, J. Borngräber, B. Heinemann, H. Rücker, and J. C. Scheytt, "A 245 GHz transmitter in SiGe technology," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2012, pp. 195–198.
- [10] M. H. Eissa *et al.*, "A 220–275 GHz direct-conversion receiver in 130-nm SiGe:C BiCMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 7, pp. 675–677, Jul. 2017.
- [11] M. H. Eissa *et al.*, "216–256 GHz fully differential frequency multiplier-by-8 chain with 0 dBm output power," in *Proc. Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Oct. 2017, pp. 201–204.
- [12] V. Giannini *et al.*, "A 79 GHz phase-modulated 4 GHz-BW CW radar transmitter in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2925–2937, Dec. 2014.
- [13] D. Fritsche, G. Tretter, P. Stärke, C. Carta, and F. Ellinger, "A low-power SiGe BiCMOS 190-GHz receiver with 47-dB conversion gain and 11-dB noise figure for ultralarge-bandwidth applications," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 10, pp. 4002–4013, Oct. 2017.
- [14] B. Gilbert, "Design considerations for BJT active mixers," in *Low-Power HF Microelectronics: A Unified Approach*. Piscataway, NJ, USA: The Institution of Electrical Engineers, 1996.
- [15] M. H. Eissa *et al.*, "A wideband monolithically integrated photonic receiver in 0.25-μm SiGe:C BiCMOS technology," in *Proc. IEEE Eur. Solid State Circuits Symp.*, Sep. 2016, pp. 487–490.
- [16] K. Schmalz, R. Wang, J. Borngräber, W. Debski, W. Winkler, and C. Meliani, "245 GHz SiGe transmitter with integrated antenna and external PLL," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2013, pp. 1–3.
- [17] K. Schmalz *et al.*, "245 GHz SiGe sensor system for gas spectroscopy," *Int. J. Microw. Wireless Technol.*, vol. 7, no. 3, pp. 271–278, Jun. 2015.
- [18] P. Rodríguez-Vázquez, J. Grzyb, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 65 Gbps QPSK one meter wireless link operating at a 225–255 GHz tunable carrier in a SiGe HBT technology," in *Proc. IEEE Radio Wireless Symp. (RWS)*, Jan. 2018, pp. 146–149.
- [19] K. K. Tokgoz *et al.*, "A 120Gb/s 16QAM CMOS millimeter-wave wireless transceiver," in *ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 168–170.



**Mohamed Hussein Eissa** received the B.Sc. degree in electrical engineering from Ain Shams University, Cairo, Egypt, in 2009, and the M.Sc. degree in electronics and communications from American University in Cairo, New Cairo, Egypt, in 2014.

He was with Silicon Vision LLC, Cairo, Egypt, where he was involved in the design of ASICs for low-power Bluetooth communication standard. From 2011 to 2014, he was with Hittite Microwave, Cairo, working on the design of transceivers for point-to-point communication. Since 2014, he has been

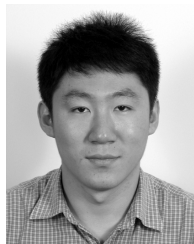
a Research Scientist with the Circuit Design Department, IHP, Frankfurt (Oder), Germany. His current research interests include RF and millimeter-wave circuit designs for communication applications.



**Andrea Malignaggi** received the B.Sc. and M.Sc. degrees in microelectronics from the University of Catania, Catania, Italy, in 2005 and 2008, respectively, the M.A.S. degree in embedded system design from Advanced Learning and Research Institute, Lugano, Switzerland, and the Ph.D. degree from the Berlin Institute of Technology, Berlin, Germany, in 2016, with a focus on the design of CMOS 60-GHz circuits.

Since 2015, he has been with IHP, Frankfurt (Oder), Germany. His current research interests

include the design and optimization of high frequency circuits and systems.



**Ruoyu Wang** received the B.Sc. degree from Tianjin University, Tianjin, China, in 2006, the master's degree in electrical engineering from the Chalmers University of Technology, Gothenburg, Sweden, in 2008, and the Ph.D. degree from the University of Paderborn, Paderborn, Germany, in 2015.

His current research interests include millimeter-wave antenna and packaging designs.



**Mohamed Elkhoully** received the B.Sc. and M.Sc. degrees in electronics and communication engineering from Ain Shams University, Cairo, Egypt, in 2003 and 2008, respectively, and the Ph.D. degree from the Technical University of Dresden, Dresden, Germany, in 2015.

In 2008, he joined the Microwave and Millimeter-Wave Group, IHP, Frankfurt (Oder), Germany, as a Researcher, where he participated in the design of 60- and 240-GHz transceivers. In 2015, he joined Robert Bosch GmbH, Reutlingen, Germany. His

current research interests include, but are not limited to, microwave and millimeter-wave circuits.



**Klaus Schmalz** received the Ph.D. degree in physics from the Humboldt University of Berlin, Berlin, Germany, in 1978.

He is currently with IHP, Frankfurt (Oder), Germany. He has been involved in the field of silicon semiconductor technologies and research and possesses expertise in the area of thermally induced defects and characterization of Si/SiGe structures. From 1998 to 1999, he was with the University of California at Los Angeles (UCLA), Los Angeles, CA, USA, where he was involved in RF circuit

design. He has authored or co-authored over 100 papers. His current research interests include the design of SiGe BiCMOS analog circuits for communication with emphasis on RF frontends for different standards and millimeter-wave circuits for sensor applications.



**Ahmet Cagri Ulusoy** received the B.Sc. degree from Istanbul Technical University, Istanbul, Turkey, in 2005, and the M.Sc. and Ph.D. (*summa cum laude*) degrees from Ulm University, Ulm, Germany, in 2008 and 2012, respectively.

From 2012 to 2015, he was a Research Engineer with the Georgia Institute of Technology, Atlanta, GA, USA. From 2015 to 2016, he was a Group Manager with IHP, Frankfurt (Oder), Germany. In 2016, he joined the Michigan State University, East Lansing, MI, USA, as an Assistant Professor. He has

authored and co-authored more than 90 publications in the field of broadband and millimeter-wave ICs for sensing and communication systems.

Dr. Ulusoy was a recipient of the Best Student Paper Award in the Radio Wireless Symposium in 2011 and the second place in the Best Student Paper Competition at the International Microwave Symposium in 2011. His dissertation was distinguished with the Suedwestmetall Young Scientist Award. He was an Associate Editor with IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS (MWCL).



**Dietmar Kissinger** (S'08–M'11–SM'14) received the Dipl.-Ing., Dr.-Ing. and habilitation degrees in electrical engineering from FAU Erlangen–Nürnberg, Erlangen Germany, in 2007, 2011, and 2014, respectively.

From 2007 to 2010, he was a System and Application Engineer with the Automotive Radar Group, Danube Integrated Circuit Engineering, Linz, Austria. From 2010 to 2014, he was a Lecturer and the Head of the Radio Frequency Integrated Sensors Group with the Institute for Electronics Engineering,

Erlangen, Germany. Since 2015, he has been a Full Professor with the Technische Universität Berlin, Berlin, Germany, and the Head of the Circuit Design Department with IHP, Frankfurt (Oder), Germany. He has authored and co-authored over 250 technical papers and holds several patents. His current research interests include silicon high frequency and high speed as well as low-power integrated systems for communication and automotive, industrial, security, and biomedical sensing applications.

Dr. Kissinger is a member of the European Microwave Association (EuMA) and the German Information Technology Society (ITG) and Society of Microelectronics, Microsystems, and Precision Engineering (VDE/VDI GMM). He currently serves as a member of the technical program committee of the European Solid-State Circuits Conference (ESSCIRC), a member of the technical program committee of the IEEE MTT-S International Microwave Symposium (IMS), and the Chair of the Executive Committee of the IEEE Radio and Wireless Week (RWW). He was a two-time Chair of the IEEE Topical Conference on Wireless Sensors and Sensor Networks (WiSNet) and a two-time Chair of the IEEE Topical Conference on Biomedical Wireless Technologies, Networks and Sensing Systems (BioWireless). He further served as a member of the 2013 and 2017 European Microwave Week (EuMW) Organizing Committee and a member of the 2018 IEEE MTT-S IMS Steering Committee. He was the Chair of the IEEE MTT-S Technical Committee on Microwave and Millimeter-Wave Integrated Circuits (MTT-6) and is currently an elected member of the IEEE MTT-S Administrative Committee. He was a recipient of the 2017 IEEE MTT-S Outstanding Young Engineer Award, the 2017 VDE/VDI GMM-Prize, and was a co-recipient of eight Best Paper Awards. He was a nine-time Guest Editor of IEEE MICROWAVE MAGAZINE and served as an Associate Editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.