Abhinav Vishwakarma*, Markus Fritscher, Amelie Hagelauer and Marc Reichenbach

An RRAM-based building block for reprogrammable non-uniform sampling ADCs

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Abstract: RRAM devices have recently seen wide-spread adoption into applications such as neural networks and storage elements since their inherent non-volatility and multi-bit-capability renders them a possible candidate for mitigating the von-Neumann bottleneck. Researchers often face difficulties when developing edge devices, since dealing with sensors detecting parameters such as humidity or temperature often requires large and power-consuming ADCs. We propose a possible mitigation, namely using a RRAM device in combination with a comparator circuit to form a basic block for threshold detection. This can be expanded towards programmable non-uniform sampling ADCs, significantly reducing both area and power consumption since significantly smaller bit-resolutions are required. We demonstrate how a comparator circuit designed in 130 nm technology can be reprogrammed by programming the incorporated RRAM device. Our proposed building block consumes 83 µW.

Keywords: ADC; CMOS circuit; comparator; memristor; non-uniform sampling; sensors.

ACM CCS: RRAM Device → ADC Sensor Evaluation → Comparator Circuit → Memristor → Hardware Evaluation → System Level.

***Corresponding author: Abhinav Vishwakarma**, Brandenburgische Technische Universität, Cottbus–Senftenberg, Computer Engineering Institute, Konrad-Wachsmann-Allee 5, 03046 Cottbus, Germany, E-mail: abhinav.vishwakarma@b-tu.de
Markus Fritscher, Brandenburgische Technische Universität, Cottbus–Senftenberg, Computer Engineering Institute, Konrad-Wachsmann-Allee 5, 03046 Cottbus, Germany; and IHP – Leibniz Institute for High Performance Microelectronics, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany, E-mail: fritscher@ihp-microelectronics.com
Amelie Hagelauer, Chair of Micro- and Nanosystems Technology, Technische Universität München, Munich, Germany; and Fraunhofer EMFT Fraunhofer Institute for Electronic Microsystems and Solid State Technologies, Munich, Germany, E-mail: amelie.hagelauer@tum.de
Marc Reichenbach, Brandenburgische Technische Universität, Cottbus–Senftenberg, Computer Engineering Institute, Konrad-Wachsmann-Allee 5, 03046 Cottbus, Germany, E-mail: marc.reichenbach@b-tu.de

1 Introduction

The memristor was introduced by Leon Chua in 1971, serving as the "missing circuit element", forming the connection between the electric charge q and the magnetic flux ϕ [1, 2]. The characteristics, among others, yield a programmable resistor, allowing to store information within these devices in a non-volatile manner. In recent years researchers have been able to demonstrate implementations of these circuit elements [3, 4]. Strukov et al. have been able to relate their implementation to the underlying memristive theory in 2008 [5]. Their implementation consists of a stack of titanium dioxide thin film (TiO_2) bounded by two platinum (Pt) electrodes. The flow of electrons in that material controls the random movement of these ions in this thin film, allowing for a change of state in the device's molecular structure. The core layer works as an insulator, whereas the top film layer conducts due to the additional oxygen vacancies in the TiO_2 material. The resistance or state changes when the oxygen vacancies move toward the base layer; As a result, the top layer maintains a steady state [6, 7]. Since the resistance of Titanium dioxide (TiO_2) can be modified it has been adopted as a component of oxygen sensors after being modified with oxygen atoms [8].

In the last years this novel device element has seen widespread adoption due to its prospective high densities and non-volatility. Recently researchers have created multiple promising circuits from these cells, including neural networks [9], memory cells [10], and radiation sensors [11].

Researchers have devised different sensors to detect physical parameters such as temperature, moisture or audio. Humidity sensors use complex mechanisms to detect the current level of moisture present within an environment [12]. Since these sensors yield an electrical parameter such as voltage or frequency, a system can use this threshold to e.g. open or close windows at a given humidity. Unfortunately, this threshold needs to be fine-tuned for a given environment and might change over a system's lifetime. A typical approach lies within using an 8-bit (or more) ADC and programming this threshold into an EEPROM. However, this yields significant implementation overhead.

We propose the approach depicted in Figure 1. We propose to utilize the programmability of the RRAM devices to

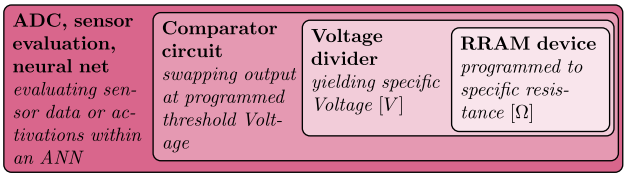

Figure 1: Proposed concept: using a RRAM device to set the threshold of a comparator allows for the easy (re)programming of a sensor evaluation circuit.

precisely set the threshold of a comparator circuit. Instead of sampling at high resolution and reading the threshold from an EEPROM we propose to use a small low-resolution non-uniform sampling ADC block consisting of one or multiple comparators. This allows to remove the high-resolution ADC from the design while maintaining the programmability.

This concept can serve as the building block for a non-uniform sampling ADC if a higher quantization resolution is desired for a given application. The reprogrammability of the devices allows to adapt to sensor degradation or environmental changes during a sensor's lifetime. While the concept of using a RRAM cell within a programmable comparator has been proposed by others [13] these implementations are merely proposed as a concept, lacking both an application and an implementation using an existing and specified CMOS-Process. Within this paper we present an example implementation, consisting of a reprogrammable ADC using an optimized comparator designed using IHP[1] 130 nm SG13S technology, which allows for the integration of RRAM technology into CMOS designs.

The remaining paper is organized as follows: We provide an introduction into relevant topics and related work in Section 2. Section 3 provides an introduction into the implemented methodology. We evaluate the achieved results in Section 4 and conclude the paper in Section 5.

2 Background and related work

2.1 Memristor modelling

A memristor's characteristic hysteresis curve is depicted in Figure 2 [14, 15]. This curve can be generated by applying a DC signal including the devices V_{set} and V_{reset} thresholds.

An early device model has been provided by Biolek et al. [16], which is mathematically similar to [5]. The model

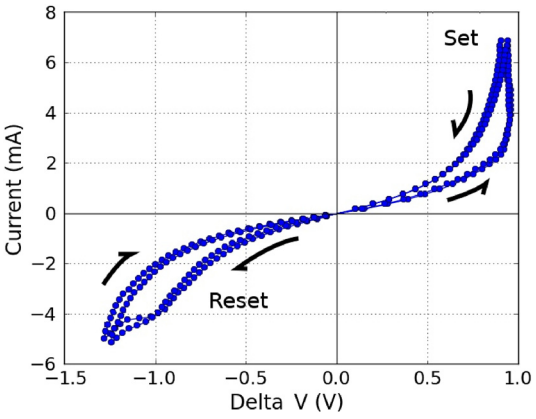

Figure 2: Memristor's I–V cycles hysteresis loop [14].

was rather simplistic, accepting only one state variable. It has been constructed as follows: The oxygen atoms doping method in TiO_2 thin films provides two zones with differing resistances in series with the film [16]. The doped zone ($TiO_2 - x$) has lower resistance and better conductivity, while the region which is not doped has higher resistance with lower conductivity. When the bias voltage is removed, the oxygen vacancies do not shift, and the region between doped and un-doped areas of the memristor's boundary remains in place [8, 17]. This is displayed by a component consisting of two resistors arranged in series (R_{ON}, R_{OFF} where, $R_{ON} < R_{OFF}$). w represents the state variable describing each resistor's relative doped or undoped part (see Figure 3). Doped areas have an oxygen deficit ($TiO_2 - x$) and serve as R_{ON}, whereas undoped areas act as R_{OFF} [8].

In the following years more sophisticated models have been developed. Ding et al. provided an HSPICE Macro design for the resistive random access memory with CuxO technology (ReRAM) [18]. Pickett et al. released a more sophisticated model for the TiOx device which included nonlinear dynamics [19]. This has subsequently been implemented in SPICE [20]. Menzel et al. adapted this model to describe the electrochemical metallization memory cells

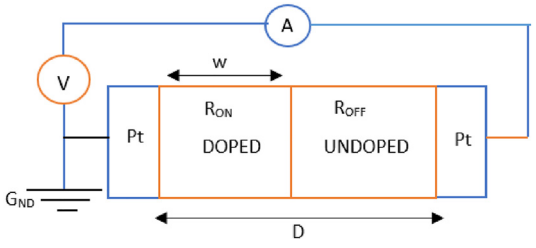

Figure 3: Memristor model based on linear ion drift titanium dioxide (HP's) [8].

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[21]. Gao et al. have found that the observed switching behaviors of metal–oxide based RRAM can be employed to quantitatively investigate and expect the resistive switching aspects [22]. Jiang et al. have proposed the Stanford PKU model [23], which has been adapted to reflect the RRAM devices fabricated at IHP by Reuben et al. [24]. Subsequently, we chose to use it for our investigation

2.2 Non-uniform sampling

Henry Landau invented nonuniform sampling in 1967. This aspect of the theory of sampling deals with the Nyquist-Shannon sampling theorem's results [25]. The Shannon sampling theory for nonuniform sampling states that when an average sampling rate meets the Nyquist condition, a band-constrained signal can be rebuilt from such samples. Several hardware implementations based on this theory have been realized and the mathematical theory of nonuniform sampling thoroughly researched and recognized [26]. Later non-uniform sampling has also been used to describe non-equally distributed quantization thresholds as depicted in Figure 1. Within this paper, we will propose an efficient implementation using RRAM devices. Table 1 shows typical values obtained through nonuniform sampling. The corresponding signals obtained from the ADC interface are quantized. A range that generates the same digital signals exists among the analog input signals.

Table 1: Regular (left) and non-uniform sampling (right) input voltages lead to ADC outputs as specified.

Analog input (V)	Digitized output	Non-uniform ADC input (V)
0	**00**	0
0.25	**01**	0.1
0.5	**10**	0.15
1	**11**	1

Only digitized output has been bolded

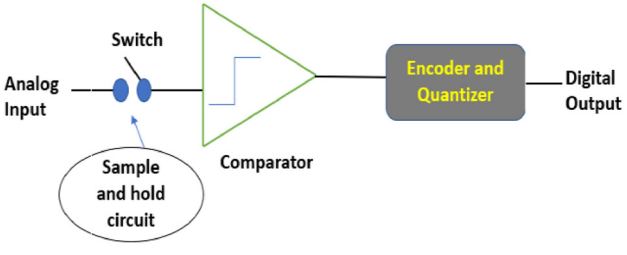


Figure 4: Operation principle of an ADC [28].

2.3 ADC design

Analog signals are converted into digital signals by using Analog-to-Digital Converters (ADCs) for digital signal processors in electronic devices [27]. The ADCs working principle is shown in Figure 4. The Analog signal is first sampled via a circuit (sample and hold) and changed into a discrete-time signal. The sample and hold circuit output is then quantized yielding an approximate quantization level [27, 28]. The quantization level is then encoded into a binary number. The encoded binary number becomes the output of the ADC. The rudimentary operation of the comparator lies within comparing two analog signals and outputting a 0 or 1, depending on whether input a is above or below input b. In recent times, dynamic comparators have found widespread use in reducing energy consumption and increasing the analog-to-digital signal conversion rate [29]. There are inverters in dynamic comparators that are effective at producing positive feedback. Such mechanisms can transform smaller voltage differences into more significant digital output levels. A schematic of the comparator is part of Figure 5. V_{IP} is the voltage supplied at the positive terminal of the input of the comparator, and V_{IN} is the negative voltage to the negative terminal [29, 30]. Suppose V_{IP}, is higher than V_{IN} in that case, the comparator outputs a binary value of 1 and 0 and vice versa.

The gain of a comparator can be written as [31]:

$$\text{Gain} = A_v = \lim_{\Delta \to 0} \frac{V_{\mathrm{OH}} - V_{\mathrm{OL}}}{\Delta V} \tag{1}$$

where ΔV is the input voltage change $V_{\mathrm{IP}} - V_{\mathrm{IN}}$. V_{OH} and V_{OL} are defined as the high and low-level output voltage of the comparator.

The comparator's propagation delay can be expressed as follows (t_{rp} and t_{fp}, respectively, represent the rising and falling propagation delays) [31]:

$$\Delta t = \frac{t_{\mathrm{rp}} + t_{\mathrm{fp}}}{2} \tag{2}$$

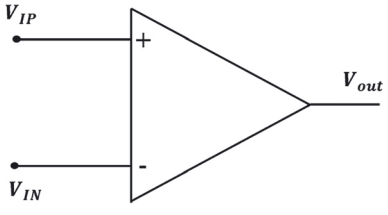


Figure 5: Schematic symbol of a comparator [30].

There are different types of comparators, namely, static, static latched, dynamic, and double-tail dynamic comparators. Within this work we will focus on the static and dynamic comparators.

2.3.1 Static comparators

A static comparator is a basic device that compares two signals (V_{IP} and V_{IN}) based on input and reference signal threshold detection. Two differential input transistors (Nla and N1b), a current mirror load (N2a and N2b), and a current source (I_{SS}) make up the traditional static comparator as depicted in Figure 6a. The input signals (V_{IP} and V_{IN}) are continuously compared without being timed, regulated, or activated by any clock signals [32]. The function of a static comparator can be compared to that of an operational amplifier with compensation. A drawback of the static comparator is that it suffers from overshoots and undershoots. The circuit of the static comparator is elementary, but since it is always energized when in operation it tends to consume more power, especially at high switching speeds [32].

2.3.2 Dynamic comparator

The dynamic comparator typically used in high-speed ADCs is shown in Figure 6b [32]. It's operation is defined as follows: Shortly before the comparison occurs, a falling CLK signal is used to reset the comparator while turning off the clocked transistor Nt. The pre-charged transistors N7 and N8 pull the differential outputs V_{OP} and V_{ON} up to VDD. During the comparison, when the clock signal rises, N7 and N8 go off, and Nt comes on [32, 33]. If V_{IP} is found greater than V_{IN}, the whole latch (N3, N4, N5, N6) begins a charge restoration process for V_{ON} due to the charges transferred to VDD-V_{tp} via the transistor N1 before V_{OP} is reduced to this voltage level and N6 turns on ahead of N5 [34]. In this moment, $V_{OP}-V_{ON}$ is the amplified input voltage difference $V_{IP}-V_{IN}$. Finally, V_{OP} is increased to VSS as V_{ON} also reaches VDD. In case $V_{IP} < V_{IN}$, the operation of the comparator reverses. This comparator relies on vital positive feedback to perform a fast comparison. It is robust against noise and can stop the flow of current at the end of the comparison process. As a result, no static power remains in the dynamic comparator [35].

2.3.3 Non-uniform sampling ADC

Several non-uniform sampling ADCs have been investigated in the literature. The unique alias-free sampling property has been explored, and an ADC architecture has been provided that switches from standard voltage quantization to a hybrid quantization paradigm that uses both voltage and time quantization. The output can be used with a digital AA filter because of this mixed quantization method [36]. When the sample and hold circuit was activated, a non-uniform sampling system based on pseudo-randomness (PN) automatically created regular sampling, a lowered

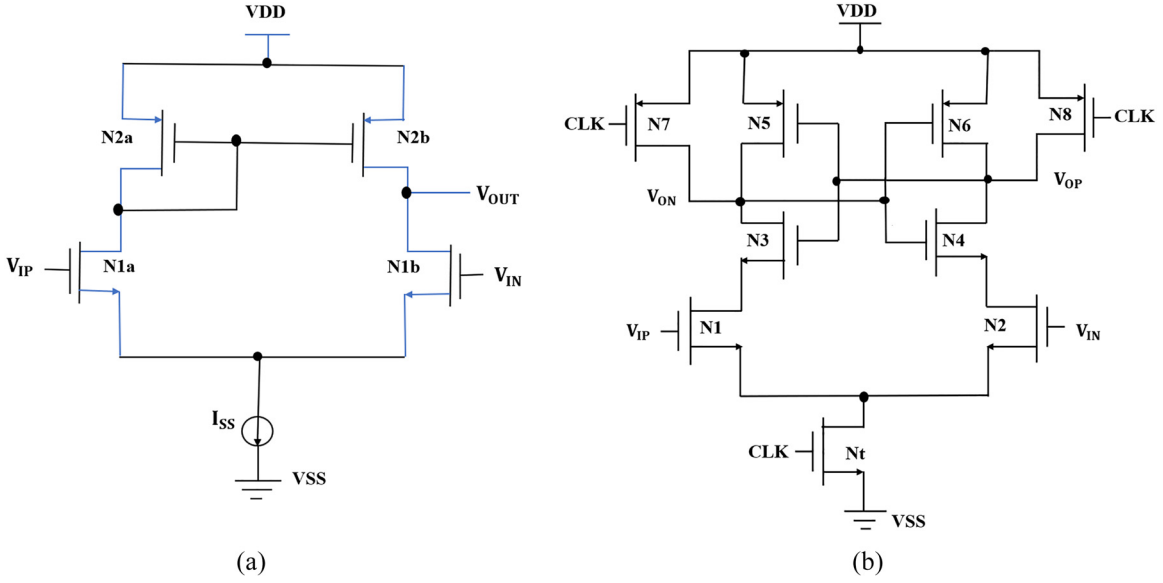


Figure 6: Schematics of the static comparator (a) [32] and dynamic comparator (b) [32, 33].

sampling rate, and ADC implication for a particular input signal bandwidth [37]. A digital AA filter is an alias-free and changeable asynchronous filter algorithm approach used within the non-uniform sampling ADC architecture. The suggested filter prevents aliasing by literally processing the non-uniform samples and dynamically adjusting the filter-restored coefficients following these irregular periodic intermissions. NeuADC uses a distinct automated strategy technique with the same hardware substrate for synthesizable A/D adaptation with changeable quantization sustenance [38]. NeuADC is built on a universal NN hardware substrate using NN as inspiration and is made possible by a cutting-edge dual-path mixed-signal RRAM crossbar architecture [39].

3 Methodology

Within this section we describe how we constructed an optimized comparator and how we extended the circuit towards yielding a (re)programmable threshold.

3.1 RRAM-based comparator

3.1.1 Novel modified CMOS comparator design: We have depicted our proposed comparator structure in Figure 7, which is a modified two-stage CMOS comparator with the primary goal of designing a low-power, low-delay, and high-speed comparator. It consists of a differential amplifier, input stage, and an inverter output stage. The advantage of a two-stage CMOS comparator is that the circuit requires the minimum number of transistors, ultimately resulting in reduced area consumption. The initial phase is a differential amplifier (N1, N2, N8, N5), the middle is a common-source amplifier (N4, N7), and the final is an inverter stage (N9, N10, N11, N12). The biasing circuit stage of the amplifier is accomplished with transistors (N4, N7, N6, and N3). The differential pair is connected to the two analog input voltages, V_{IP}, and V_{IN}. To enhance the gain of the first stage and decrease the input offset voltage, we increased the widths of the input differential pair, N1-N2. To decrease the parasitic capacitance at the N7 gate and, consequently, the propagation delay, the area of the common-source transistor was decreased. A CMOS inverter is used in the third stage, improving the comparator and adding a small amount of gain. All the other transistors act as for switching operations. The supply voltage in this circuit is 1V, while the input bias current is designed to be 50 μA. In Table 3, the dimensions of the transistors in the proposed comparator structure are presented. The circuit is designed with appropriate W/L ratios to obtain better performances in terms of delay and power. Compared to conventional architectures, the comparator power consumption and delay have improved. The key benefit of this type of comparator is that no power is wasted from the supply when the comparator is not in use. This comparator controls the leakage current on the device. It is the main advantage of this comparator, and its performance is excellent (delay) compared to those covered in refs. [35, 40, 41].

3.1.2 Design criteria for the CMOS two stage comparator: The positive and negative power supplies are referred to as VDD and VSS or GND, respectively. The NMOS and PMOS threshold voltages are denoted by VIP and VIN. In contrast, the transconductance parameters of NMOS and PMOS transistors are represented by $K_n = u_n.C_{\text{ox}}$ and $K_p = u_n.C_{\text{ox}}$, respectively [27, 42].

Where C_{ox} = gate oxide capacitance per unit area.

u_n, u_p = signifies the electron and hole mobility.

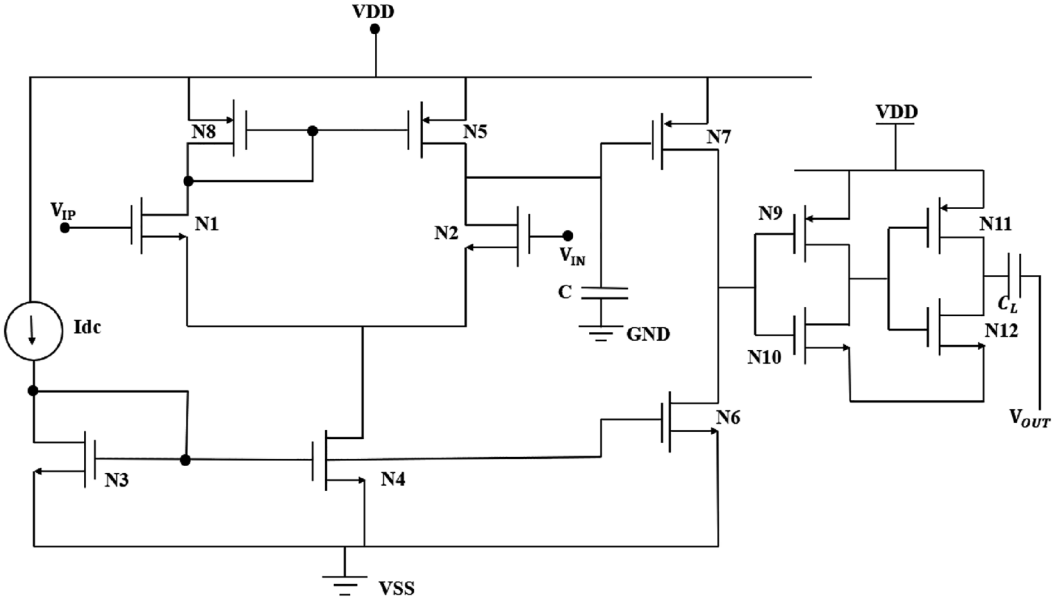


Figure 7: Modified comparator schematic.

The process of creating a CMOS comparator has been explained by others [27, 30, 42] and is being repeated here for reference:

The gain of this stage is equivalent to the transconductance of N4 multiplied by the combined effective load resistance of the N4 and N7 output resistances. N6 serves as the load, whereas N7 requires a current to fulfill the slew rate. The current flow through N_7 can be determined as follows:

$$I = C\frac{\mathrm{d}v}{\mathrm{d}t} \tag{3}$$

where I represents the flow of current through a capacitor, and V represents the voltage across it. Subsequently the Slew rate S_R can be determined as follows

$$S_R = \frac{ID_7}{C_L} \tag{4}$$

$$ID_7 = (S_R)C_L \tag{5}$$

Size of N_6

$$\frac{N_6}{L_6} = \frac{2I_{\mathrm{DS6}}}{K_p[V_{\mathrm{DS6}}]^2} \tag{6}$$

Size of N_7

$$\frac{N_7}{L_7} = \frac{2I_{\mathrm{DS7}}}{K_p[V_{\mathrm{DS7}}]^2} \tag{7}$$

Following the above rule, we calculated the remaining transistor size.

Gain of the first stage

$$A_{v1} = \frac{g_{n1}}{g_{n2} + g_{n5}} \tag{8}$$

Gain of the Second stage

$$A_{v2} = -\frac{g_{n6}}{g_{n6} + g_{n7}} \tag{9}$$

Current values passing via N1, N2, N3, N4 and N6.
$I_{\mathrm{DS1}} = I_{\mathrm{DS2}} = I_{\mathrm{DS3}} = I_{\mathrm{DS4}} = I_{\mathrm{DS6}}$.
* N4, ascertain the current I_{DS4} that the mirror with N6.

$$I_{\mathrm{DS4}} = \frac{(W/L)_4}{(W/L)_6} \times I_{\mathrm{DS6}} \tag{10}$$

The comparator receives the biasing current from the biasing circuit. Biasing current is described in ref. [43]:

$$I_{\mathrm{ds}} = \frac{k}{2}\frac{w}{l}(V_{\mathrm{gs}} - V_{\mathrm{th}})^2(1 + \lambda V_{\mathrm{ds}}) \tag{11}$$

The W/L ratio is computed according to the biasing currents of the transistors.

3.1.3 Proposed RRAM based comparator: In this section, we introduce the proposed memristor-based comparator with hysteresis, as shown in Figure 8. The application of the CMOS comparator part has been explained in the previous section. Table 2 shows the set of parameters fed to the Memristor model to simulate the behavior of the IHP's 130 nm technology RRAM cells [44]. The circuit configuration uses a voltage divider which is used to set up an upper threshold voltage (V_H) to transition below a lower threshold voltage (V_L). The comparator input signal is applied to the inverting input. The memristor network comprising N_1, N_2, the voltage divider, and N_3 – the hysteresis level, as used in this circuit has been preprogrammed to set the hysteresis at the desired value [13]. If the supply voltage causes the output to reach

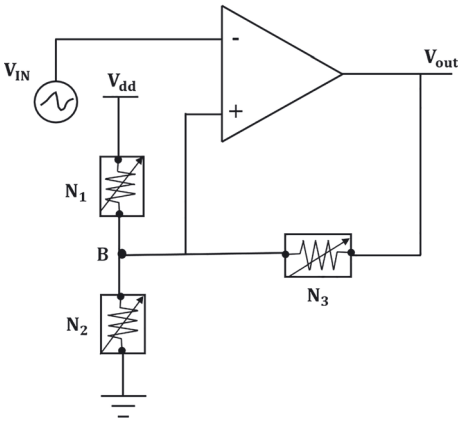


Figure 8: RRAM based comparator.

1V memristor N_3 is set in parallel with memristor N_1, raising threshold voltage node B [13, 45].

This concept and the following equations have been proposed by others [13, 46], our contribution lies within adapting this to a given CMOS process and a specific RRAM device.

$$V_H = \frac{N_2}{N_2 + \frac{N_1N_3}{N_1+N_3}}.V_{dd} \tag{12}$$

$$V_H = \frac{N_2N_3 + N_1N_2}{N_1N_3 + N_2N_3 + N_1N_2}.V_{dd} \tag{13}$$

Similarly, when the supply voltage causes the output to reach 0 V, N_3 is set in parallel with N_2, thus reducing the current to memristor N_2 and the threshold voltage V_L [13, 45].

$$V_L = \frac{\frac{N_2N_3}{N_2+N_3}}{N_1 + \frac{N_2N_3}{N_2+N_3}}.V_{dd} \tag{14}$$

$$V_L = \frac{N_2N_3}{N_1N_3 + N_2N_3 + N_1N_2}.V_{dd} \tag{15}$$

A transition happens when the input voltage is below V_L. The following hysteresis voltage equations are derived from Equations (13) and (15) [13, 45].

$$V_H - V_L = \frac{N_2}{N_2 + \frac{N_1N_3}{N_1+N_3}}.V_{dd} \tag{16}$$

$$V_H - V_L = \frac{N_1N_2}{N_1N_3 + N_2N_3 + N_1N_2}.V_{dd} \tag{17}$$

$$V_{dd} - V_H = V_{dd} - (\frac{N_3N_2 + N_1N_2}{N_1N_3 + N_2N_3 + N_1N_2}).V_{dd} \tag{18}$$

$$V_{dd} - V_H = \frac{N_1N_3}{N_1N_3 + N_2N_3 + N_1N_2}.V_{dd} \tag{19}$$

Table 2: RRAM model parameters as fitted by [24].

go = 5e-10	**Vo = 0.27 V**	**I0 = 0.0003**
vo = 0.8 m/s	$\beta = 5.2$	$\alpha = 2.1$
gapini = 1.5e-10	$T_o = 300$ K	$\gamma = 22$
gapmax = 1.5e-10	$t_{\mathrm{ox}} = 6$ nm	$I_o = 0.003$
Ea = 0.6 eV	$R_{\mathrm{th}} = 1500$ K/W	$\gamma_{\mathrm{reset}} = 15.3$ nm

Table 3: Transistor sizes/part specifictions in the circuit shown in Figure 7.

Part	Width/length	Part	Width/length
N1	0.15 µ/0.13 µ	N8	0.8 µ/0.13 µ
N2	0.15 µ/0.13 µ	N9	0.8 µ/0.13 µ
N3	0.15 µ/0.13 µ	N10	0.8 µ/0.13 µ
N4	0.15 µ/0.13 µ	N11	0.8 µ/0.13 µ
N5	0.15 µ/0.13 µ	N12	0.8 µ/0.13 µ
N6	0.15 µ/0.13 µ	I_{dc}	50 mA
N7	0.15 µ/0.13 µ	C, C_L	20 pf

The resistance of the memristors N_1, N_2 and N_3 should be chosen to be very high in order to minimize the current consumption of this circuit. Equations (12) and (14) show the equations for setting the threshold voltages. We obtain the following equations from Equations (13), (15) and (17)–(15) and (19)(15) and (17)–(19)(15) and (17)–(19) [13, 45].

$$\frac{N_1}{N_3} = \frac{V_H - V_L}{V_L} \tag{20}$$

$$\frac{N_1}{N_2} = \frac{V_{dd} - V_H}{V_L} \tag{21}$$

The hysteresis threshold voltages (V_H and V_L) are described in Equations (20) and (21), respectively.

3.2 Non-uniform sampling ADC and model parameters

We can use the comparator shown earlier to implement a non-uniform ADC or a sensor evaluation circuit by stacking multiple of these blocks and having them switch at non-uniformly distributed voltages. We will demonstrate the reprogrammability within the next section.

We have used the Stanford PKU memristor model parameters as fitted by Reuben et al. [24] and as depicted in Table 2.

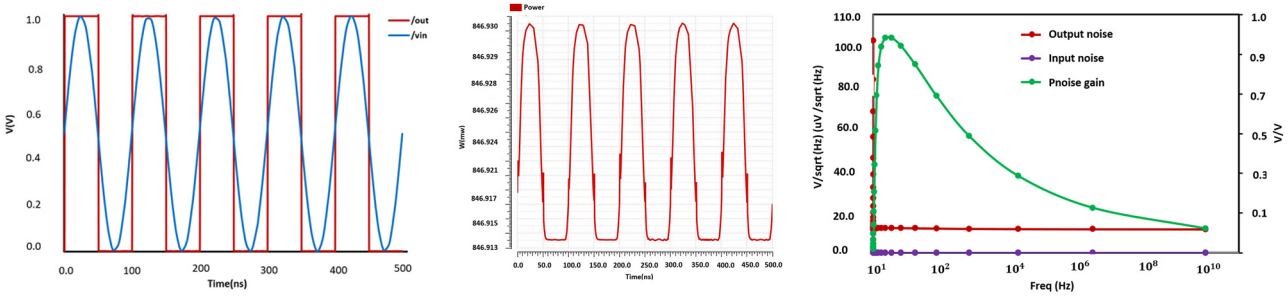
4 Evaluation

4.1 Comparator design

In this section, we will evaluate the proposed design as ported to the 130 nm process. We use Cadence Virtuoso to achieve the depicted simulation results. All simulations are performed considering 1V of supply voltage at T = 27 °C operating temperature. We used an input clock of 10 MHz with a rise and fall time of 50 ps each. The transient analysis of the proposed comparator is shown in Figure 9a. In this situation, the difference between the two inputs is 5 mv. Using the concepts described earlier the total power consumption for the proposed circuit is 8.64 µW. Figures 10 and 11 depict Monte-Carlo simulations (2000 samples) for both power consumption and delay; The total power consumption is 847.364 mw and the standard deviation is 6.188 mw. As one can see the average delay seems to be 51.63 ps, with a standard deviation of 1.31. The dynamic power consumption variation is shown in Figure 9b. The simulation results in noise performance are shown in Figure 9c, showing the effects of input-referred noise, output noise, and phase noise margin, respectively, for the proposed comparator. The graph plot shows the relationship between Frequency (Hz) and V/sqrt referred noise (V/Hz). The merging technique, on the other hand, has been used in preamplifier transistors to increase speed and decrease the delay. The achieved specifications of the implemented comparator circuit are shown in Table 4. A comparison of the proposed comparator with designs proposed in literature is presented in Table 5. The proposed technique seems to be promising regarding delay; The power consumption is not directly comparable since this circuit is highly optimized for the specified application. The next Section will illustrate that the circuit uses way less power when integrated into the RRAM circuit.

4.2 Comparator RRAM optimizations

In this section we show the effectiveness of our proposed comparator design for the usage with RRAM devices. As discussed, the proposed RRAM comparator design can preserve its pre-programmed state, acting similarly to a



(a) (b) (c)

Figure 9: Results: transient analysis (a), corresponding power consumption (b) and noise response (c) of our design.

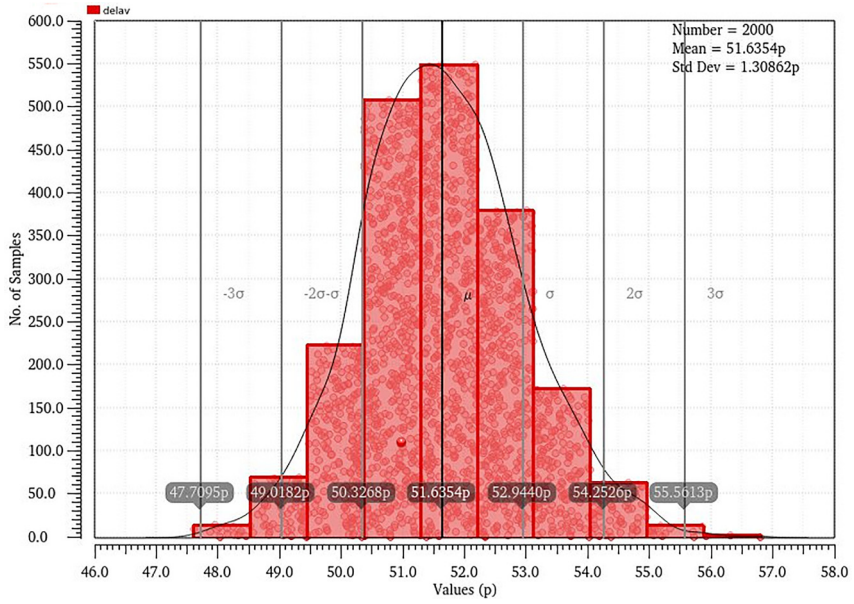


Figure 10: Monte Carlo simulation result for delay.

conventional resistor. Figure 12 depicts the simulation verifying the threshold voltages. The input is an ideal triangle waveform. The memristor N_3 sets the hysteresis level. When the output is at a logic high (1V), N_3 is in parallel with N_1. This drives more current into N_2, raising the threshold voltage (V_H) to 504.77 mv. The input signal needs to be below $V_H = 504.77$ mv to cause the output to transition to logic low (OV). When the output is at logic low (OV), N_3 is in parallel with N_2. This reduces the current into N_2, reducing the threshold voltage to 495.07 mv. The input signal needs to increase until $V_L = 495.07$ mv to cause the output to transition to logic low (0 V). This helps avoiding glitches when the input is slightly above or beyond the desired threshold. Figure 13 depicts the output of the

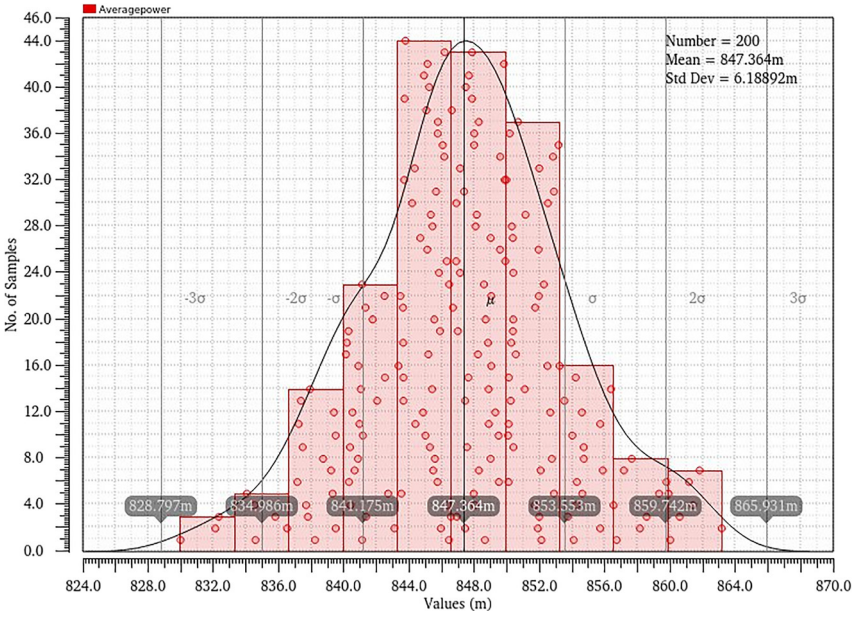


Figure 11: Monte Carlo simulation result for power consumption.

Table 4: Parameter specification of the proposed circuit.

Process file	Propsed comparator
Power supply	Vdd = 1 V ± 10 %, Vss = 0 V
Reference voltage	Vref = 0–1 V
Clock signal (CLK)	High = 1 V; low = 0 V
Delay time (ps)	51.63
Power consumption (mw)	846.364
Rise and fall time	10 ps

comparator showing a single transition in spite of the noisy triangular waveform signal at its input. V_H and V_L are set to 504.77 and 495.07 mv, respectively. The output of the memristor-based comparator hysteresis ranges from 504.77 mv to 495.07 mv. The simulation results in output noise performance are shown in Figure 14a and b. These show the effects of input-referred noise and phase noise margin, respectively, for the proposed memristor-based comparator. The graph plots also show the difference between Frequency (Hz) and V/sqrt referred noise (V/Hz). Figure 14c shows Monte-Carlo simulations (1200 samples) for power consumption of the proposed memristor-based comparator for changes in process and mismatch operations. The total power consumption is approximately 84.69 µw with a small standard derivation of 6.2 µw. Table 6 shows the simulated parameters of the proposed RRAM comparator.

4.3 Non-uniform ADC embedding RRAMs

We have programmed the memristor to modify the threshold of the comparator. Since the memristors current state is modelled using the gap model variable using the employed model we use this variable to depict the current state of the device. This is equivalent to the w/d ratio depicted in Figure 3, resulting in different device resistances. The effect of different gaps on the threshold of the comparator is depicted in Figure 15. As one can see programming the RRAM device to a given gap state leads to a different threshold. Subsequently this yields a comparator with programmable threshold. Future work should investigate how device variations impact this block.

Table 5: Comparison of the proposed design with designs proposed in literature.

	This work	2015 [40]	2014 [35]	2015 [41]
Technology CMOS (nm)	130	130	180	65
Power supply (V)	1	1.2	1.2	1.2
f_{clock} (MHz)	10	1250	500	1800
Delay time (ps)	51.63	17.8 ps/dec	550	56 ps/dec
Power consumption (µW)	846.364 mw	600	329	252
Input referred offset (mV)	0.5	7.78	7.8	5.8

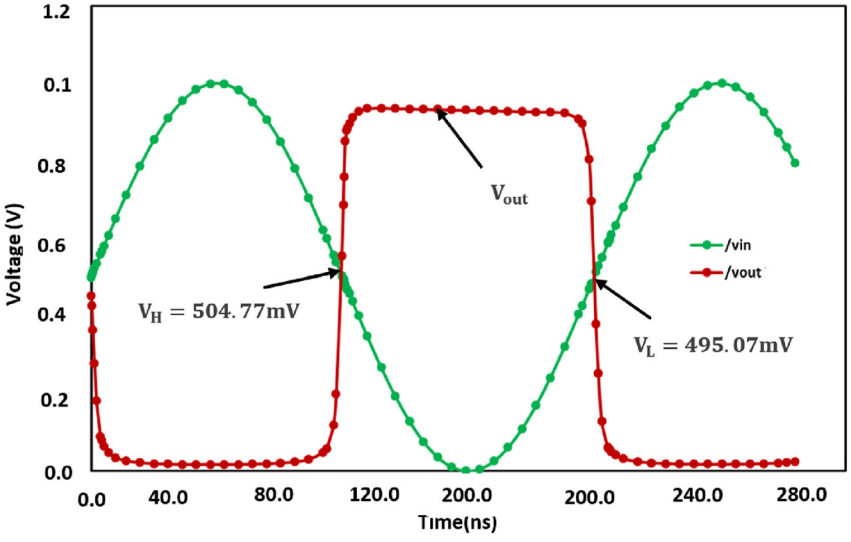


Figure 12: Simulation results: comparator behaviour without noise applied to its input.

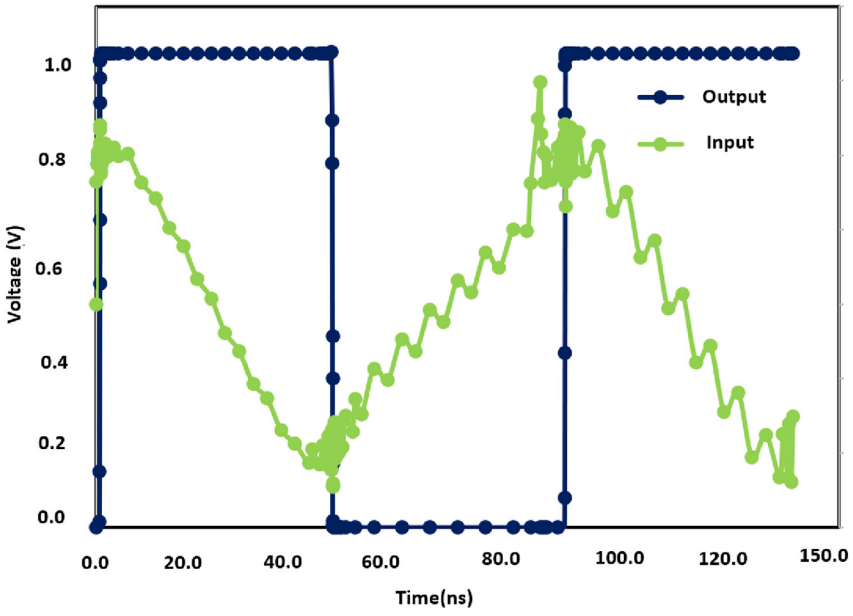


Figure 13: Simulation results: comparator behaviour when applying noise to its input.

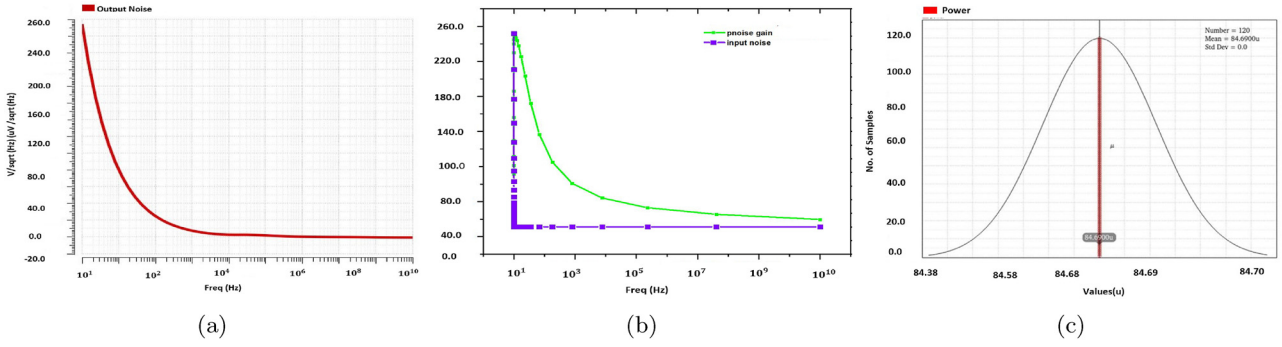


Figure 14: Output noise response (a), input and phase noise response (b), and Montecarlo simulation regarding the power consumption of the proposed comparator (c).

The programming circuit does not need to be part of the design, it can be connected externally in case a readjustment of the threshold is required. Additionally, multiple of these blocks can be combined to form a larger ADC block which is highly optimized towards the required thresholds.

Table 6: Simulated parameters of the proposed design.

Specification	Simulated result
V_H (upper threshold)	504.77 mv ± 0.1 V
V_L (lower threshold)	495.07 mv ± 0.1 V
$V_H - V_L$	504.77 mv–495.07 mv
Power consumption (µW)	84.69 µW
Suply voltage	Vdd = 1 V

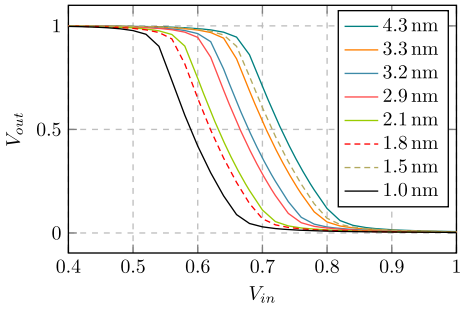


Figure 15: Simulation results: programming the RRAM device to different resistances/gaps (individual colors) leads to different threshold behaviour.

5 Conclusions

Within this paper we have demonstrated how RRAM devices can be used to create a (re)programmable comparator

by implementing this circuit using 130 nm technology. We have also elaborated how combining multiple of these blocks can form non-uniform sampling ADCs. We believe that this can help designing area and power efficient edge computing designs dealing with sensor data.

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Bionotes

Abhinav Vishwakarma
Brandenburgische Technische Universität, Cottbus—Senftenberg, Computer Engineering Institute, Konrad-Wachsmann-Allee 5, 03046 Cottbus, Germany
abhinav.vishwakarma@b-tu.de

Abhinav Vishwakarma received the B.Tech. degree in Electronics and Telecommunication Engineering from Uttar Pradesh Technical University, Lucknow, India, in 2014 and the M.Tech degree in Electronics Engineering from Madan Mohan Malaviya University of Technology, Gorakhpur, India, in 2017. He is currently pursuing a Ph.D. degree in Computer engineering with Brandenburgische Technische Universität Cottbus, Senftenberg, Germany. Before joining his Ph.D. degree, he was Research Associate in Electrical Engineering Department, Indian Institute of Technology Indore, India, from 2018 to 2019. His current research interest includes ReRAM and SRAM memory design, and Mixed-signal ICs design.

Markus Fritscher
Brandenburgische Technische Universität, Cottbus—Senftenberg, Computer Engineering Institute, Konrad-Wachsmann-Allee 5, 03046 Cottbus, Germany; and IHP — Leibniz Institute for High Performance Microelectronics, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
fritscher@ihp-microelectronics.com

Markus Fritscher received both a B. Sc. degree in Computational Engineering and a M. Sc degree in Computer Science at the Friedrich Alexander Universität Erlangen-Nürnberg (FAU). He is pursuing a PhD degree at BTU Cottbus-Senftenberg, Germany as part of a joint researcher position at BTU and IHP — Leibniz Institute for Microelectronics, Frankfurt (Oder). His main research interests are the development and modelling of large memristive systems, dedicated frameworks which can assist with that endeavour and HPC.

Amelie Hagelauer
Chair of Micro- and Nanosystems Technology, Technische Universität München, Munich, Germany; and Fraunhofer EMFT Fraunhofer Institute for Electronic Microsystems and Solid State Technologies, Munich, Germany
amelie.hagelauer@tum.de

Amelie Hagelauer (Senior Member, IEEE) received the Dipl.-Ing. degree in mechatronics and the Dr.- Ing. degree in electrical engineering from the FAU Erlangen-Nuremberg, Germany, in 2007 and 2013, respectively. In November 2007, she joined the FAU Institute for Electronics Engineering, where she researched on BAW resonators and filters towards her Ph.D. degree. Since 2013, she has been focusing on SAW/BAW and RF MEMS components, as well as on microwave integrated circuits for frontends. From 2016 to 2019, she had been leading a Research Group on electronic circuits and from August 2019 to September 2021 she was a Full Professor at the University of Bayreuth, Germany. In September 2021, she joined the Technical University of Munich (TUM) as a Full Professor and became the Co-Director of the Fraunhofer Institute for Electronic Microsystems and Solid State Technologies EMFT, Munich. She has authored or co-authored more than 150 peer-reviewed publications in her research fields, which include research and development of microwave theory and technology, electronic circuits and systems, and communication and sensing systems. She acted as a Guest Editor for a special issue of the IEEE Transactions on Microwave Theory and Techniques on the topic RF Frontends for Mobile Radio and as an Associate Editor of the IEEE Transactions on Microwave Theory and Techniques.

Marc Reichenbach
Brandenburgische Technische Universität, Cottbus—Senftenberg, Computer Engineering Institute,
Konrad-Wachsmann-Allee 5, 03046 Cottbus, Germany
marc.reichenbach@b-tu.de

Marc Reichenbach (Member, IEEE) received the Diploma degree in computer science from Friedrich-Schiller University Jena, Germany, in 2010, and the Ph.D. degree from FriedrichAlexander University Erlangen-Nürnberg (FAU), Germany, in 2017. From 2017 to 2021, he worked as a Postdoctoral Researcher at the Chair of computer architecture, FAU. Since 2021, he has been heading the Chair of computer engineering at the Brandenburg University of Technology CottbusSenftenberg (BTU), Germany, as a Substitute Professor. His research interests include novel computer architectures, memristive computing, and smart sensor architectures for varying application fields.