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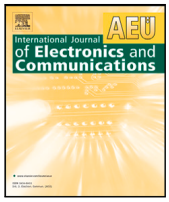

Design of radiation-tolerant digital-to-analog converter and investigation on analog single event transient effects

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ABSTRACT

A circuit design methodology for space applications is presented with an 8-bit resistive digital-to-analog converter (DAC) with XY addressing mode and BiCMOS buffer designed in IHP's 130 nm SiGe BiCMOS technology (SG13S). The radiation tolerance of the implemented DAC is evaluated by circuit-level simulations particularly analyzing the radiation sensitivity of the DAC to analog single-event transients (ASETs). Radiation mitigation techniques are addressed. The total current consumption with a 3.3 V supply is 0.54 mA at a 1 MHz sampling frequency.

1. Introduction

Space applications are among the many fields that benefit from advancements in semiconductor technology. Extremely hostile space environments including intense radiation fields, large amounts of chemical corrosion, mechanical stress and any combination of extremely low or high temperatures are encountered by microelectronics for space applications. One of the most challenging issues faced by the electronic systems used for space applications is its vulnerability to radiation and increasing rates of failure [1]. Therefore designing radiation-tolerant or hardened electronics is crucial and indispensable for space applications.

Semiconductor devices exposed to radiation can have two major effects that impact their reliability namely cumulative-effects and single event effects. Cumulative effects also known as total ionization dose (TID) effects are characterized by the accumulation of gradual effects mainly the shift in the device parameters over the lifetime of electronics as a result of the deposition of energy by radiation during chronic exposure to a radiation environment [2]. The semiconductor device fails when the accumulated dose reaches the tolerance limits. Whereas single particle or photon passage through the semiconductor device triggers the spontaneous, random disruptions known as the single event effect (SEE) [2].

Data converters are crucial components in integrated circuits. Therefore, a digital-to-analog converter (DAC) is considered an exemplary circuit in this work, to understand the circuit design methodology for space applications. Since DAC design involves both analog and digital circuits, it offers a great opportunity to understand the radiation behavior of both types of circuits. Several radiation-tolerant design methods are presented in the literature [3,4]. However, this work aims to investigate the radiation susceptibility of the DAC under the influence of analog single-event transients (ASETs) on the analog auxiliary circuits providing the reference and biasing voltages to the DAC.

The single event effect (SEE) is a function of energy, linear energy transfer (LET) trajectory, biasing, local layout, layers and a myriad of circuit details. SEE mechanism could be split into a sequence of phases when a high-energy particle is injected into the semiconductor device and generates charges. Initially, a non-equilibrium condition is created in the semiconductor device, along the path traversed by the energetic ion as it leaves behind the charge carriers in excessive amounts. As a response carrier transport and carrier recombination mechanisms occur at the material to restore the equilibrium. Transients are created by the drift and diffusion mechanisms of the carrier transport in microelectronics. If the active devices are far away from the ion event, then there is a harmless collection of charge by the substrate. Whereas, if the ion traverses across or near the volumes of active devices the functionality of the device can be impacted by the collected charge [2]. The basic literature provides a detailed description of the radiation effects on the semiconductors and could be followed for further information [2,5].

Single-event effects can be broadly classified into two categories namely nondestructive SEE and destructive SEE. As the name suggests non-destructive SEEs do not destroy the semiconductor device or circuit even though it corrupts the data state or disrupts the output. The self-recovering transient disruptions, in the combinational logic or analog circuits with no memory, caused by the radiation event, return functionality of the circuit as soon as the excess charge has been removed

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from the struck junctions. As these non-equilibrium charges are cleared by the recombination and transport mechanisms an external input is not necessary to restore the state of the system.

Analog single-event transients (ASETs) are classified under non-destructive SEE. Single-event transients that affect the output of analog circuits, like amplifiers and comparators by causing a transient disturbance for a short period of about 100 ps to a few ns, are known as analog single event transients (ASETs). There are certain parts/nodes of the analog circuit blocks/ individual circuitry which are more sensitive to the ASETs depending on the magnitude, shape and duration of the transients [2]. Whereas digital single event transients (DSETs) are generated in the digital circuits, composing combinational circuits and/or a clock tree, and propagate as a narrow glitch through them. DSETs are broadened and attenuated at individual stages following down the stream. While most of the SETs do not have the potential to cause reliability issues as they are below the threshold of the digital voltage, a few larger SETs can impact the systems down the line. From the reliability point of view, corruption of the circuit components downstream is of major concern. This could be caused by the persistent erroneous data in the sequential circuits as a consequence of DSETs in those circuits [2].

In this paper, we present general guidelines for designing a radiation-tolerant circuit using a DAC as the test vehicle. We focus on the susceptibility of the auxiliary analog circuits to ASETs. Specifications of the DAC are such that it could be designed straightforwardly, therefore providing ample attention to evaluate the radiation effects on the circuits. The 8-bit DAC architectural and circuit design details are described in Section 2. Section 3 aims to evaluate the radiation tolerance of various circuits, identify the critical circuit blocks, and implement the circuit-level mitigation methods if required, particularly focusing on the simulation approach to assess the design reliability at the primary phase of a design cycle. Section 4 discusses the implemented results. The circuits are implemented at the layout level in IHP's 130 nm SiGe BiCMOS technology (SG13S), offering excellent TID immunity and optimal mixed-signal design flexibility at the monolithic level.

2. Circuit design

3. Design flow

At first, the flow diagram to design a radiation-tolerant circuit needs to be outlined. While [6] reported a design flow of SET effects modeling for digital circuits at a system level, work of [7] has proposed a flow diagram of the design methodology at a circuit level focusing on SET effects. Inferring from these design flows and considering the TID effects a general design flow of radiation tolerant circuit is laid out as presented in Fig. 1. To begin the circuit design select the architecture, individual components and device parameters that show radiation resiliency. Simulate the designed circuit and characterize the nominal results as simulated pre-radiation results. Determine a representative key performance figure to evaluate the radiation effects on the concerned circuitry. Characterize the TID immunity of the circuit by observing the change in the key performance figure of the circuit for the modified device parameter at the simulation level, that corresponds to the variation in the device parameter due to TID effects. If the circuit tolerance is not sufficient enough, then use mitigation methods to increase the immunity of the circuit against the TID effects. Furthermore, to evaluate the SET sensitivity of the circuit emulate the SET-induced current using a reverse-biased pulse current model. Inject the charge on each node (N_i) of the circuit to evaluate its vulnerability to SET effects. Identify the sensitive nodes by comparing the obtained results with the key performance figure obtained during the pre-radiation simulations. Record the sensitive node(s). Once all the sensitive nodes are noted then try to reduce the circuit sensitivity by applying the mitigation techniques without altering the functionality of the circuit. Re-evaluate the SET sensitivity of the modified nodes (M_i) of the circuit. If the circuit is still too sensitive then a different or additional mitigation technique has to be implemented. Several iteration cycles might need to be performed to evaluate the effectiveness of the mitigation techniques and to finally achieve the radiation-tolerance.

Table 1
Overview of DAC designs for space applications available in the literature.

	[10]	[11]	[4]
Technology	130 nm CMOS	180 nm CMOS	500 nm BICMOS
Architecture	Resistor string	R-2R ladder	R-2R ladder
Design techniques	Poly-res[a], ELT	Poly-res[a], guardrings	guardrings
Resolution	10 bit	8 bit	12 bit
Sampling rate	3 MS/s	N/R[b]	100 kHz

[a] Polysilicon resistors.
[b] Not reported.

3.1. Architecture selection

The first step in the DAC design flow is the selection of the DAC architecture based on the requirements namely resiliency to radiation effects, electrical requirements and area occupation. DAC architectures can be broadly categorized into resistor-based architectures, capacitive architectures and current source-based architectures [8]. Comparison of DAC architectures reported in [3] shows the sensitivity of the DAC to radiation effects and possible design-level interventions to increase the resiliency of the DAC. Resistors, that are not based on active layers, like polysilicon or thin film resistors in resistive DACs are generally tolerant to radiation since they are devoid of the sensitive active area as reported in [5,9]. Whereas, capacitive DACs are sensitive to SET whose energy is higher than the critical charge and the current sources in current steering DACs are very sensitive to TID since even a minimum MOS threshold variation could be critical [3]. Table 1 gives the overview of different techniques used to design a radiation-tolerant DAC available in the literature.

Resistor-based architecture is selected for this work as it is evident that the resiliency of resistor-based architecture is better when compared to other architectures as it is devoid of the sensitive active area and also requires fewer design-level interventions. Details of the resistive architecture of the DAC described below mainly follow the explanation from the basic literature and can be referred to for more details [8]. Resistive DAC with X-Y addressing scheme and shunt resistors, also known as segmented architecture [8] is designed as shown in Fig. 2. The main advantage of using shunt resistors across each line of an X-Y arrangement is that the time constant can be reduced without reducing the unit resistance as given in (1). Thus the power consumption across the resistive divider can be reduced along with a better matching performance. The following expressions on the unit resistance calculations considering the settling time constraint can be considered to demonstrate these advantages.

$$R_{eq} = \frac{k R_u R_s}{k R_u + R_s} \tag{1}$$

where R_u is the unit resistance of the unity elements of the resistor string, k is the number of unity elements in the resistor matrix, R_s is a shunt resistance.

3.2. DAC sub-circuits

3.2.1. Resistor matrix

Once the suitable architecture is chosen, selecting a resistor for the matrix is the following step. The major criteria for the resistor selection are radiation resiliency, settling time, power, mismatch and noise levels. Resistors based on polysilicon are selected due to their insensitivity to radiation.

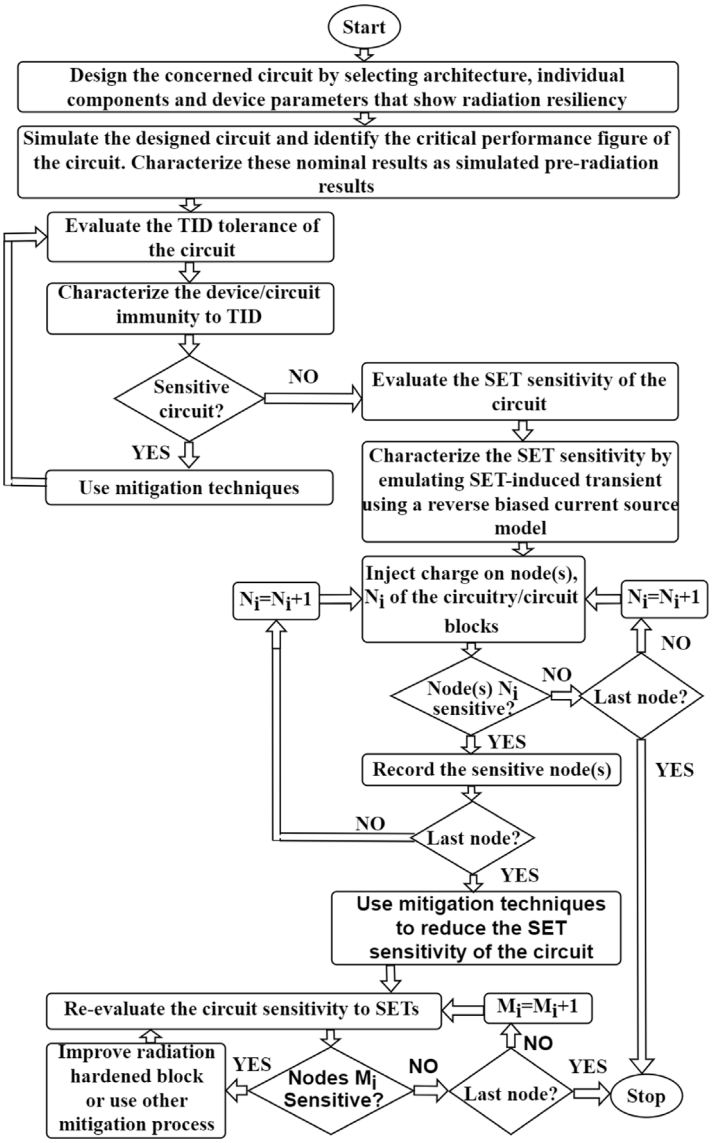

Fig. 1. RT Designflow.

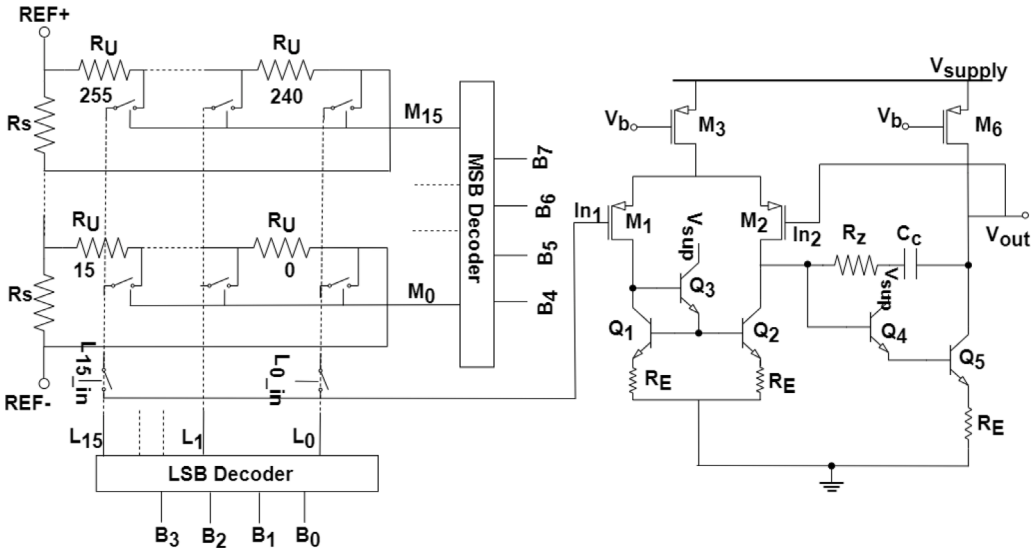

Fig. 2. Schematic of resistive DAC with XY addressing scheme and BiCMOS buffer [8,12].

Table 2
Unit resistance calculation considering settling time.

Parameters	C_{in}	t_{conv}	Error	n	t_{total}	R_{u-XY}	$R_{u-shunt}$
Values	1 pF	1 µs	0.0039	6	166.6 ns	2.603 kΩ	41.65 kΩ

Table 3
Unit resistance calculation considering noise level.

Parameters	k	BW	T	V_{n-max}	$R_{u-shunt}$
Values	13.8E−24 J/K	1 MHz	300 K	1.9531 mV	231.25 MΩ

Settling time $\mathbf{t}_{total}$ of the DAC should be well below (represented by **n**) the DAC conversion time $\mathbf{t}_{conv}$ as given in (2) to achieve a spur free output spectrum [8].

$$t_{total} = \frac{t_{conv}}{n} \tag{2}$$

where n can be calculated using (3) .

$$n = -ln(Error) \tag{3}$$

Error can be calculated using (4)

$$Error = \frac{V_{lsb}}{V_{ref}} \tag{4}$$

where V_{lsb} can be calculated using (5) [13]:

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{5}$$

where 2^N represents the number of input combinations, $N = 8$ bit, $V_{ref} = 1$ V, $V_{LSB} = 3.90625$ mV.

Once the settling time required by the resistor matrix is calculated as given in Table 2 using the above equations, unit resistance can be calculated. Equivalent resistance is parabolic in nature [8]. While Eq. (6) can be used to calculate a unit resistance (considering maximum value of the equivalent resistance) of the resistive DAC with X-Y addressing scheme, Eq. (7) provides a unit resistance (considering maximum value of the equivalent resistance) of the resistive DAC with X-Y addressing scheme and shunting resistors.

$$R_{u-XY} = \frac{t_{total}}{2^{N-2} \cdot C_{in}} \tag{6}$$

$$R_{u-shunt} = \frac{t_{total}}{2^{\frac{N}{2}-2} \cdot C_{in}} \tag{7}$$

where C_{in} is the parasitic capacitance loading the input of the buffer.

Noise caused by the resistors limits the maximum value of the unit resistance. The equivalent resistance given in (9) depending on maximum noise level voltage calculated using (V_{n-max}) (8) is given in Table 3. Then, the respective unit resistance is calculated using (1).

$$V_{n-max} \leq \frac{1}{2} V_{LSB} \tag{8}$$

$$V_{n-max} = (4 \cdot k \cdot T \cdot BW \cdot R_{eq})^{\frac{1}{2}} \tag{9}$$

where k is the Boltzmann constant, T is the room temperature and BW is the bandwidth.

To determine the best matching behavior of the resistors Monte-Carlo simulations (statistical simulations) have been performed on the available types of polysilicon resistors. If the standard deviation of the voltage, caused by the process and mismatch variations in the resistors, is greater than half of the V_{LSB}, then such resistors are not to be used in the resistor matrix of the DAC. Table 4 gives an analysis of the voltage at matrix mid-code since it is the most affected voltage by mismatches which is 500 mV in this work for different types of resistors available in SG13S technology. A resistor of 4 kΩ is selected as a unit resistor for the resistor matrix considering the power constraint (≤300 µW) as well as the smaller chip area. It can be seen from the following results that the resistor of type Rppd has the least standard deviation over 500 samples for a wide range of temperatures, therefore offering a better choice. An 8 bit Kelvin divider with X-Y addressing scheme and shunting resistor as shown in Fig. 2 has 2^4 coarse resistors (shunting resistors) R_{Cx} and 2^4 strings of fine resistors where each string consists of 2^4 fine resistors R_{Fx}.

Table 4
Monte-Carlo simulation results on voltage at matrix mid-code.

Resistor (4 kΩ)	Std. deviation of V_{out} (mV)		
	−40 °C	25 °C	125 °C
Rsil	1.1011	1.1017	1.1010
Rppd	0.5596	0.5598	0.5599
Rhigh	4.1193	4.1112	4.1288

Table 5
Boolean expansion of the 4 to 16 bit decoder logic.

Input	Output (form 1)	Output (form 2)
0000	a'b'c'd'	(a+b+c+d)'
1000	ab'c'd'	(b+c+d)' a

A classical transmission gate (TG) is used in this work as a switch. The device aspect ratio of (width(W)/length(L)) of 10 is determined by considering the on-resistance (r_{on}) of the switch (357.6 Ω). A larger switch size (W = 5 µm/L = 0.5 µm) helps to reduce the SET effects as the critical charge required to generate an ASET is increased by increasing the transistor sizes recommended in [1,14,15]. In this work IHPDK's standard transistor PCELL is used to layout the design. Special structures like enclosed layout transistors (ELTs) are not implemented in this work and the future work aims to incorporate them only on critical devices when high TID tolerance is required [16].

3.2.2. Decoders

X-Y selection scheme of the 8-bit resistive DAC groups the 8-bit input digital data into two parts where the 4 most significant bits are used to control the switches of the lines (rows) in a resistor matrix while the 4 least significant bits drive the switches of the columns of the matrix. Since the switches are laid in 16 rows and 16 columns, each of the 4-bit input data groups needs to be decoded into 16-bit data to drive these switches. Therefore, two N to 2^N decoders are designed with N = 4. 8 bit input data can be represented as 4 MSB and 4 LSB. Logic gates required for the decoder are determined using Boolean expressions obtained by solving the Karnaugh map with the sum of products. Logic gates used in this work are taken from the customized digital library available in the IHP-PDK for SG13S technology and are supplied with 1.2 V supply voltage. An example of the Boolean expansion of the 4 to 16 bit decoder logic is given in Table 5 in two forms, where the output (form 2) is a simplified Boolean expression of the output (form 1) using De Morgan's theorem.

3.2.3. Output buffer

To design a buffer that passes the output of the resistor matrix to the next stage, its effects on the output voltage settling have to be considered. Parameters limiting the dynamic performance of the buffer are mainly gain-bandwidth product (f_T) and slew rate (SR). For the DAC with a conversion period of 1 µs, (f_T) of 1 MHz is sufficient for the buffer to work without excessive signal distortion. Due to the limitations rendered by the input common mode range and the output swing of the buffer given in Table 7 the full-scale voltage of the DAC scales from 0.3 V (V_{REF-}) to 1.3 V (V_{REF+}), instead of 0 V to 1 V. Two-stage OpAmp with a Miller compensation as shown in Fig. 2(a) [12] is chosen for this task since it is straightforward to implement and yet provides a sufficient gain. The reason to choose a simple OpAmp is its sensitivity to radiation effects, as the performance of the OpAmp degrades with an increasing level of its complexity as

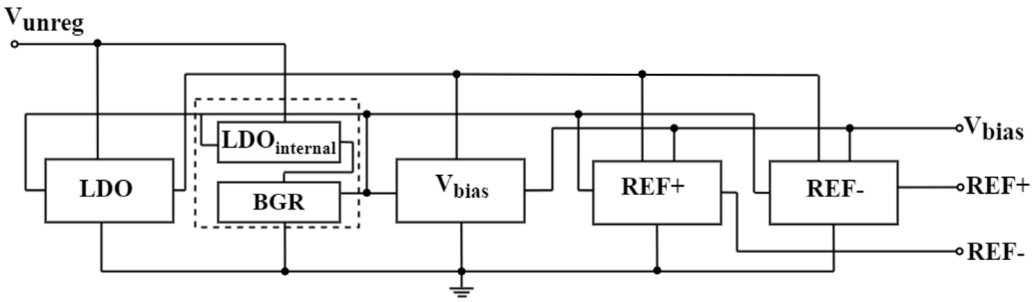

Fig. 3. Block diagram of auxiliary analog circuits required to operate the DAC. An internal LDO regulator provides the regulated supply voltage to the BGR circuit to achieve a supply-independent reference voltage.

Table 6
LSB value obtained from the DAC for different gain of the ideal OpAmp.

Gain (dB)	20	40	60	80
LSB (mV)	3.551	3.868	3.902	3.906

Table 7
Specifications of the designed unity gain buffer.

Parameter	Conditions	Value
Supply (V_s)		3 V
Input common mode range		0.2–2.56 V
Output swing	R_L = 50 kΩ	0.084–2.8 V
	R_L = 35 kΩ	0.08–2.6 V
Slew rate		5.72 V/μs
Open-loop gain		96.5 dB
Phase margin		89.5°

reported [3,17]. While stage 1 is made of a differential amplifier, stage 2, which is a gain stage, consists of a common source amplifier. The minimum open loop gain (A_v) required for the OpAmp is determined by observing the LSB output from an ideal OpAmp available in the analogLib library in Cadence Virtuoso. As it can be seen from Table 6 that the (A_v) of 80 dB would result in the expected V_{LSB} of 3.906 mV, however, 60 dB would also result in a reasonable V_{LSB}. The achieved specifications of the implemented OpAmp are given in Table 7.

3.3. Voltage reference

As the Kelvin divider network divides the reference voltage in order to tap the equivalent analog voltage for the digital input, reference voltage needs to be generated. Reference voltage with temperature and supply independency is generated using a bandgap reference circuit (BGR) by adding proportional-to-absolute temperature (PTAT) voltage with a base-emitter voltage [18]. Using self-biased cascode topology, the need for the biasing circuits is avoided. To achieve better supply independence a PMOS low dropout regulator (LDO regulator) is used which provides the internal supply voltage (V_{DDi}) of 2.44 V to the bandgap reference circuit. Even though, the BGR voltage of 1.08 V can be directly used as a reference voltage for the resistor matrix, V_{in-CM} of the buffer limits using it. To overcome this situation, a voltage source providing a voltage (V_{ref-}) of 300 mV is placed at the bottom of the divider network. To achieve a reference of 1 V, the voltage from the bandgap reference circuit that is applied at the top of the resistor matrix is DC shifted to 1.3 V (V_{ref+}). The DAC output buffer works with 3 V (V_{reg}) which is a regulated voltage from 3.3 V (V_{unreg}) main supply to reduce the supply dependency. The biasing voltage required to operate the transistors $M_{1,6}$ is provided by the biasing circuit V_{bias}. Therefore, the required circuits as shown in Fig. 3 are bandgap reference circuit, voltage regulator, OpAmp's biasing circuit, circuits proving V_{ref+} and V_{ref-}.

4. Results

4.1. Pre-radiation simulations

At first, the pre-radiation simulations are carried out to characterize the performance matrix of the designed DAC. Up-counter provides the consecutive pulses with a frequency of 1 MHz, required for the incremental digital input word from "00000000" to "11111111" for the DAC simulations. Fig. 4(a) and (b) presents the static performance DNL and INL of the initial DAC respectively at the post-layout level. The critical parameter DNL of the DAC shows that the designed DAC is monotonous since the DNL is less than −1 LSB, hence fulfilling the requirement of monotonicity. The dynamic performance is characterized by the sine wave for the input frequency of 3.90625 kHz from (10) [19] defining the N separate DFT analysis frequencies considering m=1.

$$f_{\text{analysis}}(m) = \frac{m \cdot f_s}{N} \tag{10}$$

where m is the index of the DFT output in the frequency domain having the values between 0, 1, 2, …, N-1; N is the number of input sequence samples and the number of frequency points in the DFT output,it is considered to be 128. The frequency spectrum of the DAC is shown in Fig. 5. It is observed that the dynamic performance of the implemented DAC meets the requirement of an 8-bit DAC as it shows the ENOB of 7.82 bits, SFDR of 56.25 dB and SNR of 48.84 at room temperature simulated with transient noise.

4.2. Radiation effects simulations

Out of the different simulation approaches available for evaluating the TID effects on the designed circuits, a method described in the basic literature [5] is partially followed for performing the simulations in this work and can be referred to for more details. In this work, a parameter that is affected by the TID effects is varied in the spectre model file (in .scs format) of the models available in the process design kit (PDK) directory. Cadence Virtuoso [20] software is used in this work to design the circuits. At first, open the design test-bench in Cadence and launch ADE (example: Explorer). In the ADE Explorer window toolbar go to Setup: Model libraries: Add model file. Then add the modified model file in .scs format and apply. The simulations are re-run with the modified model file and the results are compared with those from the pre-radiation simulations.

In SiGe HBT devices the most affected device parameter due to hot-carrier injection is the non-ideal component of the base current (iben) as given in (11) [21]. Since the device shows similar effects for ageing due to hot-carrier injection as well as TID, the iben parameter in the device model file of IHP SG13S technology is varied to simulate the DAC tolerance against TID [22].

$$I_{BE} = ibei \cdot (exp[V_{BE}/nei \cdot V_T] - 1) + iben \cdot (exp[V_{BE}/nen \cdot V_T] - 1) \tag{11}$$

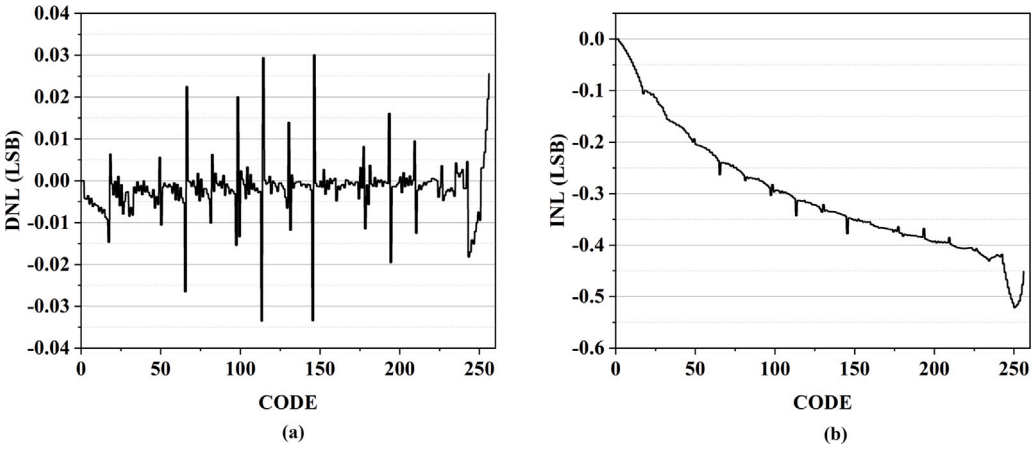

Fig. 4. (a) DNL, (b) INL of the initial DAC.

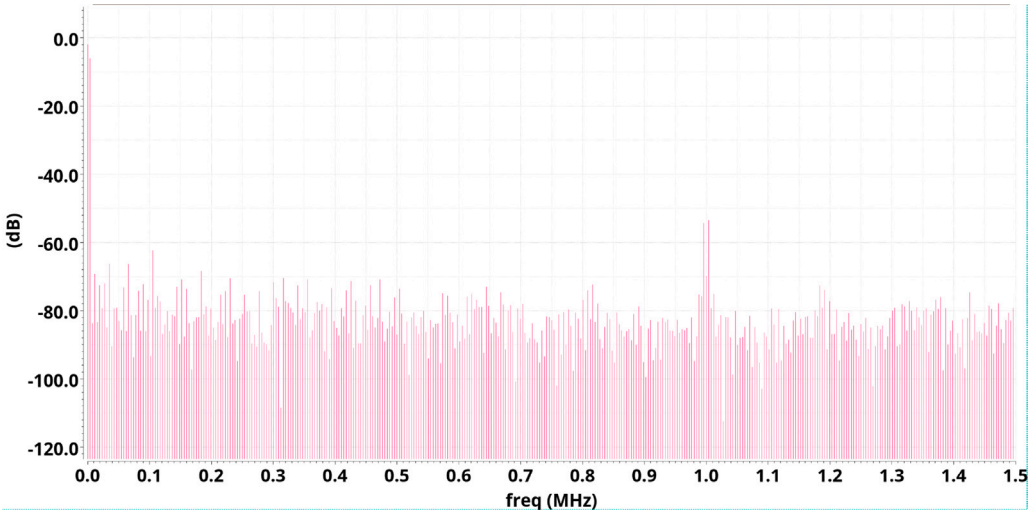

Fig. 5. DFT spectrum of the DAC output.

where, I_{BE} is the base-emitter (BE) saturation current, V_{BE} is the voltage across the base-emitter terminals, V_T is the thermal voltage, ibei is the ideal component of the base-emitter saturation current, iben is the non-ideal component of the base-emitter saturation current, nei and nen are the ideality factors.

Since one of the most affected parameters of the MOS transistors is its threshold voltage (V_{th}), it is mainly considered for the TID effect analysis. To modify V_{th} in the model file, doping concentration (N_a) of the Si available in the model file is varied according to (12) [13]. V_{th} is varied (δ V) between ± 100 mV from the nominal value (V_{th}) as for most applications the devices would become unusable when (δ V) approach the range of 50–100 mV [23].

$$V_{th} \propto \sqrt{N_a} \tag{12}$$

The SET-induced charge is emulated with the trapezoidal current pulse model. The current source is set according to the critical charge calculation using technology-dependent parameters for LET of 60 MeVcm^2/mg [5,24–26]. To evaluate the sensitivity of the DAC for the ASET effects, the performance of the DAC is analyzed, primarily observing variations in the DNL since it is generally assumed to be less than ±0.5 LSB, for a converter to have N-bit precision. Also, the DNL greater than −1 LSB indicates the non-monotonicity of the DAC. Therefore, considering these factors, any change in the DNL, resulting from the SET effect on the DAC devices, above ±0.5 LSB value results in the radiation intolerant-DAC and needs to be addressed by implementing SET mitigation techniques. The following chart shown in Fig. 6 presents an absolute maximum of the DNL of the DAC with auxiliary analog circuits when each device of different circuit blocks is hit by the charge individually. It is clear from this chart that the DAC core itself is resilient to SETs. That is, the digital part of the DAC containing switches and decoders is immune to DSETs, while the OpAmp constituting the analog part of the DAC shows negligible sensitivity to ASETs. However, the bandgap reference circuit providing the reference voltage for the DAC is the most sensitive part of the entire DAC circuitry, as the resulting DNL is 15.67 LSB, which is far away from the allowed DNL. This worst-case behavior is due to the fact that the long-lasting change in the bandgap reference voltage not only distorts the output signal for a longer duration but also, distorts the outputs from other circuit blocks that are dependent on the bandgap reference voltage [24]. Sensitivity of the circuits, providing V_{ref+} and V_{ref-} are negligible to ASETs as the DNL shows less change in its values for ASETs.

4.3. Radiation effects mitigation methods

It is observed from the SET simulation results, that the voltage regulator and the bandgap reference circuit are the most sensitive circuit blocks to ASETs. Therefore, mitigation techniques for these circuit blocks need to be implemented. As explained in [24], a capacitor of 3 pF is placed at the sensitive node of the LDO regulator circuit.

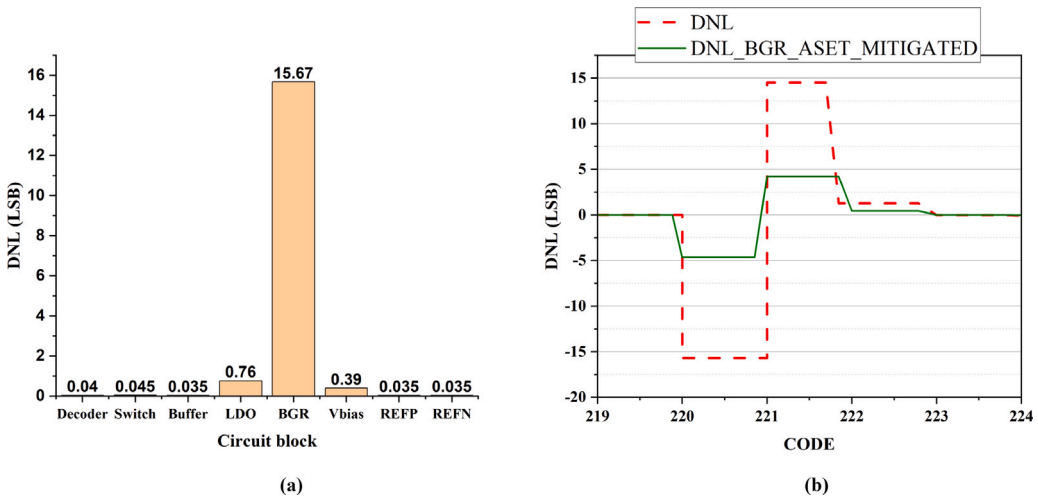

Fig. 6. (a)Simulated maximum absolute DNL of the DAC for ASETs at different circuit blocks of the DAC design, (b) DNL observed during post-radiation simulations with ASET occurring at the BGR circuit. The dashed curve represents the DNL when the original BGR circuit is hit by a particle, whereas the solid line shows the same with the BGR implementation with the analog redundant blocks to mitigate the ASET effects.

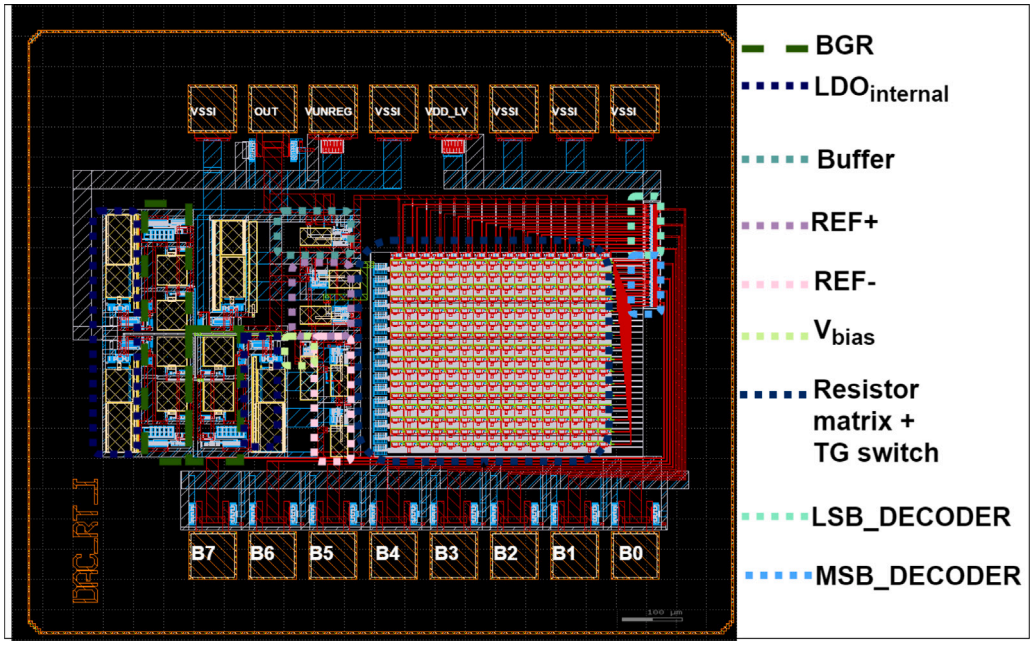

Fig. 7. Layout of the implemented radiation tolerant DAC.

Whereas, analog redundancy technique is implemented by placing 3 redundant BGR blocks in parallel since more than 3 instances are not practical to implement on-chip in terms of area requirements and power dissipation [24]. The emitter degenerative resistors with 200 Ω implemented at the emitters of the heterojunction bipolar transistors (HBT) placed at the DAC output buffer 2 reduce the sensitivity of the circuit to the rapid voltage transients due to internal negative feedback loop [27], thus shows less sensitivity to the ASET.

5. Discussion

The designed layout of the DAC with the capacitor at the sensitive nodes of the voltage regulator and analog redundant blocks of BGR is shown in Fig. 7. The implemented radiation tolerant DAC (RT-DAC) chip is 1.2 × 1.6 mm large and consumes 542.3 uA with 3.3 V supply. The layout is designed by following the standard DRC rule-set of the SG13S technology.

TID effects simulation results show negligible variation in DNL within 0.05 LSB for the DAC along with the auxiliary voltage references. Considering the characterized TID levels for both CMOS and HBT devices of SG13S technology and also observing from these simulation results, the design can be characterized as tolerant to TID levels 100 krad(Si) - 300 krad(Si).

The analog circuits of the DAC, consisting voltage divider circuit and a two-stage OpAmp with Miller compensation for the output buffer, show no or minimum sensitivity to SETs, simulated using a square pulse model. Similarly, logic circuits like switches and decoders of the X-Y addressing scheme constituting the digital part of the DAC can also be categorized as SET tolerant circuits. However, the auxiliary analog circuits are sensitive to ASETs.

The high-frequency transient current could be filtered in the following stage depending on the position of the charge incident node in an analog circuit, thus causing no effects on the concerned circuit, like the output buffer of the DAC. Whereas, if the connected circuit to the hit

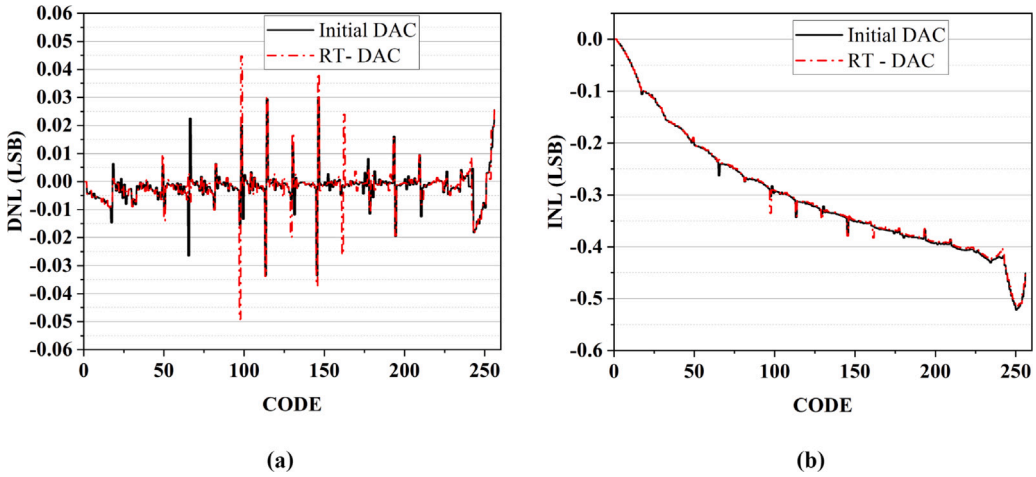

Fig. 8. (a) DNL, (b) INL of the initial DAC and radiation-tolerant (RT) DAC.

Table 8
Post-radiation simulation results of DNL.

Circuit block	$DNL_{no-mitigations}$	$DNL_{mitigations}$
LDO	0.76	0.43
BGR	15.67	4.6

node tends to increase the transient duration, it could potentially lead to undesired circuit behavior. This likely happens in high impedance nodes, where the excess charges hardly find a path to disappear towards the ground. Primary circuits like a reference circuit on which other circuits depend could be a critical sensitive circuit as the sensitivity of this circuit to ASET not only disturbs this particular circuit but also all the other circuits depending on it.

The designed layout of the DAC with the capacitor at the sensitive nodes of the voltage regulator and analog redundant blocks of BGR is shown in Fig. 7. Fig. 8 shows as expected that the performance of the radiation tolerant DAC (RT-DAC) is still similar to that of the original or initial DAC.

Table 8gives the simulated post-radiation DNL of the DAC implemented with the mitigation techniques.

Even though the sensitivity of the DAC to ASETs at the BGR circuit as shown in Fig. 6 is greatly reduced, efforts have to be made in the future to reduce the sensitivity of the BGR circuit by system-level mitigation techniques. Or, if the application allows for a larger area with higher power dissipation then adding an additional redundant block of the BGR circuit might reasonably reduce the sensitivity of the DAC to about 1 LSB.

6. Conclusion

Resistive string 8-bit DAC with X-Y addressing mode and shunt resistors in 130 nm IHP SG13S technology is designed. Radiation tolerance of the DAC is evaluated with SPICE simulations. The importance of evaluating the radiation tolerance of the concerned circuit block, like DAC in this work, by the vulnerability of the auxiliary analog circuits to ASETs is investigated. Critical circuits are addressed with the mitigation techniques.

CRediT authorship contribution statement

Aishwarya Harneer Suresh: Writing – original draft, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Gunter Fischer:** Supervision – Methodology, Investigation, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors are unable or have chosen not to specify which data has been used.

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