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Novel Backside IC preparation stopping on STI with full circuit functionality using Chemical Mechanical Polishing (CMP) with highly selective slurry

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Abstract

Mechanical sample preparation is a crucial and indispensable step in modern failure analysis (FA). Traditional methods excel in reducing bulk silicon to thicknesses of several tens of micrometers. However, contemporary demands necessitate sample preparation below 10 µm or even below 5 µm, which is challenging, time-consuming, and requires an expensive toolset and advanced operator expertise. Existing methods, which rely on mechanical components for bulk removal, induce mechanical stress and microcracks that can alter the electrical characteristics of the sample. Maintaining the sample's electrical behavior is essential for accurate FA.

This paper introduces a novel approach to sample preparation that employs concepts from wafer-level chemical mechanical polishing (CMP). This method ensures reliable sample preparation without introducing microcracks, accurately halts material removal at the shallow trench isolation (STI) – or deep STI - level, and maintains the sample's electrical functionality. The proposed approach is discussed in detail, including successful thinning of various sample types to the STI level, which were subsequently tested for electrical functionality.

Introduction

Mechanical sample preparation is a cornerstone in the field of modern failure analysis (FA), providing essential groundwork for accurate diagnostics and evaluation. Traditional sample preparation methods are proficient in reducing bulk silicon to thicknesses of several micrometers, a task that existing tools and techniques handle effectively. However, as FA techniques advance, the requirements for sample preparation have become more stringent. Modern applications demand sample preparation that achieves thicknesses below 10 µm or even 5 µm. This level of precision is challenging to attain, necessitating significant time, a comprehensive toolset, and advanced expertise from operators.

Current mechanical sample preparation methods inherently involve mechanical abrasives to remove bulk silicon, which introduces mechanical stress and microcracks into the sample. These microcracks can adversely affect the electrical characteristics of the sample, posing a significant issue in the FA process. Ensuring the electrical integrity of the sample is paramount, as any alteration can lead to inaccurate analysis and results.

The problem is further exacerbated with the increasing importance of novel FA techniques such as electron-beam (e-beam) probing [1,2] and visible light probing [3]. These techniques require extremely thinned bulk silicon, which in turn demands finer and more precise sample preparation. But also “mature” techniques based on near field optics e.g. SNOM (NSOM) or Atomic Force Microscopy (AFM) would benefit from a direct access to the transistor level. Short process windows as well as the presence of mechanical microcracks introduced by conventional methods hinders the effectiveness of these advanced probing techniques. Figure 1 shows a schematic drawing of existing FA techniques requiring direct access to the transistor level to be performed.

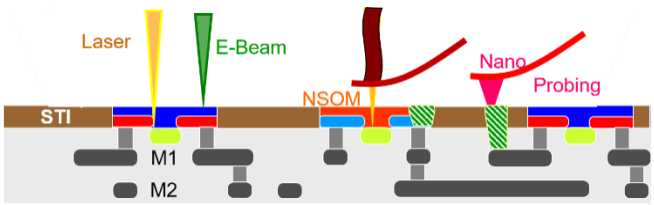


Figure 1: High resolution fault isolation techniques [4]

In response to these challenges, this paper presents a novel approach to sample preparation, leveraging the principles of wafer-level chemical mechanical polishing (CMP). This innovative method promises to eliminate microcracks, ensure reliable stopping at the STI level, and preserve the electrical functionality of the prepared sample. The subsequent sections of this paper will outline the methodology of this approach, provide detailed discussions on various types of samples successfully thinned to the STI level, and demonstrate the maintained electrical functionality through manual handling and testing.

In [4] a method to locally open small areas of a die while combining FIB trenching and CMP has been presented. This method can have good applications however, it is time

consuming and inflexible in terms of moving the area of interest.
The here proposed approach not only addresses the limitations of current methods but also sets a new standard for precision and reliability in mechanical sample preparation for modern failure analysis.

Sample Preparation Process

Sample Mounting
Parallel sample mounting and adjustment are critical steps in achieving full-area bulk silicon removal, particularly when using systems such as the Allied Multiprep or UltraTech UltraPol. Although this step is less crucial when thinning in cavities, such as with the Allied X-Prep or UltraTech ASAP-1, we would like to share recent internal improvements in the uniformity of full-area thinning.

The use of Fujifilm's Prescale measurement film, with a pressure range of 0.05 MPa – 0.20 MPa, has proven beneficial in enhancing the parallelism between the sample and the polishing pad. The process involves placing the pressure-sensitive film on the polishing pad and then dipping the sample onto the film. The color patterns produced by the film indicate the pressure distribution, allowing for precise adjustments to the sample holder. This process is repeated until an equally distributed color pattern is achieved, ensuring optimal parallelism. Figure 2 illustrates the resulting color patterns that guide the adjustment process.

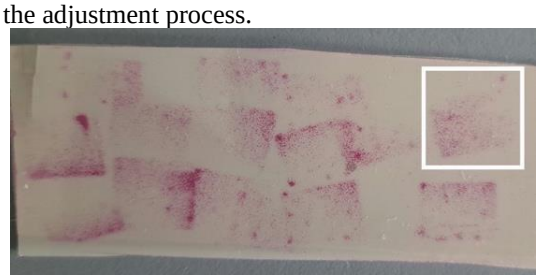


Figure 2: Used Fujifilm's Prescale; pressure marks for adjustment of parallelism between sample and pad. White frame shows optimum

Mass Bulk Removal
The initial step in the sample preparation process involves the removal of a significant portion of bulk silicon, which can range from 100µm to 800µm thickness, depending on the packaged chip. This bulk removal is achieved using a classical grinding approach that utilizes diamond lapping films or diamond plated tools when working in cavities. The goal is to reduce the silicon thickness to approximately 50 µm. This is accomplished by sequentially using grain sizes of 35 µm, 15 µm, and 6 µm for the bulk removal process.

An important consideration during this step is the sub-surface damage caused by the grinding process. As a rule of thumb, it is assumed that the sub-surface damage extends to three times the grain size used in the lapping film. This results in a sub-surface damage-free remaining bulk silicon thickness of 32 µm. This substantial safety margin is necessary due to the absence of an interferometer for precise thickness measurement. Instead, the thickness measurements are performed mechanically, ensuring a conservative approach to maintaining the integrity of the remaining silicon.

Accurate Sample CMP Thinning
Subsequently to the mass bulk removal, CMP is used for polishing using an IC1000™ perforated pad and different CMP slurries e.g. the SS12™ slurry. While standard CMP slurries consist of a mixture of nano-abrasives and chemical additives, abrasive-free slurries have been developed with high Si removal rates [5]. By adding cationic and nonionic polymer additives into basic solutions, predominantly Si is removed, while nearly no attack of SiO_2 can be observed [6]. An experimental, not yet commercially available, realizes a highly selective (HS) Si to SiO_2 removal (>500:1) while being abrasive free. This slurry, representing the final polishing step, is utilized to realize a reliable stop of material removal at STI level.
For a reference area of 5 mm², a first iteration of process optimization, has determined material removal rates of 0.7 µm / min for the SS12™ slurry and 0.4 µm / min for the HS-Slurry.

This results in an overall process time of 2h to 3h, starting from sample mounting to a full area removed bulk silicon.

Sample Description

The open-source nature of the IHP 130nm process [7] facilitates a transparent review of test structures and process characteristics. This transparency allows verification that the STI thickness is 400 nm and the BEOL has a total thickness of approximately 15 µm. The doping profiles extend deeper than the STI region, particularly the deep n-well associated with the bipolar transistor. A schematic drawing of the layer properties is shown in Figure 3.
This open behavior makes test structures from this process ideal candidates for scientific research in various fields, such as chip design, education for failure analysis, or process development.
The samples used in this study were sourced from the IHP BiCMOS 130 nm process, and the test structures analyzed are process control monitoring (PCM) structures. These PCM structures encompass a variety of test cases, both passive and active, allowing for comprehensive analysis of the sample preparation process.

Passive Test Structures
The passive test structures consist of components such as resistors and capacitors. These structures serve as a baseline to evaluate the mechanical integrity of the samples post-preparation.

Active Test Structures
The active test structures include single bipolar transistors, bipolar transistor-based ring oscillators, and single MOS devices. The functionality of these active structures is crucial for evaluating the sample preparation process, as they provide

insight into the electrical characteristics and potential impacts of the preparation methods.

In summary, the diverse range and open-source characteristics of test structures available from the IHP BiCMOS 130nm process provide a robust platform for evaluating the efficacy of the sample preparation process. There is a particular focus on the challenges associated with maintaining the functionality of bipolar devices in extremely thinned samples.

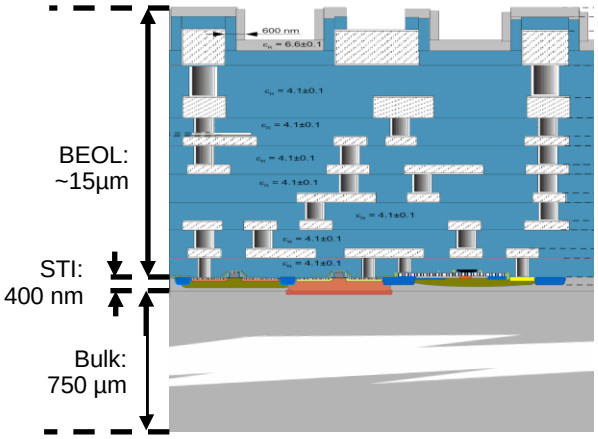


Figure 3: Schematic IC cross section of the IHP BiCMOS process [7].

Process Verification

This chapter deals with the mechanical and electrical process verification.

Mechanical Integrity

Ensuring mechanical integrity is paramount in the sample preparation process, particularly when targeting the shallow trench isolation (STI) level. A detailed discussion on achieving a reliable stop at the STI level, supported by e-beam images, is carried out in [8]. For routine verification, we rely on optical inspections. Thanks to precise parallel sample mounting (see Figure 2), the entire chip area of approximately 1 cm² has the STI exposed. As shown in Figure 4, only a minor veil of silicon remains in the middle area. Detailed microscopic analysis of a ring oscillator (Figure 5), prepared for electrical measurement, reveals that the device level is fully exposed, with no mechanical cracks or other irregularities.

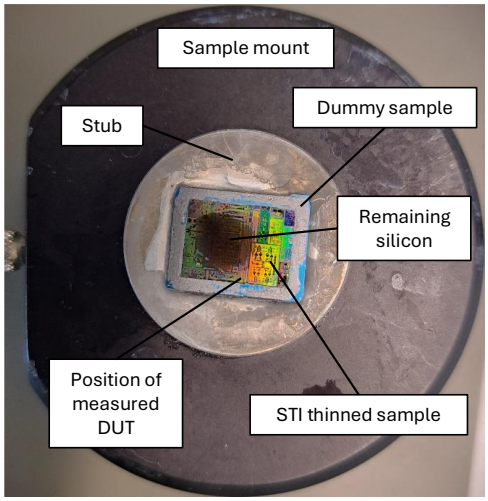


Figure 4: Overview image of the STI thinned sample, sample stub holder and sample mount. Picture taken before sample release.

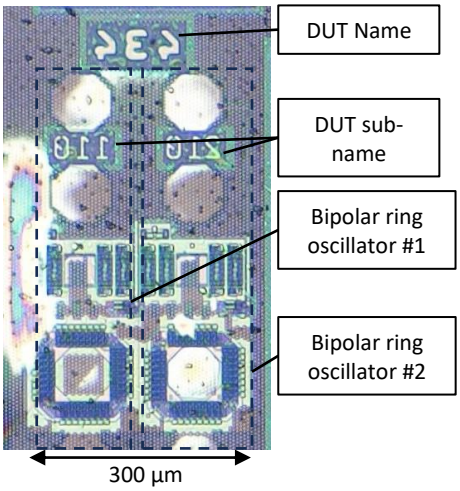


Figure 5: Full removal of the backside silicon allows to directly look at the device level, using an optical microscope.

The chip is front-side mounted and only 15 µm thick. To measure or bond the device, it must be released, turned around, and mounted on a new substrate. Maintaining mechanical integrity during this process is crucial. The release process was performed in an acetone bath, followed by manual handling, which demonstrated good mechanical stability. An optical front-side image of the released die on a filter paper is shown in Figure 6.

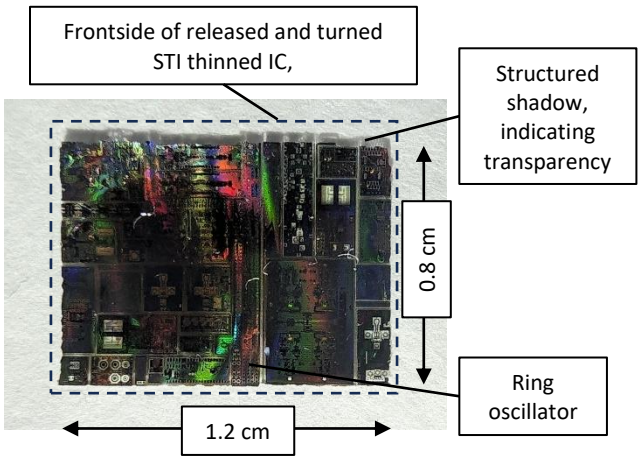


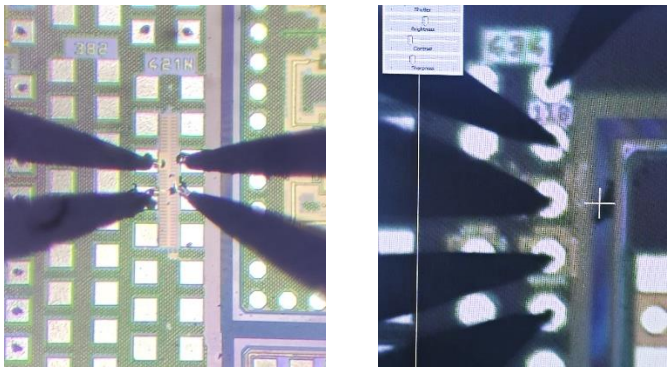
Figure 6:Front side image of an STI chip that has been release and placed on a filter paper. Total remaining thickness of the shown chip is approximately 15 µm.

For electrical measurements on a needle prober, the 15 µm thick sample requires a die carrier. A blank silicon wafer was used for this purpose. Two mounting options were evaluated: mounting wax and DI water using capillary force. Both methods provided good mechanical stability, but the wax induced thermal problems, which will be discussed in the next chapter.

Electrical Verification

Electrical verification of the prepared samples involved measuring the functionality of various test structures, including resistors, capacitors, bipolar transistors, and ring oscillators. The primary focus was on maintaining the electrical characteristics of the bipolar devices, which are more challenging to preserve due to higher power consumption (thermal load) and the presence of deep n-well doping.

In this paper we present two measurements in detail. Single BiPo transistors and BiPo based ring oscillator. Probing images of both structures can be seen in Figure 7. From a probing point of view there is no difference in contacting these extreme thinned samples.



(a) (b)

Figure 7: Needle probed test structures after STI thinning: (a) single transistors; (b) ring oscillators.

Single Transistor Characteristics:

Single transistor characteristics before and after thinning are shown in Figure 8. The overall functionality is maintained, although characteristics are altered post-thinning. Two effects are observed: an increasing early factor for increasing base currents and a reduced overall collector current, which aligns with the reduced collector well volume. No significant difference in electrical characteristics was observed for different mounting methods.

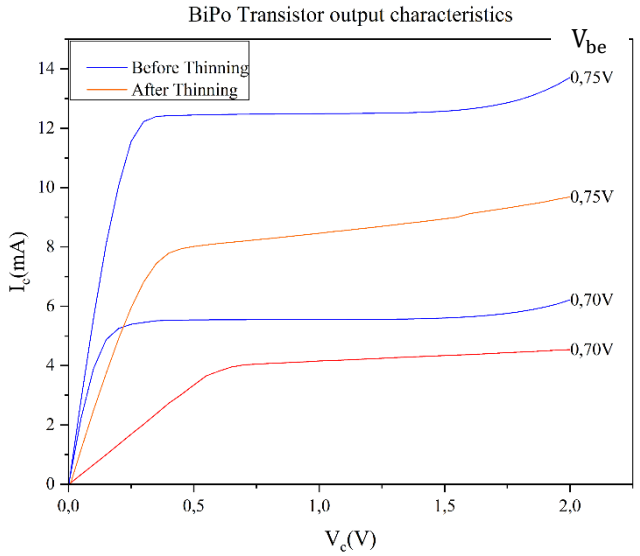
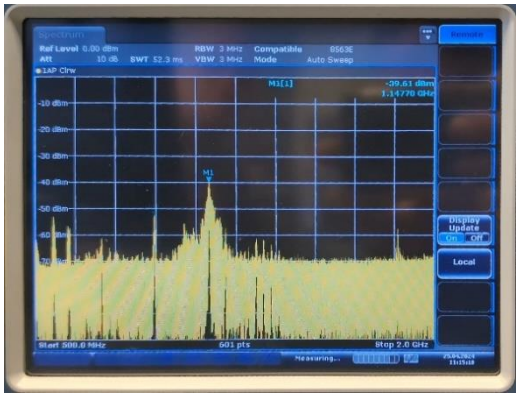


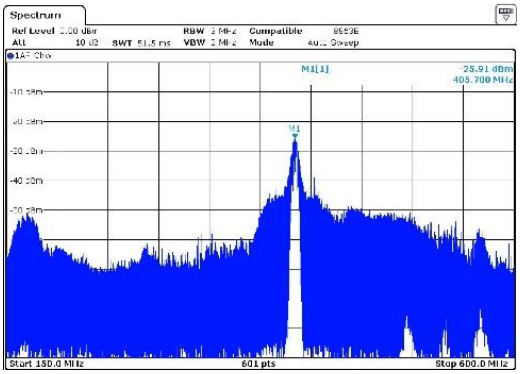
Figure 8: Output characteristics of a single bipolar transistor before thinning and after thinning to STI level.

Ring Oscillator Probing:

Significant differences in electrical characteristics were observed for ring oscillators with different mounting methods. The thermal properties of the ring oscillators are foreseeable more challenging compared to single transistors. In normal operation the power consumption is 325 mW on an area of 0.04 mm² Wax mounting showed good oscillation frequency greater than 1 GHz. However, due to the high power consumption, the resulting heat destroyed the measured structure during the measurement sweep. Figure 9a is an extracted frame from a video captured during the measurement sweep, showing the oscillation frequency. In contrast, mounting the STI level thinned sample with Di-Water on a carrier wafer, allows a continuous operation of the ring oscillator. However, the oscillation frequency is reduced, most likely due to electrically non isolating volume coupling to the device level. The corresponding measurement can be seen in Figure 9b.



(a)



(b)

Figure 9: Measured oscillation frequency of STI thinned bipolar ring oscillators: (a) for a way mounted device (b) for a Di-Water mounted device

Thermal Considerations:
Mounting wax has low thermal conductivity as a consequence, the generated heat cannot be transported away sufficiently from the device level. In contrast, mounting with DI water offers good thermal connection to the carrier wafer, allowing continuous oscillation frequency measurement.

In summary, the process verification confirmed that the sample preparation methodology successfully maintains both the mechanical integrity and electrical functionality of the devices. The precise parallel sample mounting and careful handling during the release process were key factors in achieving reliable results. The differences in mounting methods highlight the importance of thermal management in preserving the functionality more power demanding devices.

Conclusion

The sample preparation process initially presented a year ago [8,9] has now undergone extensive mechanical and electrical verification, demonstrating its robustness and reliability. The current study confirms that the entire sample can be effectively thinned to the STI level within 2.5 hours, with potential improvements poised to reduce this time to approximately 1.5 hours. Once the process parameters are properly established, the method exhibits a high success rate, with minimal sample loss observed during the preparation process. This high success rate is a significant achievement, as it not only ensures the mechanical and electrical integrity of the samples but also reduces the risk of mechanical damage during over-polishing to zero, even for applications requiring a remaining silicon thickness.

The robustness and reliability of the established approach and procedure underscore its suitability for routine application in semiconductor failure analysis. This study focuses on full die thinning, but the basic functionality of the described approach has also been successfully tested on milling-based tools such as the Ultratech ASAP-1 and Allied X-prep. However, further process development and characterization are planned to fully validate these techniques.

The study has proven that thermal budgeting is a key aspect when aiming for a full bulk removal. While single transistors can be operated without additional cooling measures, more power-demanding blocks require careful cooling. This issue was addressed by using a blank silicon wafer to ensure a good thermal connection to the sample.

In summary, the verification of the sample preparation process highlights its efficacy in maintaining mechanical and electrical integrity, ensuring reliable results in semiconductor failure analysis. The demonstrated improvements in efficiency and success rate offer significant advancements in the field, promising a robust and efficient approach to sample preparation. The ongoing development and validation of milling-based techniques and novel cooling solutions will further enhance the utility and impact of this methodology.

Outlook

The findings presented in this paper underscore the importance of further exploration in several key areas to enhance the effectiveness and applicability of the sample preparation process. The future directions for this research will focus on detailed evaluations of electrical performance, innovative cooling concepts, process improvements and the thermal limitations associated with device testing.

A more comprehensive evaluation of the electrical performance of thinned samples will be critical to further prove the usability of the presented approach for novel FA requirements.

Effective thermal management remains a significant challenge, particularly as devices under test (DUTs) continue to generate increasing amounts of heat due to the demands of AI and advanced computing applications. Two promising approaches to thermal management are currently being explored: global cooling with systems like the SEMICAPS AuriCool and localized cooling using the Aplanatic Refractive Solid Immersion Lenses (ARSIL).

The SEMICAPS AuriCool system offers a global cooling solution that has demonstrated strong thermal management capabilities. This method uses an array of contact elements thermally coupled to a cooling fluid, with a flexible heat conductive sheet positioned between the contact elements and the DUT surface. This configuration efficiently transfers heat from the semiconductor device to the cooling fluid. The AuriCool has proven capable of removing up to 200W of heat flux on a 20 mm x20 mm die, and ongoing developments aim to further enhance its thermal performance and surface conformity across a variety of applications.

In contrast, the localized cooling approach focuses on the use of ARSIL, which is typically employed for its enhanced optical resolution. The ARSIL lens, with a numerical aperture (NA) of 3.3, can resolve features at the 3 nm technology node, achieving < 150 nm pitch resolution. Interestingly, the ARSIL also contributes to localized cooling when in physical contact with the DUT.

As the demands of AI and advanced computing continue to escalate, the need for reliable and high-resolution FA becomes increasingly critical. Therefor a reliable sample preparation that allows the incorporation high resolution FA techniques as well as sustainable thermal management concepts are highly in demand. A combination of ARSIL, global cooling (AuriCool) and the here presented sample preparation approach seems promising to meet current and future needs for device FA.

In conclusion, the ongoing development of thermal management strategies, coupled with a deeper understanding of the electrical impacts of sample thinning, will be essential in advancing the field of semiconductor failure analysis. These efforts will not only improve the reliability of FA techniques but also support the continued evolution of electronic devices in increasingly demanding applications.

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