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Reliable backside IC preparation down to STI level using Chemical Mechanical Polishing (CMP) with highly selective slurry

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Abstract

When aiming for extreme thinning of the bulk silicon down to the shallow trench isolation (STI) level, endpoint determination is a challenging task. Here, we present a novel approach providing reliable access to the STI level of single dies. Therefore, we transfer the wafer-based CMP process to be applicable to single dies on a table-top machine. In a first step, the developed process is applied to the whole IC backside simultaneously. Using a highly selective slurry with a material removal ratio from Si to SiO of more than 500:1 ensures that the STI level remains intact. Two types of samples have been prepared for experiments performed for this paper. A 115mm x 80mm flip-chip bonded device with a bulk silicon thickness of 500µm has been prepared to STI level within less than 4 hours.

Introduction

First silicon debug and other processes of integrated circuit (IC) product development and failure analysis require contactless fault isolation techniques with optical interaction through the chip backside. Over the past 20 years, these techniques have been proven to be based on near infra-red optics, keeping silicon transparent over the entire backside of the chip. However, the achievable resolution of an optical system is strongly related to the wavelength used to visualise the point of interest (POI) [1]. Miniaturization to single nm nodes requires shorter wavelengths to still be able to achieve adequate resolution. The use of visible light potentially allows further improvement of the achievable resolution, especially when combined with a GaP Solid Immersion Lens (SIL) [2]. On the other hand, the backside silicon of an IC shows a strong absorption for visible light. For example, visible light with a wavelength of 550nm results in a penetration depth of ~1µm [3]. This means that the remaining silicon thickness must not exceed 1µm in order to transmit significant signal intensity. Realising a reliable process stop with this minimal margin is a very challenging task.

State of the art

Conventional sample preparation methods are based on point shaped tools which are used to trench local slots into packed ICs similar to a milling cutter. Figure 1 shows such a packed and mechanically prepared IC.
The IC itself must then be thinned within this package opening. Famous tools such as the Ultratech ASAP-1 have been utilised to perform such jobs [3]. These tools are mainly based on the use of abrasive materials that drive the material removal of the backside silicon. Endpoint detection must be performed by measuring the remaining bulk silicon thickness. While this approach is still suitable for a wide range of applications, the mechanical stress to the sample, due to the milling tool, causes problems. Developments in processes and tools have made this method much more advanced. New tools, featuring a built-in IR light source being used to continuously measure the remaining silicon thickness. This approach allows to reduce the bulk silicon thickness to 1-5µm [4].

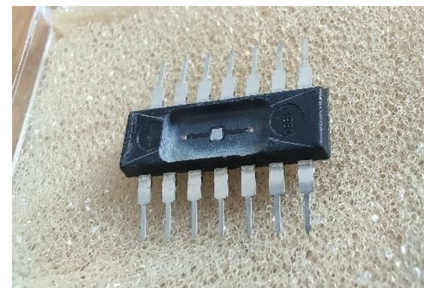

Figure 1: Opened Dual Inline Package (DIP) to access the chip backside. Further processing would remove the back side silicon.

Another problem that has evolved and is being addressed is related to IC size and new IC packaging methods. Larger ICs in particular are often subject to non-trivial mechanical bending after the packaging process. The shrinking characteristics of the packaging material are a driving factor in this issue. IC heating can be used to relieve stresses during the decapsulation and silicon thinning process, and in combination with 3D curvature correction techniques, bending can be compensated to a certain degree. Still, uniform endpoint detection is challenging. In [5], a resistivity-based endpoint detection method using conductive

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tips on prepared pockets was presented. With this approach, a silicon thickness of >2µm is targeted.
In addition to mechanical removal of the backside silicon, laser-based thermal removal has also become established in recent years. However, endpoint detection at STI is still a challenging task [4].
Concluding, the removal of the backside silicon has been subject of innovation for many years. However, new technology nodes require reliable extreme thinning of backside silicon down to STI level in order to use modern analysis such as e-beam probing [5]. The techniques and endpoint methods available are not capable to fulfil this requirement.

Chemical mechanical polishing

Our work shows that chemical-mechanical polishing (CMP), which was a key enabler for IC fabrication, enables reliable thinning of backside silicon down to STI level. This chapter provides a brief overview about CMP [6].
Chemical mechanical polishing (CMP) is a crucial technique used in the semiconductor industry to planarize and smooth the surfaces of silicon wafers during the fabrication of integrated circuits (ICs). It is a precise and controlled process that simultaneously applies chemical and mechanical forces to remove imperfections and achieve a flat and uniform surface.
CMP is an essential step in semiconductor manufacturing as it enables the creation of multiple layers of complex circuitry. In this process, a wafer is pressed against a rotating polishing pad while a slurry containing abrasive particles and chemical agents is applied. The mechanical action of the polishing pad and the chemical reactions in the slurry work together to remove peaks and even out the surface. This polishing technique is crucial in minimizing the depth of interconnects and creating a smooth surface for subsequent lithography, deposition, and etching processes. It helps ensure proper alignment, improve electrical performance, and enhance yield rates in IC production. CMP involves careful control of parameters such as pressure, pad material, slurry composition, and process time to achieve desired results. The process is highly automated and monitored using advanced metrology techniques to ensure consistent polishing quality across large batches of wafers.
In summary, CMP is a fundamental process in semiconductor manufacturing to achieve planarity and smoothness of silicon wafers. It plays a vital role in the production of advanced integrated circuits with multiple layers of intricate circuitry.

Sample description

To develop the thinning method presented here, we used several dedicated process development samples consisting of a simplified three material layer stack of aluminum, silicon oxide and silicon. However, the process development is outside the scope of this paper. More information can be read in [9]. The process then developed was evaluated on two kinds of samples.

A. 130nm BiCMOS bare die sample

As the first test vehicle we had chosen a chip from a fully open documented process, the IHP 130nm BiCMOS process [7]. This is a process with seven metal layers, corresponding to a BEOL thickness of ~15 µm and a STI thickness of 400nm (Figure 2).

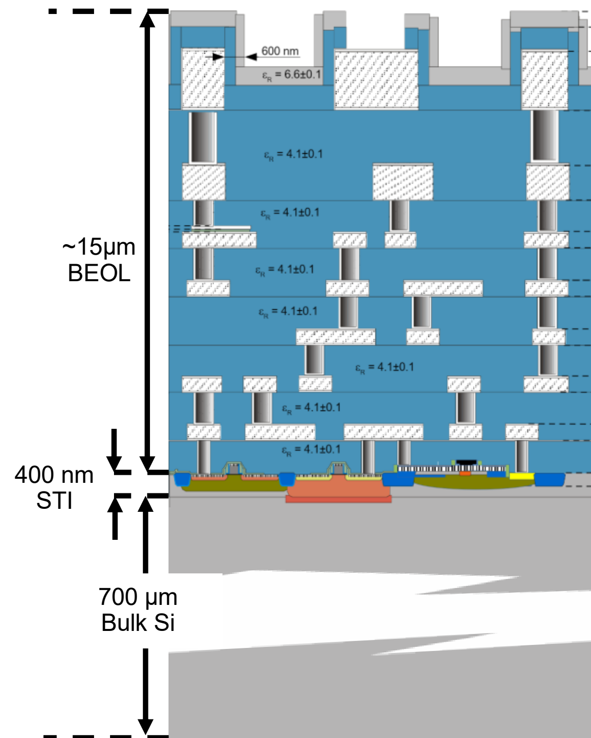

Figure 2: Schematic layer stack of IHP Open Source PDK, containing layer thicknesses [7]

Using a bare die has the advantage that no package material is required and, as we will show later, to mechanical bending from any bonding/packaging process occurs. On the other hand, a bare die requires a spacer to increase the distance between the sample holder and the device under preparation. A standard mounting wax is used to mount both dies. The thickness of the wax film was determined to be approximately 20µm. Even though the mounting has been performed with extraordinary caution, the parallelism between the silicon and the grinding/polishing pad can only be maintained to a certain level. (Figure 3).

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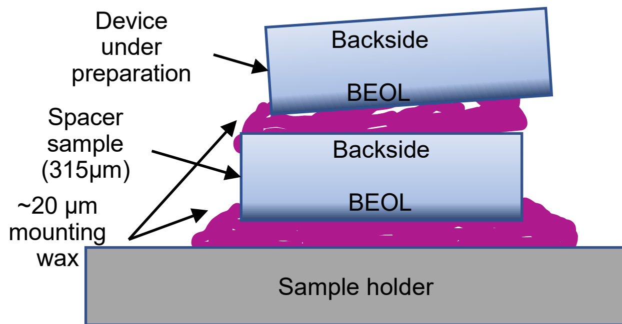

Figure 3: Schematic drawing of bare die mounting with additional spacer die to increase the distance to the sample holder; multiple reasons can cause non-parallelism

Finally, five specimens were mounted on the larger specimen holder to maintain good edge retention. (Figure 4)

Figure 4: Mounting of ten bare dies in a geometrically stable arrangement. The outer chips serve as dummy chips to protect the die in the centre

B. Sub50nm flip chip mounted processor

The second type of samples, to which we applied the developed backside thinning method was a commercially available processor chip flip-chip bonded to a PCB carrier board. First, we had to remove the capacitors soldered to the board. Then, using mounting wax, the PCB was mounted on the parallel polishing fixture already shown in Figure 5. Mechanical measurements of the die thickness had revealed a convex curvature of the chip's backside silicon of 25µm.

Figure 5: Flip-Chip mounted sub 50nm device mounted; carrier PCB mounted on a customised sample holder for the Allied Multiprep; Protective blocking capacitors not yet removed.

Novel thinning approach and process planning

A reliable stop of backside silicon removal at STI level can only be achieved by a process that selectively removes silicon from silicon oxide. For the last decades, the development and improvement of CMP processes has been driven by the semiconductor manufacturing. So far, extremely high material removal selectivity was not a major driving force, as due to process parameter, tool and cost optimisation low selectivity has proven well in mass production. Thus, the widely adopted CMP slurry SS12(SS25) enables selective removal of silicon at a rate of max 3:1 compared to silicon oxide. Novel and experimental CMP slurries from the company "resonac" (former Showa Denko) allow a highly selective removal of silicon from silicon oxide with a selectivity higher >200:1. However, a disadvantage of the CMP process compared to classical grinding is the comparatively low material removal rate (MRR). Therefore, a process combination of grinding, classical CMP slurries and highly selective slurries was developed to achieve the goal of highly reliability chip tinning down to STI level. A detailed process plan is necessary to ensure that grinding-related sub-surface damage does not propagate into the STI region. The sub-surface damage of mechanically grinded silicon can influence the mechanical stability or, if it propagates into the active region, the electrical characteristics of a die. A detailed study on the measurement of sub-surface damage is given in [8]. However, a commonly applied rule indicates the sub-surface damage to be less than three times the grainsize of the abrasive material used. According to this rule, a process plan for a 300µm bulk silicon chip is given in Table 1.

Process Step	Initial Thickness (µm)	Target Thickness (µm)	Sub-Surface Damage (µm)
Grinding with a 35 µm grainsize foil	300	200	105
Grinding with a 15 µm grainsize foil	200	95	45
Grinding with a 6 µm grainsize foil	95	50	18
CMP with SS12	50	30	Minor
CMP with SS12 + HS slurry (Optional)	30	18	Minor
CMP with HS slurry	18	STI	-

Table 1: Process plan for thinning a 300µm Bulk silicon sample to STI level; HS stands for highly selective.

While the MRR of a foil-based grinding process is highly dependent on the wear condition of the foil, the resulting MRR is not deterministic. However, it is possible to abrade several tens of microns within minutes. At this stage, an inline mechanical gauge is sufficient to monitor the thinning process. For the prepared samples, we decided to stop at a measured bulk thickness of 50 µm and an estimated sub-surface damage of 18 µm – with an expected undamaged bulk thickness of 32 µm.

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The inaccuracy of mechanical measurement tools as well as the uncertainty of the mounting wax and BEOL thickness require a higher safety margin – in this case we decided to have a safety margin of 32 µm. A non-selective CMP based process using the SS12 slurry is used to remove the sub-surface damage. With this slurry, we achieved material removal rates of 0.87µm / min. At this point, the remaining bulk silicon thickness must be determined using optical measurement tools such as reflectometer, NIR LSM, and interferometer. Finally, highly selective slurry can be used to remove the remaining few µm of bulk silicon. However, if the chip was stored in air for several hours, the native oxide must be removed by a short pulse of SS12 polishing.

At last, after initial optimization of the process parameters, the highly selective slurry can achieve an MRR of 0.34µm / min. During process development, we identified a ten-minute process cycle as a good working point to regularly monitor the remaining thickness. A more detailed description of the parameter optimization process can be found in [9].

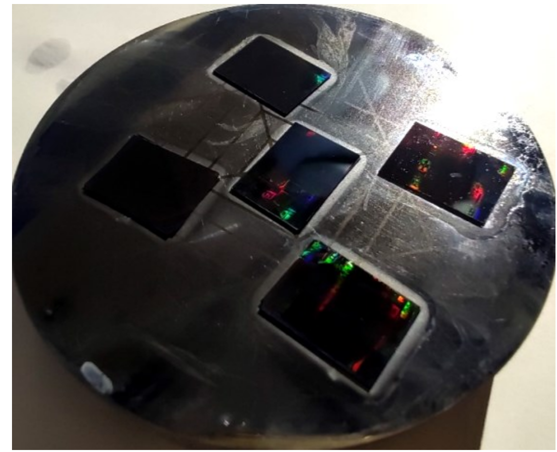
Results

A. Bare die STI thinning

A sample that is thinned to STI level reveals its structured STI layer, which than can be optically inspected, similar to the chips frontside.

Figure 6a shows and overview image of the nearly to STI thinned samples illustrated in Figure 4. It can be seen that all five sample stacks partially reveal their structured STI level. A more detailed optical evaluation, shown in Figure 6b, makes clear that the fully backside silicon removal evolves from individual edges of the singles, thus the samples are individually tilted as sketched in Figure 3.

A tilted sample is incorporated with the fact that the area which is initially exposed has to face the upcoming CMP thinning cycles and hold its structures. Figure 7a and b shows the evolving STI revealed area after ten additional minutes of CMP thinning with the highly selective slurry. Within ten minutes ~ 4 µm of silicon have been removed and as it is proven in Figure 7c the firstly revealed corner of the chip is still maintaining its 400nm thick STI structures.



(a)

(b)

Figure 6: (a) Overview of an optical analysis of samples shown in Figure 4 after thinning them to STI level. (b) Enlarged image visualises the already STI thinned area as silver reflecting; area with remaining silicon is reflecting in brown – but already transparent for visible light

A feature of the developed process is the perfect edge retention. During the whole process we did not found a single edge breaking off nor we found cracks in the remaining silicon. Exemplarily, Figure 8 shows a microscope image of the fully STI thinned corner section. As it can be seen the edges are fully intact. Furthermore, the alignment of the spacer sample to the device under preparation (Figure 2) was inaccurate, leaving an overhang of the top die. After the STI thinning process, the overhang comprises only FEOL and BEOL layers. According to Figure 2 this stack is ~15 µm and as is can be seen in Figure 8 the overhang is mechanically fully intact.

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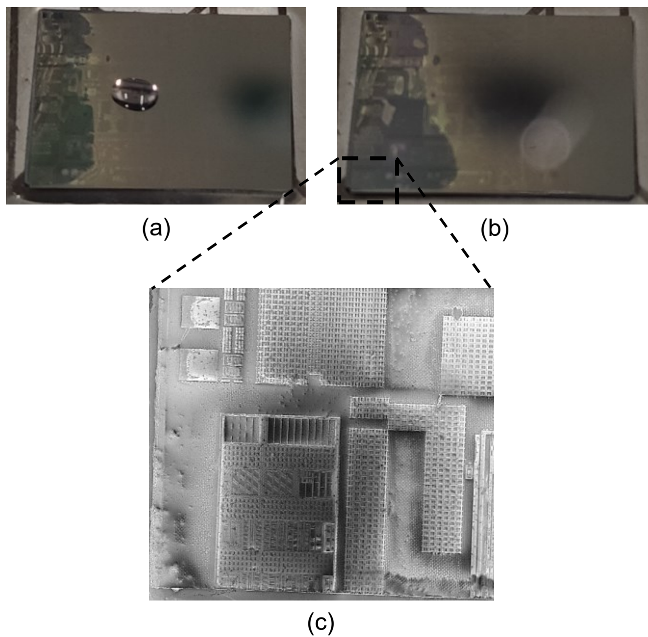

Figure 7: (a) and (b) showing optical analysis of the same bare die during two steps of the fully backside removal process. (b) shows additionally exposed area after ten more minutes of highly selective CMP thinning; (c) shows a REM image of the still intact STI structuring

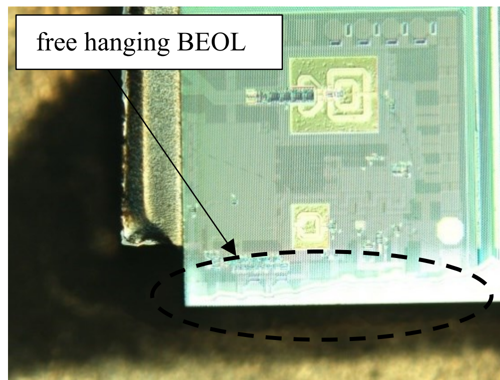

Figure 8: Good edge retention; the 15µm BEOL stack is free hanging and not damaged as it is exposed to the CMP process

B. Flip Chip STI thinning

The flip chip mounted, sub 50nm node processed, IC features an initial backside silicon thickness of 500 µm. A process plan similar to Table 1 has been written to plan the thinning process ahead. The only difference is that the 35µm grinding foil step was extended.

The processing went straight ahead such that the centre of the device revealed its STI region after only three hours of work, this includes planning, mounting and regular checks. Figure 9 shows that the thinning process evolves circular from the centre of the device. This observation goes hand in hand with the convex curvature determined earlier. Unfortunately, further polishing steps with the highly selective CMP slurry could not propagate the STI exposed area, leaving a circular area with a diameter of ~1mm revealed. A first assumption is that the stiff polishing cloth used could not overcome the ICs convex bending of 20 µm.

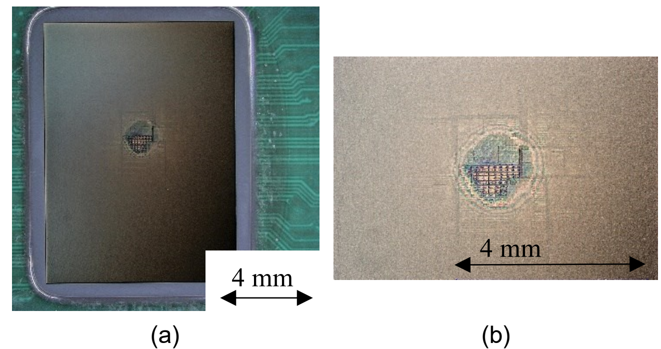

Figure 9: Flip-chip mounted commercial sub 50nm chip thinned down to STI level within less than 4 hours processing

Conclusion

The CMP assisted sample preparation process developed and presented here enables a reliable thinning of the IC backside with a highly selective process stop on STI level. Another novel aspect is the uniform thinning of the whole chip backside at once. However, this can also be seen as a limitation. In a first approach, the presented process requires that the IC is flip chip bonded, specialised packages have been utilised or initially not packaged at all. It has been proven that the presented approach can compensate non-parallel polishing as well as mechanical strain on the chip backside. This is due the highly selective MRR characteristics of the utilised CMP slurry. Finally, the presented process is comparable fast and generated a smooth and homogeneous surface which is ready for the use of solid immersion lenses, to further increase the numerical aperture. An even higher resolution would be archived using e-beam probing [5].

Even though the process capabilities have been demonstrated on a mature 130 nm node as well as on an advanced sub 50 nm node, further process development should be carried out to learn about the influence of polishing pad characteristics, possibilities to compensate for IC bending/tilting. On a next step it should be evaluated how the globally extreme thinning of the bulk silicon influences the electrical performance of the device.

Acknowledgment

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The developed procedure is applied for patent.

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