Frank Herzel*, Thomas Mausolf and Gunter Fischer

A Novel architecture for low-jitter multi-GHz frequency synthesis

https://doi.org/10.1515/freq-2021-0188
Received August 9, 2021; accepted January 13, 2022;
published online February 16, 2022

Abstract: A phase-locked loop (PLL) cascade driven by a crystal oscillator and a free running dielectric resonator oscillator (DRO) is proposed. For minimizing phase noise, spurious tones and jitter, a programmable PLL1 in the lower GHz range is used to drive a millimeter-wave (mmW) PLL2 with a fixed frequency multiplication factor. The phase noise analysis results in two optimum bandwidths of the two PLLs for the lowest output jitter of the cascade. Phase noise and spurious tones (spurs) in PLL1 are further reduced by dividing the output frequency of PLL1 and up-converting it by means of a single-sideband (SSB) mixer driven by the DRO. By including the SSB mixer in the feedback loop of PLL1 manual tuning of the DRO is avoided, and a low-noise free running DRO can be employed. An exemplary design in SiGe BiCMOS technology is presented.

Keywords: dielectric resonator oscillator; frequency synthesizer; low-jitter clock; phase noise; phase-locked loop.

1 Introduction

Phase noise and jitter of PLLs are critical in communication systems and data converters [1]. Jitter describes the deviation of the zero-crossings of the output signal from the expected points in time, whereas phase noise (PN) is the corresponding frequency-domain equivalent. Minimization of jitter implies a minimization of the PN spectrum and spurs. This is important for high-speed wireline transceivers, wireless transceivers in 5G radios, and high-speed, high-resolution analog-to-digital converters (ADCs).

Integrated millimeter-wave (mmW) frequency synthesizers usually employ a voltage-controlled oscillator (VCO) embedded in a PLL to stabilize its output frequency by using a spectrally pure low-frequency input signal with a frequency f_{in}. The PLL output frequency, f_{out}, is larger by a factor $M(N+\alpha)$, where M is the prescaler division ratio (typically 2 or 4), N is the integer part of the programmable divider ratio, and α is its fractional part, where $0 \le \alpha < 1$. The PN of mmW VCOs is typically quite high, mainly due to the low Q-factor of the integrated variable capacitor (varactor). In order to reduce VCO PN and in-band PN, a high f_{in} and a large loop bandwidth, f_L, are usually mandatory. Since in an integer-N PLL the spacing of the output frequencies is as large as Mf_{in}, a fractional-N PLL ($\alpha > 0$) is often required for programming f_{out}. Here, the in-band PN and in-band spurs may become excessive for small α, especially, for a large f_L [2]. Unfortunately, a large f_L is required for VCO noise suppression. Therefore, a simple fractional-N PLL is not capable of combining efficient VCO PN suppression with a low level of in-band noise. If a low-frequency PLL1 with a low-noise VCO is available, it can be used to drive a mmW PLL, named PLL2 in this paper. In order to save DC power, the feedback divider ratio in PLL2 should have a simple value, preferably a power of two. The loop bandwidth of PLL1, $f_{L,1}$, should be much smaller than the loop bandwidth of PLL2, $f_{L,2}$. In such a PLL cascade, a relatively low level of in-band PN and spurs can be combined with a significant reduction of the VCO PN in PLL2 [3]. PLL cascades are especially useful in phased-array systems, where a common reference signal in a few-gigahertz range is distributed to a set of local mmW PLLs located at each antenna element [4].

Further reduction of the output jitter requires a high-Q device in PLL1 in addition to the crystal oscillator. For achieving a low phase noise in the kHz offset region of the phase noise spectrum, opto-electronic oscillators (OEO) and DROs are promising [5]. A DRO is based on ceramic material to function as a resonator for radio waves, generally in the microwave bands. The unloaded Q factor of the resonator is typically on the order of 10000s. As a result, the PN of DROs is much lower than that of PLL-based frequency synthesizers. In [6] a 19 GHz DRO was used to down-convert a radar signal around 18 GHz to a frequency of about 1 GHz for use in a 77 GHz automotive radar frontend. Unfortunately, the thermal stability of the DRO frequency is much worse than for a crystal oscillator,

***Corresponding author: Frank Herzel**, IHP - Leibniz-Institut für innovative Mikroelektronik, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany, E-mail: herzel@ihp-microelectronics.com
Thomas Mausolf and Gunter Fischer, IHP - Leibniz-Institut für innovative Mikroelektronik, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

Open Access. © 2022 Frank Herzel et al., published by De Gruyter. This work is licensed under the Creative Commons Attribution 4.0 International License.

especially, if a low-cost DRO is employed. This problem can be solved by using a voltage-controlled DRO and lock it to a crystal reference in a PLL. However, this raises the DRO phase noise, mainly due to varactor pulling. Moreover, the electronic tuning range of DROs is quite limited, and manual tuning is usually required, which raises the system cost significantly. A solution based on a free running DRO is, therefore, highly desirable to avoid electrical and mechanical DRO tuning.

This paper proposes a method to lower the PN of mmW PLLs by combining a PLL cascade with a free running DRO. The low PN is achieved by dividing the output frequency of the VCO in PLL1 and up-converting the result by means of a single-sideband (SSB) mixer driven by the DRO. The presented circuit architecture requires no manual or electrical tuning of the DRO and compensates its frequency drift due to temperature changes and aging.

2 Architecture

In a first step, we assume that a *calibrated* low-noise DRO in the lower GHz range is available. A frequency division of a PLL output signal using a cascade of i divide-by-two circuits (DTC) will reduce the PN of a signal by $i \times 6$ dB. An up-conversion of the divided signal by an SSB mixer will leave this low PN basically unchanged. The combination of these two operations leads us to the brute force approach depicted in Figure 1.

Here, a PLL in the lower GHz range (PLL1) generates an output frequency from a crystal oscillator, preferably an oven-controlled crystal oscillator (OCXO). The multiplication factor can be an integer number, i.e. $\alpha = 0$, or a fractional number ($\alpha > 0$). In order to reduce the PN and the spurious tones (spurs) in the output spectrum, the output signal is divided by a cascade of i DTCs, typically $i = 2$–4. The DRO signal is also divided by a cascade of k DTCs, typically $k = 1$–2. The DTCs deliver accurate quadrature signals (I and Q) which are needed for single-sideband mixing. As long as the signals stay on the same chip, the accuracy of this method is high over a wide frequency range. In [7] the measured static phase error was as low as 0.16° for an output frequency of 20 GHz, corresponding to a sideband suppression of 57 dB. Each DTC reduces the phase noise by 6 dB, assuming that the divider noise can be neglected.

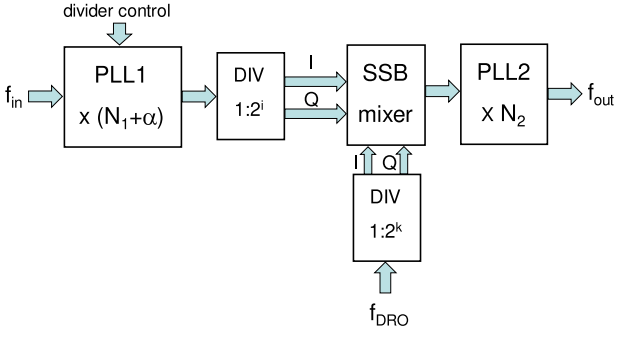

Figure 1: Uncompensated low-jitter PLL cascade using a single-sideband mixer driven by a dielectric resonator oscillator.

For illustration, we assume that a low-noise 4.4 GHz DRO and a high-noise PLL1 at 2 GHz are available. A frequency division by i DTCs will reduce the PLL PN by $i \times 6$ dB, and the division of the DRO frequency by k DTCs will reduce its PN by $k \times 6$ dB. These two low-noise signals are then mixed, where their PN is added to a level, which is still much lower than that of PLL1. Figure 2 illustrates this effect for $i = 3$ and $k = 1$, where the PN level is much exaggerated.

The divided outputs are multiplied in a single-sideband (SSB) mixer. The PN reduction is reflected in the narrower line at the mixer output (violet curve) compared to the broader line of PLL1 (dark blue curve). Assuming a perfect DRO output signal and a noiseless mixer, the mixing operation will neither change the shape of the PN spectrum nor the level of spurs. Neglecting the noise of the DRO, the dividers and the SSB mixer for a moment, the overall PN reduction of PLL1 is as large as 18 dB with similar center frequencies of PLL1 and SSB mixer output.

The architecture in Figure 1 was named 'uncompensated', since any deviation of the DRO frequency from the nominal value will appear at the output of the cascade. This requires manual tuning of the DRO, which raises the total system cost. A tunable DRO has also a higher phase

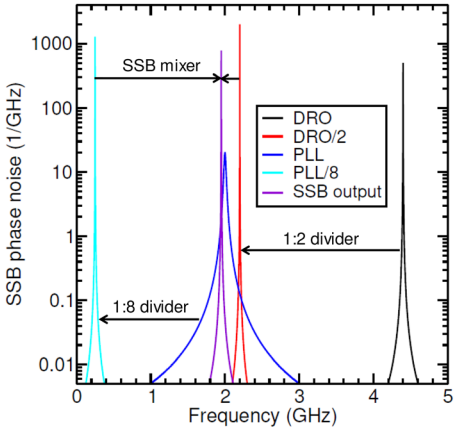

Figure 2: Single-sideband phase noise spectrum at different locations in the circuit. The phase noise level is exaggerated for better visibility.

noise compared to a free-running DRO. Moreover, the change of the DRO frequency with temperature is typically larger than for a crystal oscillator, which may require phase locking with the crystal as reference. In order to solve these problems, the SSB mixer should be included in the feedback loop of PLL1 as depicted in Figure 3.

Some exemplary numbers are given related to a possible application in the 122 GHz ISM band. The divided VCO signal is compared with an 80 MHz input signal in the phase detector. Here, the term 'phase detector' includes all circuitry to derive the VCO control voltage(s) from the incoming signals, typically a phase-frequency detector (PFD), one or two charge pumps (CP), and one or two low-pass filters (LPF). If the output frequency of the DRO is modified due to temperature change or aging, the feedback loop will change the VCO tuning voltage such that the SSB mixer output frequency remains at the nominal value, defined as the crystal oscillator frequency multiplied by the feedback divider ratio N_1.

3 Spectral purity considerations

3.1 Sideband suppression

In an SSB mixer unwanted sidebands appear due to delay mismatches between the I and the Q paths. In the case of the 122 GHz ISM band synthesizer, they will occur at the sum of the two input frequencies of about 2.5 GHz. After multiplication by 64 this corresponds to frequencies around 160 GHz. Sidebands at these frequencies are well suppressed by the antenna filter of a system working in the 122 GHz ISM band.

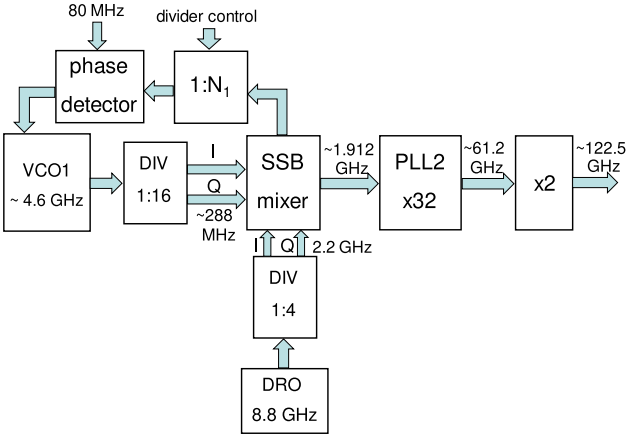

Figure 3: Compensated low-jitter PLL cascade for the 122 GHz ISM band.

3.2 Phase noise spectrum

A more severe problem is PN. Let us assume a PN of –110 dBc/Hz at 100 kHz offset from the 4.6 GHz carrier. After the 1:16 frequency divider this corresponds to a PN of –134 dBc/Hz. The PN of DROs is much lower than that of silicon-based integrated VCOs. In [8] a PN of –125 dBc/Hz was specified at 100 kHz offset from the 8.8 GHz carrier. We assume a little more conservatively a PN of –122 dBc/Hz at 8.8 GHz and obtain –134 dBc/Hz after the 1:4 frequency divider shown in Figure 3. As a result, we expect a PN of –131 dBc/Hz at 100 kHz offset from the 1.9 GHz mixer output, and –95 dBc/Hz in the 122 GHz ISM band. This is much lower than for typical mmW PLLs [9]. Note that the PN contributions of frequency dividers, SSB mixer and frequency doubler were disregarded in this simplified consideration. Nonetheless, it is evident that PN and spurs in a PLL can be reduced significantly by combining frequency division and SSB mixing, provided that a low-noise frequency source such as a DRO or an OEO is available.

3.3 Jitter minimization

For a rough jitter estimation, the power spectral density (PSD) of the PLL output phase can be described in the framework of an overdamped second-order PLL model [10]. Here, the low-pass filtered in-band PN floor adds to the high-pass filtered VCO PN spectrum according to

$$S_\phi(f) = S_{\text{floor}}\, H_{\text{LPF}}(f) + S_{\text{VCO}}(f)\, H_{\text{HPF}}(f). \tag{1}$$

The rms timing jitter at the PLL output is given by

$$\sigma_t = \frac{1}{2\pi f_{\text{out}}} \sqrt{\int_0^\infty 2 S_\phi(f)\, \mathrm{d}f} \tag{2}$$

where $S_\phi(f) = 10^{£(f)/10}$ is the *two-sided* PN spectrum. The jitter minimization for the PLL cascade implies the optimization of two loop bandwidths. According to (3) in [11], the jitter-optimum loop bandwidth for each of the two PLLs is approximately given by

$$f_{\text{L}}^{\text{opt}}[\text{MHz}] = \sqrt{S_{\text{VCO}}/S_{\text{floor}}} \tag{3}$$

where $S_{\text{VCO}} = 10^{£_{\text{VCO}}/10}$ is the VCO PN at 1 MHz offset, and $S_{\text{floor}} = 10^{£_{\text{floor}}/10}$ is the in-band PN floor of the PLL. The corresponding minimum timing jitter in seconds reads

$$\sigma_t^{\min} = \frac{1}{f_{\text{out}}} \sqrt{\frac{1\,\text{MHz}}{2\pi}} \left(S_{\text{VCO}}\, S_{\text{floor}}\right)^{1/4} \tag{4}$$

where f_{out} is the PLL output frequency. Note that 1/f noise was disregarded in (3) and (4).

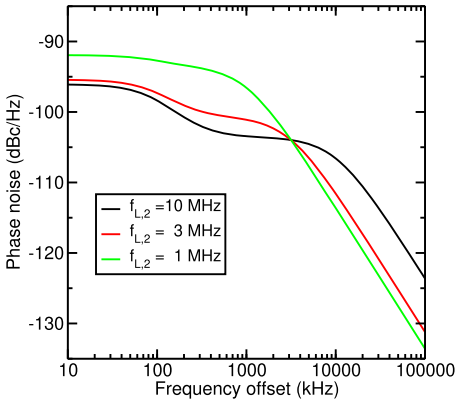

Figure 4: Modelled PN spectrum at the output of the 60 GHz PLL from Figure 3 for three different loop bandwidths $f_{L,2}$.

As an illustration, we assume a PN of –94 dBc/Hz for VCO2 at 1 MHz offset and an in-band noise floor of –104 dBc/Hz for PLL2. From (3) we obtain an optimum loop bandwidth of $\sqrt{10}$ MHz ≈ 3.16 MHz for PLL2. Figure 4 shows the modelled PN spectrum for three different loop bandwidths of PLL2.

The red curve has a loop bandwidth close to the optimum value according to (3).

In order to see the effect of the post-synthesis divider and the SSB mixer, we calculated the spectrum for $f_{L,2}$ = 3 MHz also for a simple cascade composed of PLL1 and PLL2 (i = 0) and for different numbers of DTCs after the VCO. As evident from Figure 5, the improved cascade has a significantly lower PN in the kHz region.

The PN in the kHz range can be reduced even more, if the division ratio of the post-synthesis divider is increased from 16 to 32 or 64. Even though this does not significantly reduce the overall rms jitter, such a phase noise reduction in the lower kHz region may significantly improve detection and tracking performance of mmW FMCW radar systems [9].

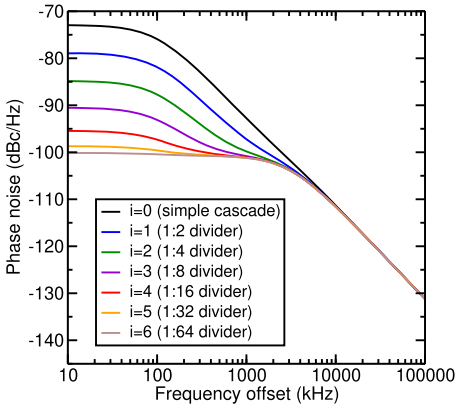

Figure 5: Modelled phase noise spectrum at the output of the 60 GHz PLL for the simple PLL cascade (black), and the PLL cascade including SSB mixer and i post-synthesis DTCs after the VCO.

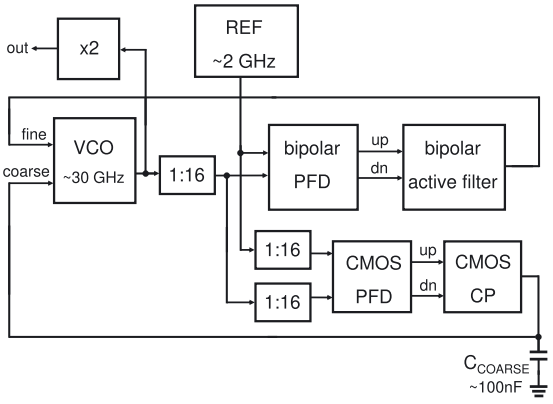

Figure 6: Block diagram of PLL2.

4 Design example

We have designed an exemplary circuit in a 130 nm SiGe BiCMOS technology featuring SiGe HBTs with f_T/f_{max} of 240/330 GHz [12].

4.1 PLL architecture

The basic design of the PLLs is similar to the PLL described in [13]. Figure 6 shows a simplified block diagram of PLL2.

A fast fine tuning loop and a slow coarse tuning loop are used in parallel and are permanently working together. The task of the coarse tuning loop is the compensation of device parameters with process, supply voltage and temperature (PVT), whereas the fine tuning loop defines the small-signal dynamics and the PN behavior. The output of the CMOS CP in the coarse tuning loop is loaded only with an on-chip capacitor to ground in parallel with a large external capacitor C_{COARSE}. Unlike in [13], we neither use a CMOS PFD nor a CP in the fine tuning loop of PLL2. Rather, a bipolar PFD followed by a differential bipolar amplifier is employed. The high speed of the SiGe-HBTs allows the input frequency to the PFD to be as large as several GHz. By using two 1:16 frequency dividers, the input frequency to the CMOS PFD is reduced to about 125 MHz, a convenient frequency for the thick-oxide MOSFETs used for CMOS PFD and CP.

4.2 Design of VCO and frequency dividers

The VCO represents a differential Colpitts oscillator shown in Figure 7.

The VCO uses four digital inputs to generate 16 subbands, where the highest bit is realized by inductor switching. In addition, the analog control input V_{ctr} used

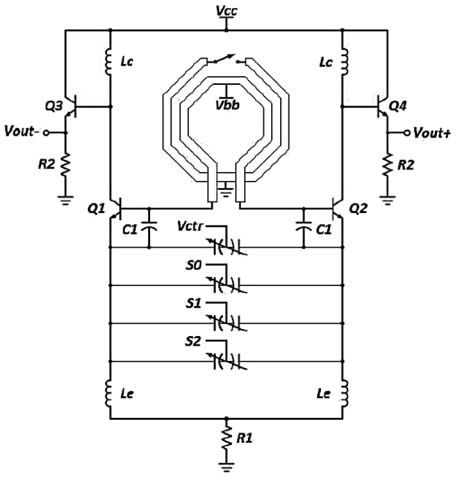

Figure 7: Schematic of voltage-controlled oscillator taken from [14].

in [14] is split into two control inputs for coarse and fine tuning according to Figure 6. The output frequency of the VCO is doubled by using a SiGe-based Gilbert mixer.

All dividers in PLL2 are cascades of DTCs to simplify the design and to minimize DC power consumption. Figure 8 shows the schematic of a DTC composed of two latches in a feedback loop, and Figure 9 shows the schematic of the latch.

The internal divider circuit uses only one emitter follower. The second emitter follower is used for driving external loads.

4.3 Design of phase-frequency detector

Figure 10 shows the schematic of the bipolar PFD.

It consists of two edge-triggered resettable D-flipflops designed with SiGe-HBTs for a high speed. Their D inputs are connected to logical ONE. A standard master-slave

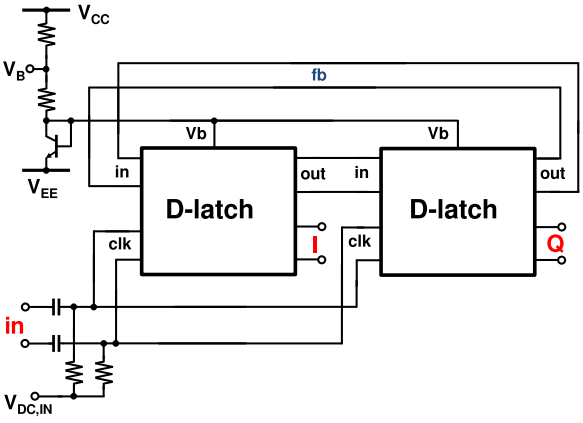

Figure 8: Schematic of divide-by-two circuit.

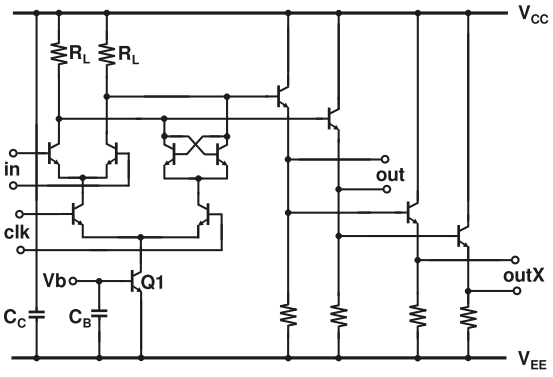

Figure 9: Schematic of D-latch.

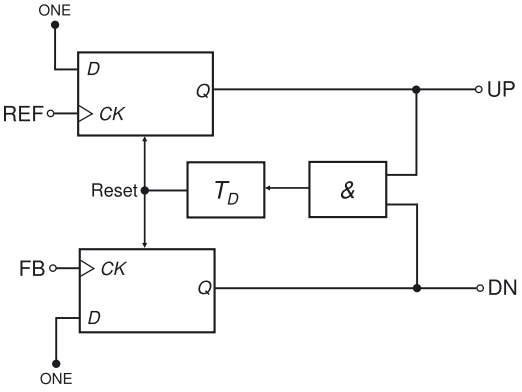

Figure 10: Schematic of phase-frequency detector.

configuration with an additional reset input was used for the ECL flipflops. All signals are differential, but only the positive branches are shown in Figure 10. The delay element in the reset path minimizes the dead-zone effect. As usual, the resettable D-flipflop is composed of two latches. Figure 11 shows the schematic of the resettable D-latch consisting of five differential pairs.

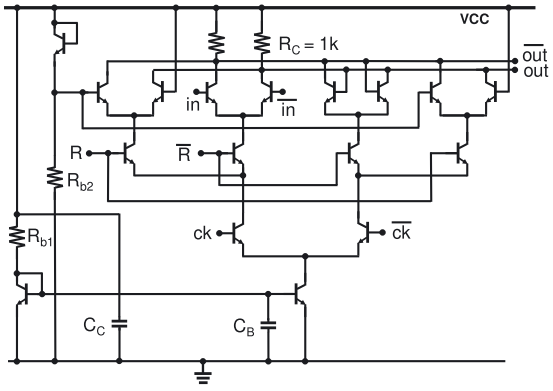

Figure 11: Schematic of resettable D-latch.

The lowest pair receives the differential clock signal and is biased by a current mirror. If the differential reset signal is LOW, then the current flows through the inner pairs, and the latch behaves like a classical D-latch. If the reset signal R goes HIGH, the current flows through the outer differential pairs and from there through the load resistor R_C connected to the positive output node "out". In other words, the differential output signal is LOW in this case, as desired.

4.4 Design of active filter

An active loop filter as in [15] was used to avoid any MOSFET in the fine tuning loop. Figure 12 shows the schematic of the active loop filter.

Unlike in [15], our filter is completely integrated and is designed for a large loop bandwidth. The amplifier is a two-stage differential bipolar amplifier. Its shot noise contribution to the phase noise spectrum is minimized by using a small VCO fine tuning gain. The output of the amplifier is softly biased close to the middle of the rails. As discussed in [13], such a biasing keeps the VCO fine tuning gain and the phase noise spectrum constant, regardless of PVT variations.

4.5 Design of SSB mixer

Figure 13 shows the schematic of the SSB mixer.

It consists of two Gilbert mixers with connected outputs. The differential output is loaded with a capacitor for high-pass filtering. Figure 14 shows the layout of the SSB mixer including 1:2 and 1:8 frequency dividers at the inputs.

The layout of the whole circuit is depicted in Figure 15.

With a reference input of 80 MHz and an 8.8 GHz DRO input a default frequency of 61.44 GHz is generated. Another output at the divided VCO frequency (7.68 GHz) can be used for phase noise measurements.

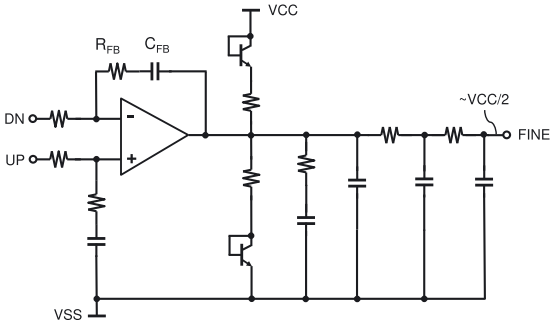

Figure 12: Schematic of active loop filter.

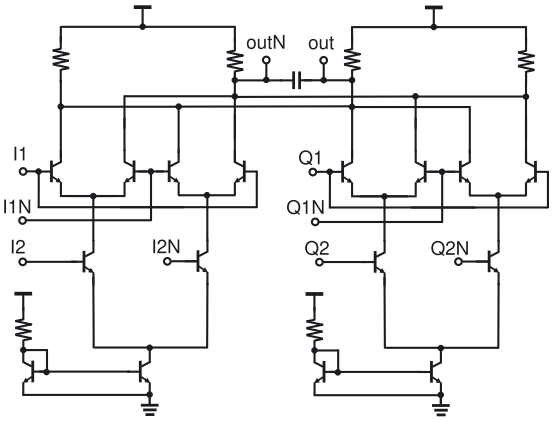

Figure 13: Schematic of SSB mixer.

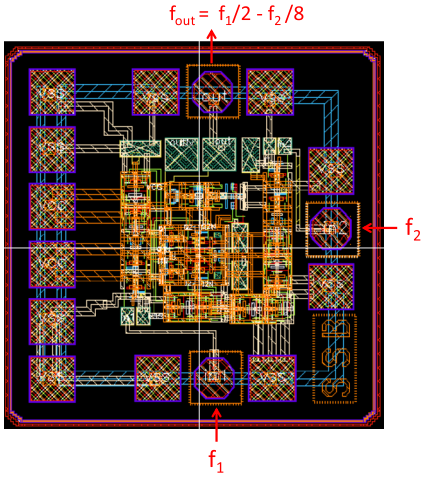

Figure 14: Layout of SSB mixer preceded by 1:2 and 1:8 frequency divider at first and second input, respectively.

5 Simulation results

We have simulated both PLLs on transistor level. Figure 16 shows the simulated settling behavior of PLL2.

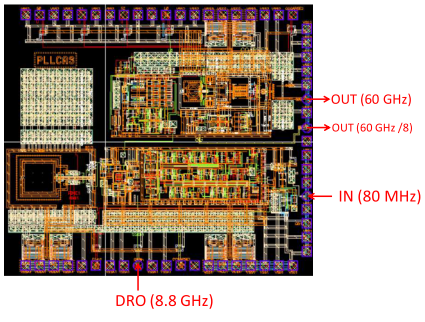

Figure 15: Layout of PLL cascade including post-synthesis dividers and single-sideband mixer.

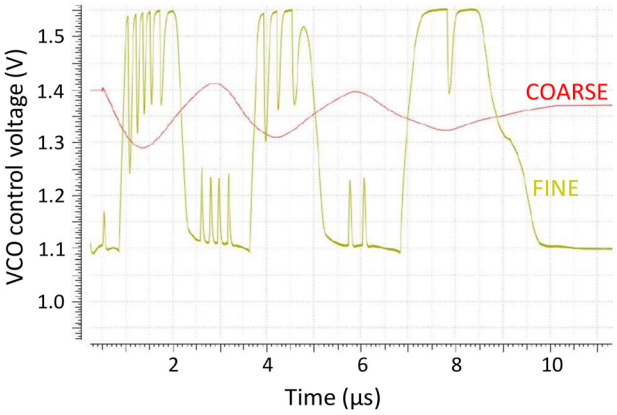

Figure 16: Simulated settling of VCO control voltages in PLL2.

During the first 10 µs the loop filter capacitances are loaded and the tuning voltages oscillate. After that period, the tuning voltages converge exponentially towards the final values. The time constant is below 1 µs, corresponding to a large loop bandwidth of PLL2. Figure 17 shows the simulated PFD output signals close to the steady state. The input frequency was as high as 3.3 GHz.

Obviously, the SiGe-HBTs used for this PFD are fast enough for such a high input frequency. As a result, the phase noise contribution of the phase detector in PLL2 is reduced, since the noise multiplication factor $20\ \log(N_2)$ is fairly small.

6 Conclusions

We have presented a low-noise PLL cascade architecture. A first programmable PLL in a few-gigahertz range is proposed to drive a second mmW PLL. The insertion of a frequency divider and an SSB mixer within the first PLL results in a low clock jitter, provided that the mixer is driven by a spectrally pure signal. A free running DRO can be employed for this purpose which avoids manual tuning. An exemplary design in BiCMOS technology was analyzed and simulated on transistor level. It employs a high-speed PFD using SiGe-HBTs to achieve a low in-band noise floor of the second PLL. The presented circuit architecture can be used for generating a low-cost, stable, mmW local oscillator source for terrestrial and satellite communications.

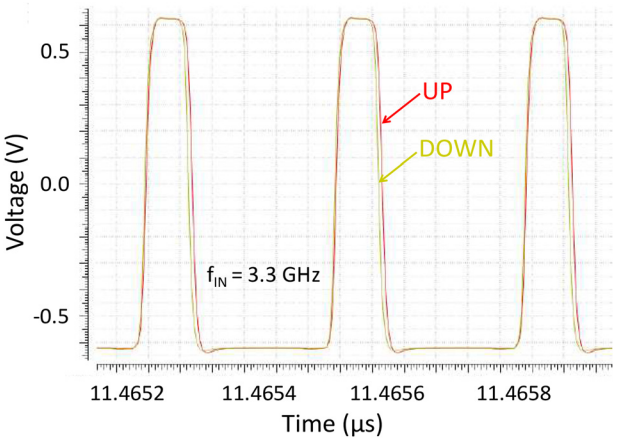

Figure 17: Simulated steady-state PFD output voltages.

Author contribution: All the authors have accepted responsibility for the entire content of this submitted manuscript and approved submission.
Research funding: None declared.
Conflict of interest statement: The authors declare no conflicts of interest regarding this article.

References

[1] B. Razavi, "Jitter-power trade-offs in PLLs," *IEEE Trans. Circ. Syst. I: Regular Papers*, vol. 68, no. 4, pp. 1381–1387, 2021.
[2] S. A. Osmany, F. Herzel, and J. C. Scheytt, "Analysis and minimization of substrate spurs in fractional-N frequency synthesizers," *Analog Integr. Circuits Signal Process.*, vol. 74, no. 3, pp. 545–556, 2013.
[3] W. El-Halwagy, A. Nag, P. Hisayasu, F. Aryanfar, and P. Mousavi, "A 28-GHz quadrature fractional-N frequency synthesizer for 5G transceivers with less than 100-fs jitter based on cascaded PLL architecture," *IEEE Trans. Microw. Theor. Tech.*, vol. 65, no. 2, pp. 396–413, 2017.
[4] A. Axholt and H. Sjöland, "A 60 GHz receiver front-end with PLL based phase controlled LO generation for phased-arrays," *Analog Integr. Circuits Signal Process.*, vol. 80, no. 1, pp. 23–32, 2014.
[5] A. K. Poddar and U. L. Rohde, "The pursuit for low cost and low phase noise synthesized signal sources: theory & optimization," in *Proc. of 2014 IEEE International Frequency Control Symposium (FCS 2014)*, Taipei, Taiwan, 2014, pp. 1–9.
[6] H. P. Forstner, H. D. Wohlmuth, H. Knapp, et al., "A 19 GHz DRO downconverter MMIC for 77 GHz automotive radar frontends in a SiGe bipolar production technology," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Monterey, CA, 2008, pp. 117–120.
[7] F. Herzel, J. Borngräber, and A. Ergintav, "A 60 GHz frequency divider with quadrature outputs in SiGe BiCMOS technology for optical OFDM systems," in *Proc. of the 10th European Microwave Integrated Circuits Conference (EuMIC 2015)*, Paris, France, 2015, pp. 69–72.
[8] Z-Communications, "Voltage-controlled oscillator surface mount module," in *DRO8800A datasheet, Rev. A1*, 2021.
[9] K. Siddiq, M. K. Hobden, S. R. Pennock, and R. J. Watson, "Phase noise in FMCW radar systems," *IEEE Trans. Aero. Electron. Syst.*, vol. 55, no. 1, pp. 70–81, 2019.
[10] F. Herzel, S. Waldmann, and D. Kissinger, "Numerical jitter minimization for PLL-based FMCW radar systems," *IEEE Trans.*

Circ. Syst. I: Regular Papers, vol. 66, no. 7, pp. 2478–2488, 2019.

[11] F. Herzel, A. Ergintav, J. Borngraeber, H. J. Ng, and D. Kissinger, "Design of a low-jitter wideband frequency synthesizer for 802.11ad wireless OFDM systems using a frequency sixtupler," in *Proc. IEEE ISCAS*, Baltimore, MD, 2017, pp. 1–4.

[12] H. Rücker, B. Heinemann, W. Winkler, et al., "A 0.13 SiGe BiCMOS technology featuring of 240/330 GHz and gate delays below 3 ps," *IEEE J. Solid State Circ.*, vol. 45, no. 9, pp. 1678–1686, 2010.

[13] F. Herzel, S. A. Osmany, K. Schmalz, et al., "An integrated 18 GHz fractional-N PLL in SiGe BiCMOS technology for satellite communications," in *Proc. of 2009 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2009)*, Boston, USA, 2009, pp. 329–332.

[14] M. Kucharski, F. Herzel, H. J. Ng, and D. Kissinger, "A Ka-band BiCMOS LC-VCO with wide tuning range and low phase noise using switched coupled inductors," in *Proc. of the 11th European Microwave Integrated Circuits Conference (EuMIC 2016)*, London, UK, 2016, pp. 201–204.

[15] H.-V. Heyer, A. Koelnberger, H. Telle, et al., "Wide frequency range fractional-N synthesizer with improved phase noise for flexible payloads," in *Proc. of 2nd ESA Workshop on Advanced Telecom Payloads*, The Netherlands, Noordwijk, 2012, pp. 1–8.