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In-orbit VNIR sensor quality validation

Johannes Buschek[a], Andreas Eckardt[a], Kristian Manthey[a], Karsten Sengebusch[b], Olaf Schrey[c], Denis Piechaczek[c], and Gerhard Kahmen[d]

[a]German Aerospace Center (DLR), Institute of Optical Sensor Systems, Berlin, Germany
[b]EURECA Messtechnik GmbH, 50679 Köln, Germany
[c]Fraunhofer Institute for Microelectronic Circuits and Systems (IMS), Duisburg, Germany
[d]Leibniz Institute for High Performance Microelectronics (IHP), Frankfurt (Oder), Germany

ABSTRACT

The Institute of Optical Sensor Systems (OS) at the Robotics and Mechatronics Center of the German Aerospace Center (DLR) has more than 40 years of experience in high-resolution imaging and imaging technology. This paper presents the current status of the institute's work on next-generation CMOS-TDI detector development. Together with the partners IHP (Leibniz Institute for High Performance Microelectronics), IMS (Fraunhofer Institute for Microelectronic Circuits and Systems), and JOP (Jena-Optronik GmbH), a new test detector was designed consisting of an embedded charge-coupled device (eCCD) and a readout integrated circuit (ROIC), combined as a silicon-bonded design. This approach enables operation at a line rate up to 150 kHz and a full well capacity above 150 ke-, thus making it very promising for high-spatial-resolution imaging systems. An FPGA-based engineering model environment with high design flexibility distributes all eCCD clocking and ROIC control signals. The unidirectional eCCD design is optimized for electrical charge injection tests and is used to verify in-orbit initialization approaches, including eCCD signal reconstruction. The paper will outline this procedure. Due to the accessible detector building blocks, this setup is ideally suited for future evaluation and verification of accumulative radiation effects on the eCCD and ROIC structures and determining possible corrective actions to contain overall radiation-related performance degradation over the mission lifetime. The evaluated method is intended to estimate the sensor's behavior under space environmental conditions during the entire mission by introducing a detector initialization phase.

Keywords: CCD, CMOS, TDI, charge injection, signal reconstruction

1. INTRODUCTION

The combination of CCD technology and CMOS-based integrated circuitry for pixel readout provides the technological basis for the next-generation detector development described in previous publications.[1,2,3] Critical parameters such as pixel behavior, achievable maximum line rate, and time delay integration operation make it suitable for high-spatial-resolution imaging systems. In the system described below, an eCCD and a ROIC are assembled in one physical package to demonstrate the interacting performance of these key elements of the aspired final detector concept. It will play a significant role during the verification phase of forthcoming, higher-integrated detector systems.

2. TEST DETECTOR ARCHITECTURE

The eCCD consists of 15 charge-coupled device test field structures, ten with 128 and five with 256 TDI stages, each implemented with a slightly different design. For the results presented in this paper, the test field selection and its technology differences play a minor role but allow upcoming technology development evaluation and verification. The main signal path from eCCD to analog-to-digital converter (ADC) is depicted in Figure 1: The unidirectional concept allows charge injection into the eCCD matrix at one side (injection side) and regular CCD readout through a floating diffusion (FD) output structure at the opposite side (readout side) via a source follower circuit (SF). After the biasing circuitry (BIAS) and the output multiplexer (MUX), the output signal is

Send correspondence to: johannes.buschek@dlr.de

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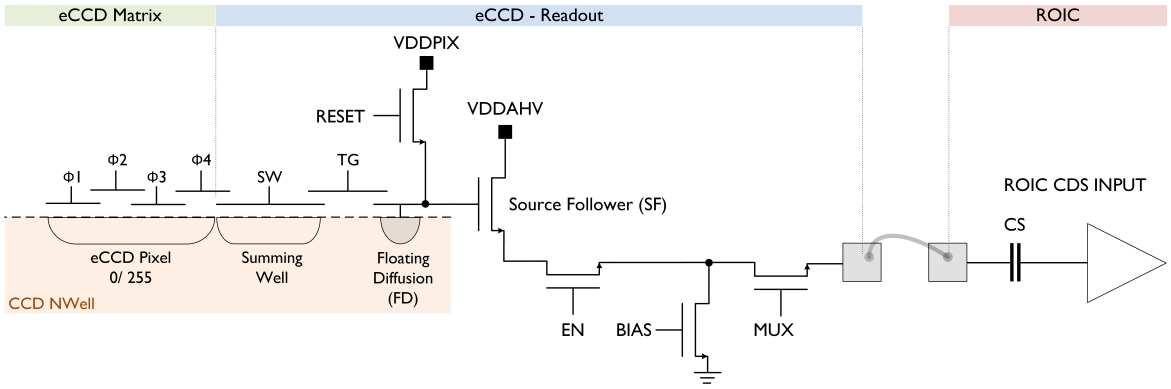

Figure 1: Schematic illustration of the analogue readout path

connected to the input of the ROIC. While this does not correspond with the final bidirectional design goal,[3] this setup is suitable for gaining the required knowledge of eCCD and ROIC technology in interaction. In addition to its well-known optical capabilities, the sensor system provides the functionality of charge injection, known as fill-and-spill,[4] as a crucial element of electrical characterization, which will be examined in the following section.

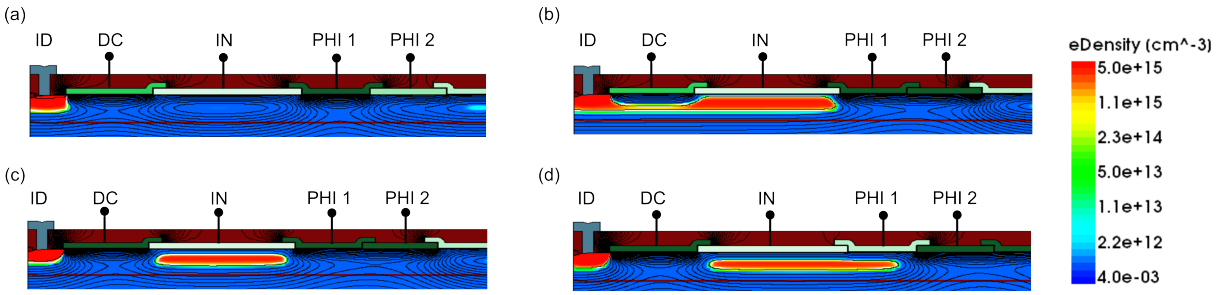

Figure 2: TCAD simulation of the charge injection structure and the fill-and-spill method. (a) Starting point of the injection cycle. IN forms a potential well while DC acts as a barrier. (b) Lowering the voltage V_{ID} causes a charge injection into the potential well. (c) Electrons start to flow back to ID as soon as V_{ID} is increased back to the initial state. A particular number of charge carriers remains under the IN gate. (d) Charge is transferred into the first pixel of the eCCD matrix. The color scale shows the volume charge density as calculated from the 2-dimensional TCAD simulation according to (1).

The fill-and-spill method is an electrical charge injection technique making use of an n^+-drain (ID) and two input gates DC and IN. The input structure as well as the basic working principle of the fill-and-spill method was simulated with technology computer aided design (TCAD) and is shown in Figure 2. At the beginning of the fill-and-spill process, the voltages V_{DC} and V_{IN} are chosen such that a potential well is formed underneath the gate IN while DC forms a potential barrier (a). Hence, the applied voltage on DC during the injection has to be lower compared to the applied voltage on IN. Moreover, PHI1 acts as a blocking gate during the injection process to isolate the potential well from the CCD channel. The injection cycle starts when the voltage V_{ID} is lowered, causing the regions under the gates DC and IN to fill with electrons (b). To remove the excess electrons afterwards, the increment of V_{ID} after the injection to the initial level results in a spilling of electrons back into the drain (c). Nevertheless, since V_{IN} forms a potential well, a particular number of electrons remains in this potential well since they can not pass the potential barrier formed by V_{DC}. This fill-and-spill process is reproducible, and the injection yields a defined number of charge carriers which depends on V_{IN} and V_{DC}. The remaining charge carriers are then transferred under the PHI1-gate (d) according to the clocking pattern shown in Figure 3. The applied voltage on the IN gate adjusts the size of the charge packet. Thus, increasing the voltage V_{IN} results in a larger charge packet and vice versa. During the injection process, the number of injected

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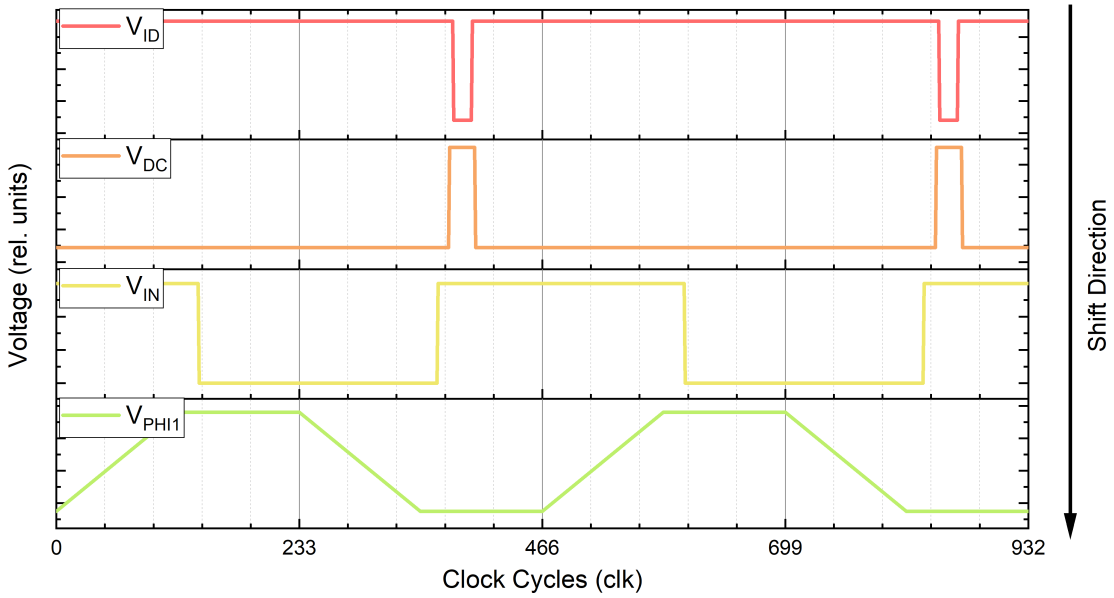

Figure 3: Clocking pattern for the fill-and-spill method.

charge carriers N_{inj} can be calculated by the difference between the applied voltages V_{IN} and V_{DC}, according to

$$N_{\text{inj}} = \frac{C_{\text{ox}} \cdot (V_{\text{IN}} - V_{\text{DC}})}{e}, \tag{1}$$

where C_{ox} denotes the oxide capacitance and e is the elementary charge. However, the linearity of this equation is only valid for surface channel CCDs. In the case of buried channel CCDs, the number of charge carriers increases non-linearly with an increasing injection voltage.[5,6] To prove this behavior, a TCAD simulation was performed where different-sized charge packets were injected in dependence on V_{IN}. The quantity of the injected electrons was determined using TCADs analysis tool, which carries out an integration over the height $h = 1$ µm of the buried channel and the length $l = 3.5$ µm of the IN-gate. As a result, the charge carrier density ρ_{inj} is obtained, which has the dimension [cm^{-1}]. Finally, the resulting charge carrier density has to be multiplied with the width $d = 5.4$ µm (depth information) of the pixel to determine the total number of injected electrons, i.e.,

$$N_{\text{inj}} = \rho_{\text{inj}} \cdot d. \tag{2}$$

Figure 4a depicts the number of charge carriers versus V_{IN}. Consequently, this simulation indicates a non-linear capacitance behavior dependent on the injected charge. Solving equation (1) for the capacitance C_{ox} and using the resulting numbers of charge carriers yields the curve depicted in Figure 4c. Here, it can be observed that as the accumulated amount of charge expands towards the Si/SiO_2 interface, the capacitance starts to scale linearly, causing the buried channel CCD to operate similarly to a surface channel CCD and proving the statement above.

In order to gain an understanding of the subsequent parts of the sensor system after charge injection, charge transport, and charge readout, the upcoming section provides an overview of the core components of the ROIC and their working principle: Figure 6b shows the face-to-face bonded setup (PGA-132 package: eCCD in the upper part and the ROIC in the lower part), including eight active pixel connections, which turns the design into an 8-pixel-TDI-column-wise ADC. Two eCCD output channels are accessible for analog measurement of the eCCD output signal to debug system functionality and compare the signal reconstruction results; in addition, two ROIC input channels can either be terminated for noise measurements or driven externally by an emulated eCCD

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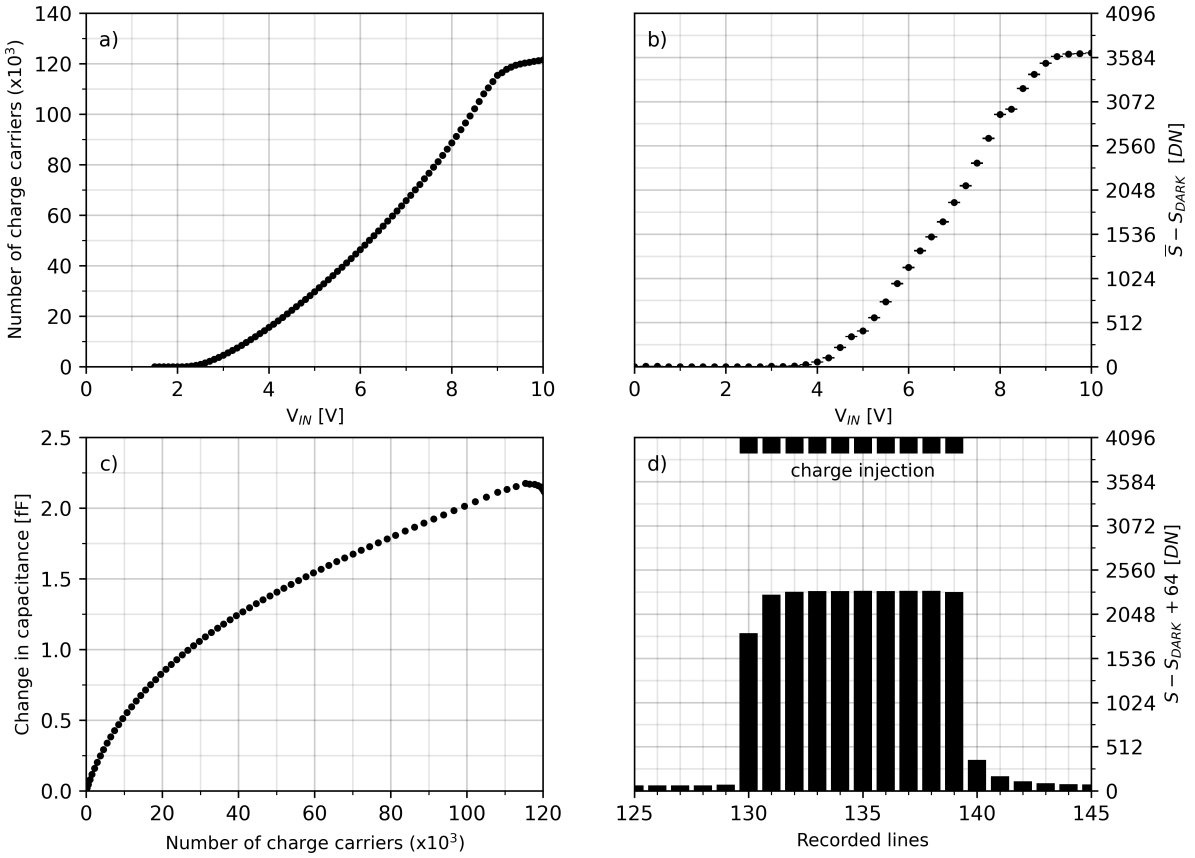

Figure 4: Simulation of the injected charge and the resulting capacitance for a buried-channel CCD: Number of charge carriers versus injection voltage (a), change in capacitance versus the number of charge carriers (c). Charge injection measurement at FSI eCCD (b) and fill-and-spill impulse train measurement for dynamic charge transfer efficiency (CTE) verification (d)

output signal for ADC validation. Besides these two ROIC input channels, all other 126 ROIC input channels can be assigned to pixels 1 and 2 of the data output by setting the five output multiplexer bits, and together with the eight active pixels, they form an overall data output stream of 10 pixels. The CDS input stage (CDS), the comparator circuitry (COMP), and the data capture block (CAPT) are the main elements of the ROIC (Figure 5). The CDS input stage contains a correlated double sampling (CDS) circuitry, performing a signal zero shift at the eCCD reset level and providing the comparator input voltage by converting the settled eCCD pixel value into an inverted positive voltage level after the sample-and-hold circuitry, which corresponds to the difference between eCCD reset and pixel level, without absolute DC components. This widely used differential sampling technique minimizes reset noise and helps suppress the flicker noise of the on-chip amplifier.[7,8] The subsequent auto-zero comparator circuitry compares the sample-and-hold output pixel value with an analog linear ramp signal. This ramp signal runs parallel with a 12-bit gray-code counter, which stops when both comparator input signals coincide. In the data capture block, the content of the gray-code counter register is transferred into the 12-bit pixel serializer to provide one-pixel output data per TDI line period.

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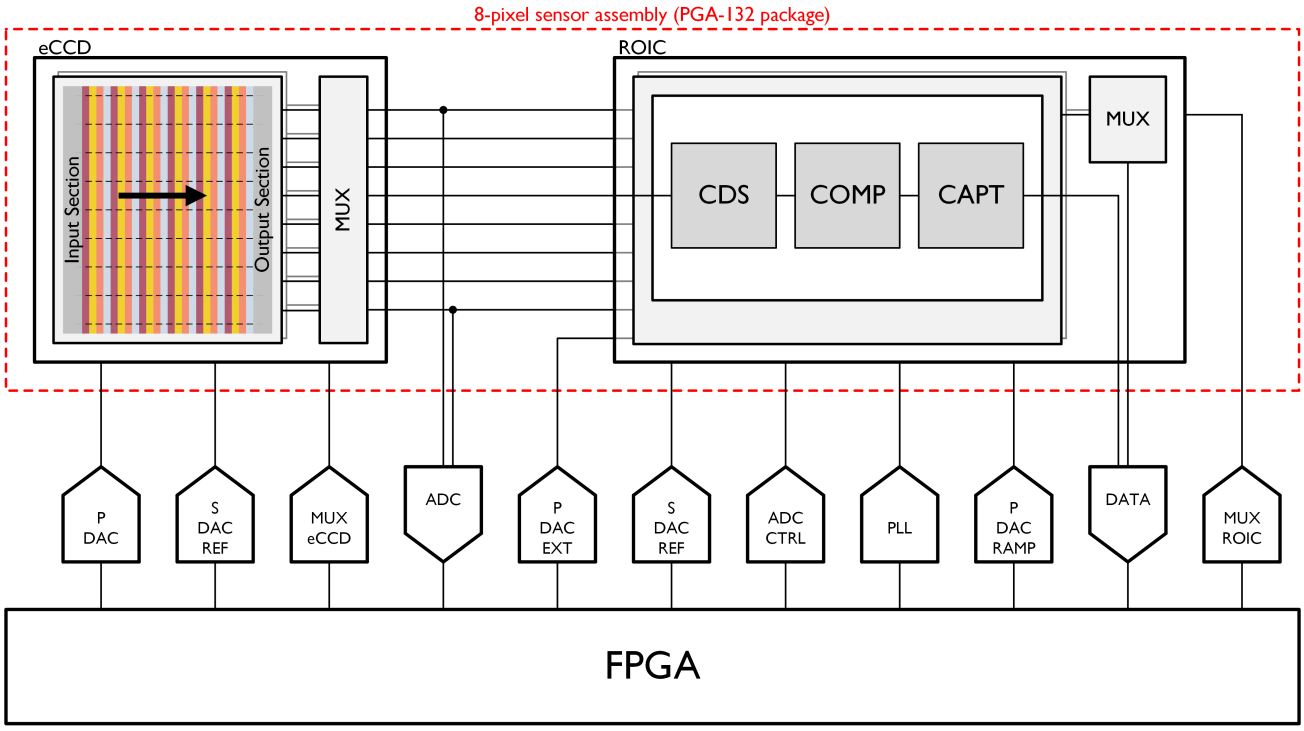

Figure 5: Test environment block diagram

3. TEST ENVIRONMENT

Figure 5 depicts the block diagram of the test environment with the sensor assembly marked in red, which is located at the center of the support PCB (Figure 6a). All required support and control circuitry is placed on a printed circuit board with eight layers arranged in functional groups around the zero-force PGA socket. Two synchronized FPGA modules are accountable for providing all detector-relevant signals, including high-speed ADC- and parallel DAC signals and serial data streams, logic level control signals, and ROIC image data for further processing via an USB interface. Specific DAC output stages drive all high-level signals for eCCD charge transfer, eCCD output selection, and bias voltages. A dedicated clock generator provides synchronous clocks for FPGA signal generation and an external 660 MHz single-ended clock for proper internal 12 Bit gray-code counter operation. An external high-speed DAC generates the analog linear ramp signal to enhance debugging and test flexibility. Two FPGA boards with a Xilinx Artix 7 XCA200T are used: The first is for generating "slow" signals (e.g., SPI, multiplexers, data input) and USB communication, and the second is for signals controlling seven DACs with an operation frequency of 165 MHz each. The FPGA design was derived from a parallel ASIC development of the upcoming detector and contains all control logic necessary to operate the sensor assembly as an imaging camera, e.g., a telecommand/telemetry interface, command decoder, and parallel data interface. The FPGA includes EGSE components for interfacing, allowing the test board to connect to a PC through USB.

4. ELECTRICAL CHARACTERIZATION

The charge injection method fill-and-spill was used to determine the electrical characteristics of the sensor assembly, utilizing the same procedure as described in our previous publication.[3] Fine adjustment on the timing relation between vertical clocking signals and injection impulse reveals increased charge injection capability and a reworked overall fill-and-spill clocking scheme, compared to the pattern used for TCAD simulation, shown above in Figure 3. The updated implementation can cover 90% of the ADC range in static and dynamic fill-and-spill operation, generating a repetitive eCCD output signal for the signal reconstruction procedure almost over the entire dynamic range. Therefore, it is possible to validate the characteristics of the sensor system within this

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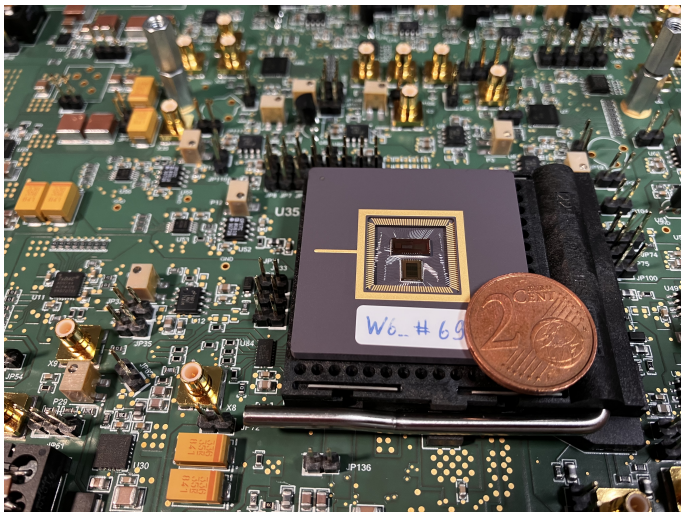
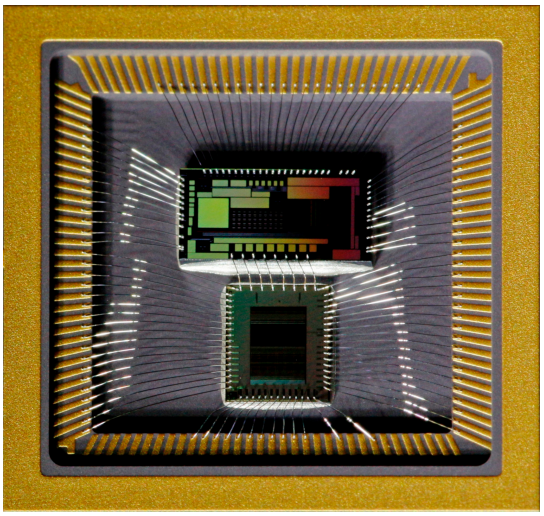


(a)



(b)

Figure 6: Test detector mounted in environment for testing (a) and sensor face-to-face assembly in PGA-132 package: eCCD in the upper part and the ROIC in the lower part (b)

signal range throughout the mission duration. In order to assess potential effects to the eCCD caused by aging or radiation during future space missions, charge pulse train tests on the current sensor system were conducted. This dynamic methodology relies on the known reproducibility of the fill-and-spill method and diminishes the importance of absolute signal accuracy. The resulting CTE for a given TDI depth can be calculated by injecting n lines at a defined level and analyzing the leading and trailing effects of the reshaped pulse train on the readout side[9] (Figure 4d). This capability allows accurate measurement and quantification of any CTE degradation that may occur during operational lifetime in space. Calculating the data with FPER/EPER[7] method reveals charge transfer efficiencies up to 99.90 % per charge transfer.

5. OPTICAL CHARACTERIZATION

For eCCD design verification, photon transfer curve[10] measurements were performed to evaluate the camera gain K of the sensor. This allows the calculation of the eCCDs sense node capacity C_{S} under consideration of all gain and ADC settings as follows

$$C_{\mathrm{S}} = \frac{A_{\mathrm{CDS}} \cdot A_{\mathrm{SF}}}{LSB \cdot K}, \tag{3}$$

where A_{CDS} denotes the gain of the CDS input stage, A_{SF} the gain of the eCCD output source follower stage, LSB one least significant bit of the ADC in V/DN, and K the measured camera gain in $DN/e-$. The results are listed in table 1.

Table 1: Camera gain K and sense node capacity C_{S} results for test different line rates

Line rate	Camera gain K	Sense node capacity C_{S}
30 kHz	0.01670 ± 0.00066 DN_{12}/e-	22.59 +0.93/−0.86 fF
150 kHz	0.01693 ± 0.00137 DN_{12}/e-	22.29 +1.96/−1.67 fF

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6. SIGNAL RECONSTRUCTION

In-orbit sensor quality validation relies on a reconfigured CDS operation mode of the existing ROIC ADC to reconstruct the analog eCCD output signal. The main objective is to identify and allocate radiation-induced degradation effects and find ways to contain them by optimizing ADC and eCCD operation control settings during the mission lifetime. The described test environment allows comparing the reconstructed output signal with the actual measured eCCD analog output, making it very suitable to evaluate the sub-sampling procedure for signal reconstruction. Utilizing static fill-and-spill operation for a repetitive eCCD output signal, ADCs sampling rate limitations can be reduced by equivalent-time sampling (ETS) methods,[11] establishing sub-sampling of the analog eCCD output signal. Due to the inherent ADC circuit design, the entire CDS regime must be involved in the ETS implementation. Consequently, the output information of this differential sub-sampling process contains the derivation of the analog eCCD output signal, which can be used to reconstruct and analyze the time-domain waveform by numerical integration. Figure 7 illustrates the ideal derivation (a) of the input (b), which acts as the input stimulus for SPICE simulation. Simulation (c) and measurement (d) are in line regarding signal output level and general signal shape, which can be stated as a confirmation of the working principle of the sub-sampling methodology.

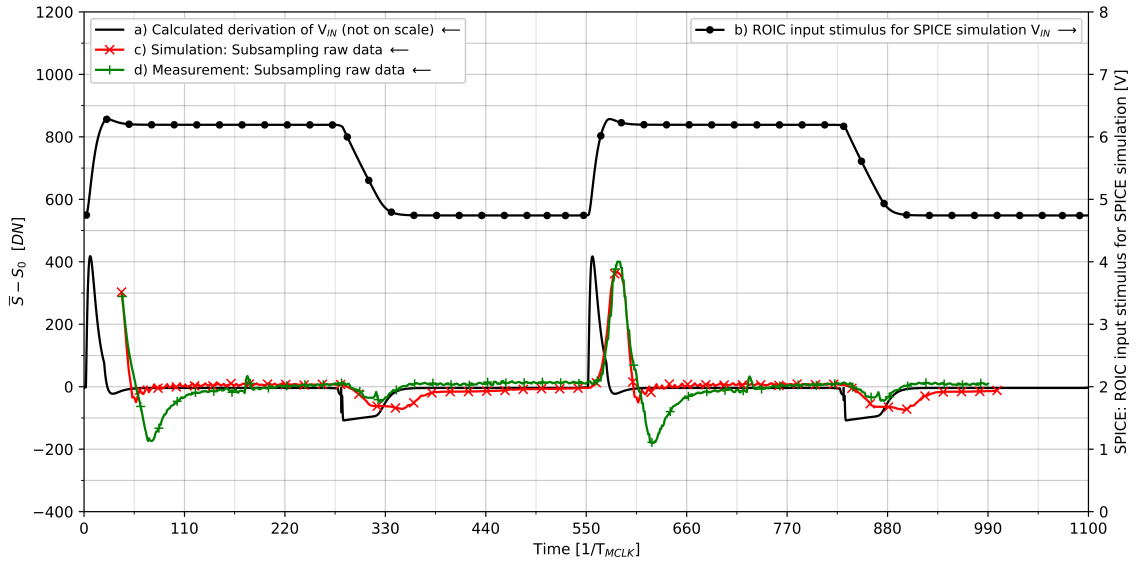

Figure 7: Simulation (c) and measurement (d) of the eCCD output signal derivation

7. CONCLUSION

The test detector's charge injection timing reveals improved results regarding the amount of injected charge and charge injection linearity. Crucial design parameter characterization mainly confirmed the design goals: Camera gain K, and the derived sense node capacity C_S align with the defined requirements. Charge transfer efficiency is already at a high level; nonetheless, there is potential to increase CTE in the further adjustment of the charge injection and charge readout timing. With the described test environment, there is the capability to establish procedures for electrical tests, optical performance measurements, and methodology verification. One example of the latter is the sub-sampling methodology for signal reconstruction, which forms a key plank with fill-and-spill for in-orbit sensor quality validation.

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8. ACKNOWLEDGMENTS

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