Integration of Memristive Devices into a 130 nm CMOS Baseline Technology

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Abstract The two main features of the memristive devices which makes them the promising candidates for neuromorphic applications are low power consumption and CMOS compatibility. The monolithic integration of memristive devices with CMOS circuitry paves the way for in-memory computing. This chapter focuses on the factors governing the CMOS integration process. Firstly, the influence of CMOS baseline technology selection on the memristor module is briefly discussed. Secondly, the selection of metal level interconnects and their effect on the memristive device performance is explained. Further, the widely used deposition technique for the CMOS compatible memristive switching layers is presented. Finally, the implementation of the optimized process for the fabrication of the memristive module and its influence on the device performance is presented in terms of electrical characterization results.

Keywords CMOS compatibility · CMOS integration · Memristive devices · Pristine current · Resistive switching · Thermal budget · Encapsulation

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1   Introduction

The well know and widely used contemporary computer hardware architectures namely, von Neumann, Harvard, Graphics Processing units (GPU) etc.have their memory and logic fabricated in different process nodes [1, 2]. The scalability gap existing between logic and memory components is the main reason for their fabrication divergence. Such hardware configuration with separate memory and logic leads to a latency delay in moving the data between the two, which is called as von Neumann bottleneck (VNB) [3]. As a result, the throughput of the hardware architectures becomes limited and several approaches had been proposed to overcome this issue. However, a change of the hardware architecture become unavoidable to solve the VNB problem. Memristive devices can be easily fabricated in the complementary metal-oxide semiconductor (CMOS) baseline technologies which are used for the logic circuitry. This possibility of monolithic integration of memory and logic pave the way for the future in-memory computing hardware architectures [2].

Moreover, memristive devices are considered as one of the potential candidates in the field of neuromorphic and edge computing applications due to their fast switching, multi-level conduction, low power consumption, high scalability and CMOS compatibility [4]. In order to obtain a reliable and reproducible performance of memristive devices, integrating them with the CMOS transistors is very essential. Firstly, the transistor which is fabricated in series with the memristor, prevents the sneak path currents in case of memristive arrays by acting as a selector device [5]. Secondly, the transistor limits the current through the memristive devices by setting the current compliance with a specific gate voltage bias [6], thus preventing the hard breakdown of the devices. Finally, the integration of memristive devices with CMOS platform reduces undesired parasitics [7].

## 2   General Technological Aspects of Integrated Memristive Devices

In order to integrate the memristive module into the CMOS baseline technology, the below aspects need to be considered from the technology point of view:
- CMOS baseline technology node.
- Metal level selection in back-end-of-line (BEOL) interconnects.
- CMOS compatible memristive switching layer.
- Optimization of memristor module fabrication process steps.

2.1 CMOS Baseline Technology Node

The first step towards integrating the memristive devices with CMOS transistors is to choose a compatible CMOS baseline technology. The smaller the technology nodes, the lower the power consumption and the faster the resistive switching [8]. The size of the memristive devices integrated in the BEOL process can be scaled down to the size of 10×10 nm^2 [9]. However, scaling down the lateral dimension of the CMOS transistors is a challenge, due to the voltage levels required to perform the forming and reset operation [10, 11]. It is in the best interest of the memristive device applications to scale down the transistor size while maintaining a memory window of at least 10 [9]. In this work, the small transistors of gate length 130 nm and gate width 150 nm from the 130 nm CMOS baseline technology of IHP is chosen for memristive module integration. Figure 1a shows the transmission electron microscopy (TEM) cross section with energy dispersive X-ray (EDX) analysis of the 1T-1R integrated test structure.

In general, the memristive module consists of a metal-insulator-metal (MIM) stack as shown in Fig. 1a. The memristor module is integrated by using only one additional MIM mask as shown in the Fig. 1b. The dimensions of the via which comes on top of the memristive device in the BEOL interconnects, governs its dimensions. In general, the memristive device size has to be larger than the size of the via as shown in Fig. 1b. The contact to the top electrode of the memristive device is made through this via. Additionally, a predefined layout design rule 'enclosure' margin of memristive layer (MIM layer) with respect to the metal layer beneath (Enc.1 in Fig. 1b) and the via layer above (Enc.2 in Fig. 1b) has to be maintained. This enclosure margins are aimed to prevent possible dry etch related damages, obtain reliable contacts between the metal layers and to achieve reproducible process parameters over the entire wafer. The smallest possible size a memristor could take is the size of the via. In order to
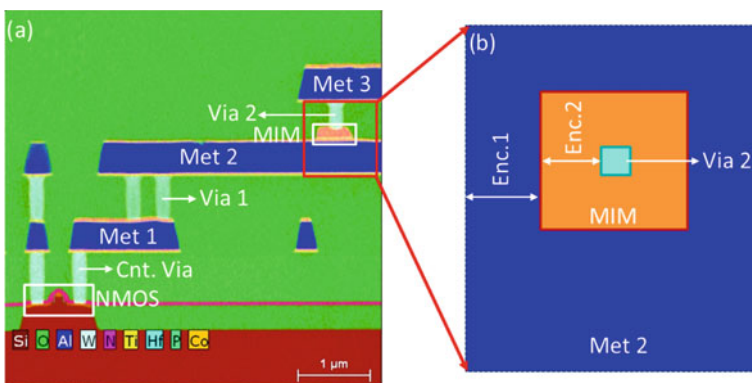
Fig. 1 **a** TEM cross section with EDX based chemical composition maps of memristive module integrated into a 130 nm CMOS technology of IHP and **b** topview layout design rules for the memristive module

reduce the size of the memristive device, intensive process developments are going on to fabricate the device on top of the via [12]. However, this approach of fabrication is out of the scope of this work.

2.2 Metal Level Selection in BEOL Interconnects

In order to have a better control over the performance of the memristive devices, it is important to fabricate them close to the transistor. However, it should not be placed so close that it affects the performance of the transistor. The memristor is a two terminal device and, in principle, the module could be placed between any two metal layers in the BEOL interconnects. We avoid to place the cell on Metal1 in order to maintain the normal functionality of the CMOS transistors and to reduce the undesired parasitic and substrate capacitance [13, 14]. The selection of the BEOL metal level for the integration of the memrsitive devices depends on the technology used for fabrication, field of application and the material used for the memristive switching layers [15–18]. Additionally, the desired thermal budget is one of the reasons behind choosing the specific metal level for the memristor module integration [19]. Further, the dimensions of the memristor devices and the allowed size of the via on top of the device according to the defined design rules in CMOS baseline technology also plays a role.

The BEOL thermal budget mainly consists of the thermal energy transferred to the wafer from the fabrication process steps including metallization, via-interconnect and inter layer dielectric (ILD) depositions. Additionally, the thermal budget consists of a forming gas passivation step in a diffusion anneal furnace towards the end of line (EOL) fabrication process at BEOL compatible temperature. The passivation step neutralizes the dangling bonds present at the interfaces and improves the contact between silicon and metal and thereby improving the electrical properties of the fabricated devices [20]. The thermal energy encountered by the memristor module is chosen carefully through the selection of the metal layer on which the module is fabricated [12]. The BEOL thermal budget steps activate the properties of the oxygen scavenging layer (OSL) present in the memristor module and thereby reduces the oxygen content in the memristor switching layer [21].

The thermal budget plays a significant role in selecting the phase of the memristive switching layer. The phase of the memristive layer illustrates the distribution of the oxygen vacancies and in turn the performance of the devices [22]. In polycrystalline layers, the oxygen vacancies are concentrated mainly at the grain boundaries whereas, they are homogenously distributed in amorphous layers [23]. The grain boundaries present in the polycrystalline memristive films results in higher device-to-device (D2D) variability. Whereas, the amorphous memristive films results in reduced D2D variability [24, 25].
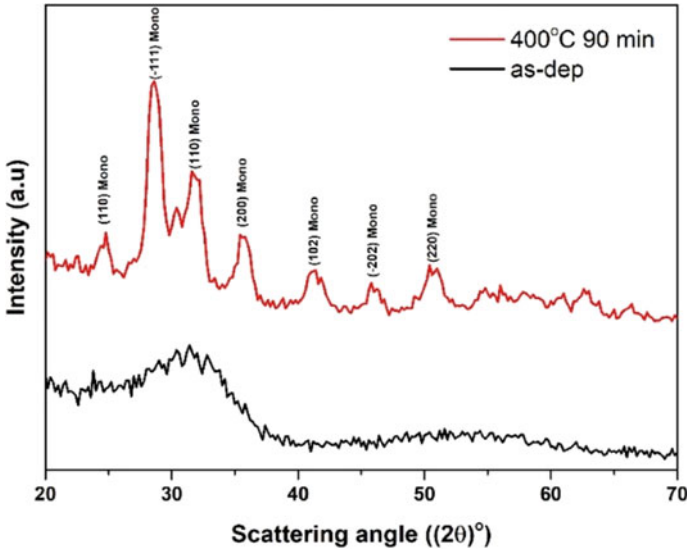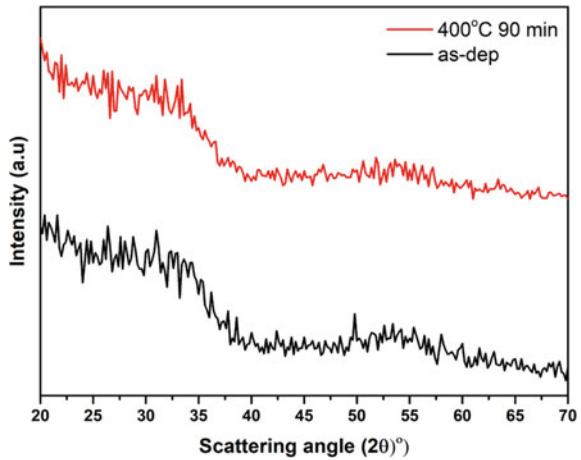
Fig. 2 XRD of as-deposited and sinter annealed HfO_2 layers

Fig. 3 XRD of as-deposited and sinter annealed Al doped HfO_2 layers

It can be clearly seen from the X-ray diffraction (XRD) patterns shown in Figs. 2 and 3 that the as-deposited layers of HfO_2 and Al doped HfO_2 are amorphous in nature. Both the layers were annealed at 400 °C for 90 m which is the BEOL thermal budget in 130 nm CMOS technology of IHP. The HfO_2 layers turns polycrystalline, whereas the Al doped HfO_2 stays amorphous after the annealing process.

2.3   CMOS Compatible Memristive Switching Layer

The successful integration of the memristive module into the CMOS baseline technology requires a CMOS compatible memristive switching layer. Several CMOS compatible memristive layers namely, TiO_2 [26], Al_2O_3 [27], SiO_2 [28], ZrO_2 [29], Ta_2O_5 [30], HfO_2 [31] etc. have been studied in the literature for various applications. Among others, HfO_2 is widely studied and used as a memristive switching layer due to its CMOS compatibility, simple precursor chemistries used for the deposition process, high dielectric constant and well developed deposition processes [32]. Along with the selection of the appropriate top and the bottom electrodes and their areas, the memristor stack configuration decides the type of switching behavior, namely, interface based switching or filamentary based switching [33–35]. The former is out of scope of this work.

Atomic layer deposition (ALD) is one of the prevalent methods used for the deposition of HfO_2 memristive layers. The deposition temperature is compatible with the BEOL thermal budget. The ALD process produces stoichiometric, highly uniform and conformal layers. The soft breakdown in a fully stoichiometric HfO_2 layer for the first time to create a conductive filament (CF) by using an inert metal electrode like TiN is almost impossible [36].Hence, an active metal electrode like Ti which has a high affinity towards oxygen needs to be deposited on top of the ALD HfO_2 layer. The Ti metal electrode acts as an oxygen scavenging layer (OSL) which scavenges the oxygen from HfO_2 layer during the electro-forming operation and thus enables the creation of a CF [37]. The CF can be disrupted and formed multiple times depending on the direction of the electric field applied. This determines the high resistance state (HRS) and low resistance state (LRS) of the device, respectively.

The HfO_2 memristive layer used in this work is deposited by using thermal atomic layer deposition (TALD) process at $300\,^{\circ}C$ in the Pulsar® module from ASM. The layers are grown by using a self-terminating reaction technique. The deposition takes place by alternate pulsing of $HfCl_4$ and H_2O precursors. Halide based precursors are preferred over the metal organic based precursors in order to reduce the impact of carbon atoms on the performance of the memristive devices [19]. Further, it is possible to incorporate the dopants into HfO_2 layers by replacing the Hf pulse with the dopant pulses at regular intervals. The doping percentage could be altered with the number of dopant pulses. Mostly, HfO_2 memristive layers are doped with Al atoms in order to keep the memristive layers in amorphous state due to the aforementioned benefits.

Finally, HfO_2 and Al_2O_3 layers could also be deposited in a stack without vacuum breakage. Initially, the Al_2O_3 layers of thickness 1 and 2 nm are deposited on the TiN metal layer by using Trimethylaluminum (TMA) and H_2O as precursors at $300\,^{\circ}C$. The deposition of Al_2O_3 is immediately followed by the HfO_2 deposition without vacuum breakage. The TEM cross section with EDX based chemical composition maps clearly shows the difference between the memristive layers with and without Al_2O_3 layers in Fig. 4. Substantial research is going on in the area of HfO_2 /Al_2O_3 bi-layer memristive devices. Addition of a thin Al_2O_3 layer below the HfO_2 layer has
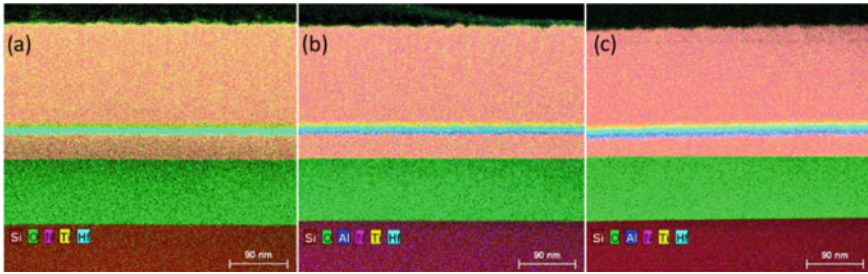
Fig. 4 EDX based chemical compositional maps of the memristor layers **a** HfO_2 **b** $HfO_2:Al_2O_3$ (8 nm: 1 nm) **c** $HfO_2:Al_2O_3$ (8 nm: 2 nm)

demonstrated an improved performance of the memristive devices in terms of HRS reliability [15, 38]. Further, the analog behavior is observed in the bi-layer memristive devices which improved the accuracy of pattern recognition in neuromorphic computing systems [39].

2.4 Optimization of Memristor Module Fabrication Process Steps

In spite of their low power consumption, fast switching, CMOS compatibility and many other potential features, the D2D and cycle-to-cycle (C2C) variability, reliability and performance of the memristive devices still remain a challenge [40]. Many approaches with respect to electrical characterization and fabrication technology, have been studied in the literature to reduce the variability and improve the performance of the devices. One of the ways is to program the memristive devices by using write and verify schemes like the incremental step pulse with verify algorithm (ISPVA) [41]. The small incremental voltage steps with read current operation in between allow the scheme to control the formation/disruption of the CF and hence result in reduced variability and supports the multi-bit operation [5]. Further, in terms of technology, the carbon content in the memristive layers is reduced by using inorganic precursors to obtain the promising results in case of D2D and C2C variabilities [19].

One of the ways to improve the memristive device performance from technology point of view is to optimize the device fabrication technique in the BEOL integration process. In this work, we use the $TiN/HfO_2/Ti/TiN$ memristive devices fabricated in the SiGe-BiCMOS technology of IHP to illustrate the three different fabrication approaches type 1, 2 and 3 and their impact on the electrical performance of the devices [42]. The memristor device stack consists of 150 nm sputter deposited TiN top electrode (TE) and bottom electrode (BE), 8 nm ALD deposited HfO_2 layer and 7 nm sputter deposited Ti on top of memristive HfO_2 layer. The reactive-ion etching
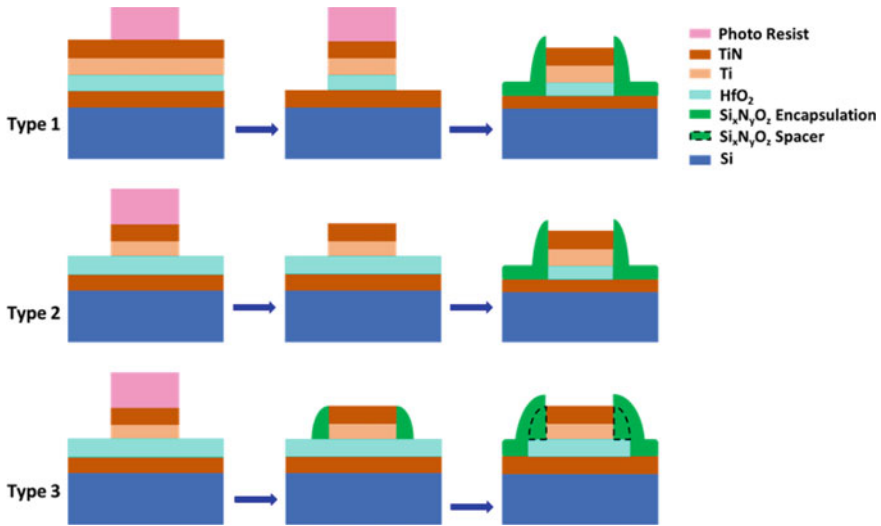
Fig. 5 Process flow of the memristive devices fabricated using three different approaches. Reprinted from [42] (License ID: 1252381-1; https://marketplace.copyright.com/)

(RIE) of the stack is one of the crucial steps in the memristive module integration. The RIE etching of the stack is challenging owing to the fact that, the stack consists of the Ti metal layer which could get oxidized during the subsequent process steps. Additionally, the etch residuals from the top electrode if prevail on the sidewalls of the devices degrade the performance of memristive devices [43, 44].

The process flow of the devices fabricated using three different fabrication approaches type 1, 2 and 3 are shown in the Fig. 5. In case of type 1 approach, the Ti/TiN and HfO_2 layers are RIE etched in one single step by using photoresist as the mask. In case of type 2 approach, only the Ti/TiN layers are etched by using photoresist as the mask. The HfO_2 layer is etched by using TiN as the hard mask. Type 3 approach follows similar process flow as type 2 until the Ti/TiN TE etch. However, the Ti/TiN layers in type 3 approach are covered with $Si_xN_yO_z$ spacers on the sidewalls before the HfO_2 memristor layer is etched. Finally, the devices fabricated in all the three approaches are encapsulated by depositing $Si_xN_yO_z$ layers. The RIE etch steps in all the three fabrication approaches are followed by a plasma ashing step and a wet etch step called neutral oxide etch (NOE) which removes the etching residuals and polymer impurities from the wafer surfaces, respectively. Further, in case of type 1 approach, due to the patterning of HfO_2 layer using photoresist, the residuals of the resist prevail even after the ash and NOE clean steps. Hence, an oxygen RIE plasma step is carried out after the memristor layer etch, which removes the residual resist and thereby assists the subsequent ash and NOE clean steps [45].

The performance of the memristor devices is tested initially on the dedicated process control monitor (PCM) structure as shown in Fig. 6a. The PCM structure consists of 2457 memristor devices of size $10 \times 10 \ \mu m^2$ connected in parallel.
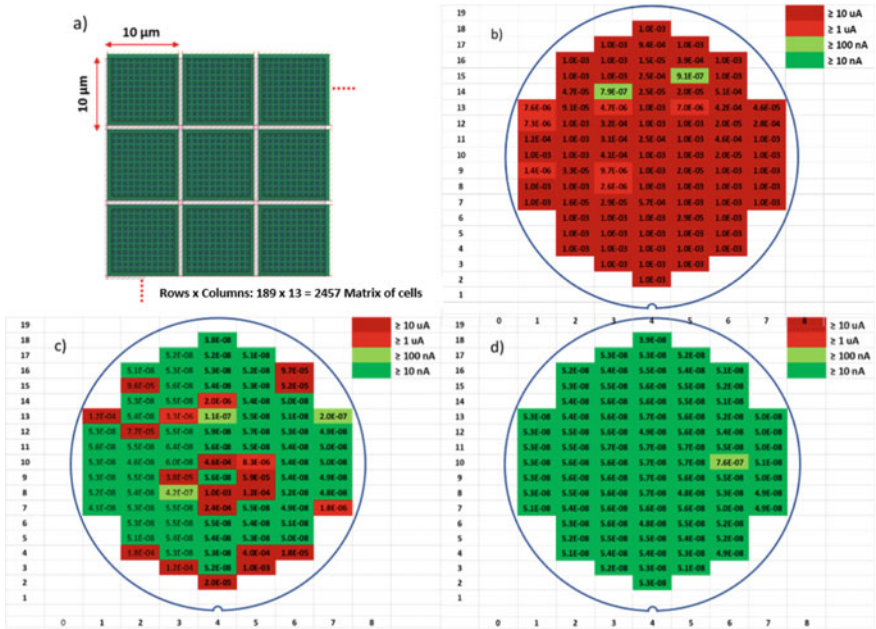
Fig. 6 The pristine state currents measured on **a** a dedicated PCM structure of memristive module fabricated using **b** type 1 **c** type 2 and **d** type 3 approaches. Reprinted from [42] (License ID: 1252381-1; https://marketplace.copyright.com/)

The structure demonstrates sensitive device topologies with 9828 corners and 98,280 µm of perimeter. Further, the quality of the memristor devices, edge patterning and their electrical performance could be checked from the in-line tester measurements inside fab. In case of out-of-spec electrical results, the memristor fabrication process steps could be reworked.

The pristine state currents of the memristive devices can be considered as a direct manifestation of their switching performance. The wafer-scale level pristine state currents of the memristive devices fabricated using three different approaches are as shown in the Fig. 6. The pristine state currents are measured at a voltage of 0.1 V. It is clearly shown that the devices fabricated in type 3 approach using the spacers and encapsulation techniques exhibit lower pristine state currents compared to the memristive devices fabricated in type 1 and 2 approach [42].

The equivalent circuit of a memristor always consists of a resistor and a capacitor in parallel, to account for the parasitic losses [7]. The parallel resistor in this case is the side walls of the memristor device. In contrast to type 1 and 2 devices, the type 3 devices have their side walls of the TE protected by $Si_xN_yO_z$ spacers before etching the HfO_2 layer. Due to this, the possibility of Ti containing polymers reaching the side walls of the memristive devices is considerably reduced. Hence, the value of parallel resistance is kept high which eventually results in low leakage current values in type 3 devices [42].
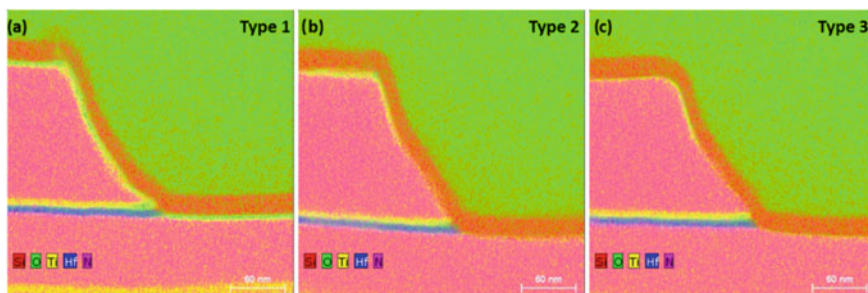
Fig. 7 TEM cross section with EDX analysis of the side walls of the memristive devices fabricated using **a** type 1, **b** type 2 and **c** type 3 approaches. Reprinted from [42] (License ID: 1252381-1; https://marketplace.copyright.com/)

Fig. 8 The MW extracted from the 1st and 50th set cycles of memristive devices fabricated using three different approaches. Reprinted from [42] (License ID: 1252381-1; https://marketplace.copyright.com/)
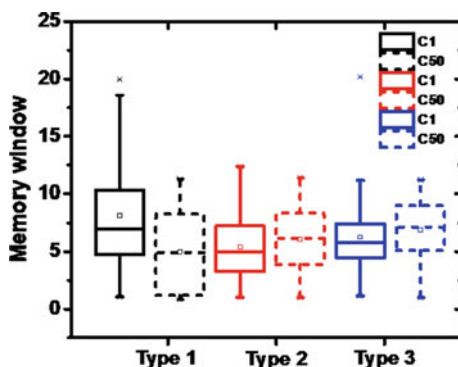
Further, to analyze the effect of three different fabrication approaches on the elemental composition of the memristive stack, TEM cross section with EDX based chemical composition analysis is performed (Fig. 7). Memristive devices of size 75 $\times$ 75 μm^2 are chosen for the analysis. In case of type 1 devices, Ti is oxidized at the side walls and there is a formation of $Ti_xO_yN_z$ on the top and bottom electrodes. The oxygen RIE plasma step which assists the removal of residual resist, might possibly have caused this oxidation. The type 2 devices show the formation of $Ti_xO_yN_z$ mainly on the TE, while it is considerably reduced in case of type 3 devices. Differentiating between the spacer and the encapsulation layers is hard due to the usage of the same material and the RIE etching angles. Even though, it is hard to notice the Ti impurities on the side walls of the devices, the electrical measurement results support the claim [42].

The 75 $\times$ 75 μm^2 memristor devices are further characterized for their resistive switching operation. The type 3 devices exhibited less variability in terms of forming, reset and set voltages. The devices are cycled for 50 cycles of reset and set operations. The memory window (MW) of the devices is extracted from the 50 set cycles. It can be clearly noticed from the Fig. 8 that the MW decreases with cycling in type 1

devices while it increases in type 2 and 3 devices. Further, the type 3 devices show slightly higher MW with less variability compared to type 1 and 2 devices [42].

3 Conclusion

The necessity and importance of memristive device integration into a CMOS baseline technology is discussed. The technological aspects of memristive module integration are presented under four different sections: (1) CMOS baseline technology (2) Metal level selection in BEOL interconnects (3) CMOS compatible memristive switching layer (4) Optimization of memristor module fabrication process steps. Under the first section, the factors governing the size of the memristive devices and, the layout design rules for the memristive module integration are briefly discussed. In the second section, the metal level selection in terms of CMOS performance and thermal budget of the BEOL processes is presented. Additionally, the phase of the memristive switching layers and their influence on the performance of the devices in terms of D2D and C2C variability is presented. In the third section, the ALD and the reason behind its wide usage as a memristive layer deposition process is briefly discussed. In the fourth section, the memristor module is fabricated using three different approaches. The optimized fabrication process steps are studied systematically in terms of TEM cross section with EDX based chemical analysis and correlated with the device performances. The devices fabricated using type 3 approach with spacer and encapsulation technique exhibited lower pristine state currents on a wafer scale analysis. Finally, the extracted MW of type 3 devices exhibited higher values with slightly less variability in comparison with type 1 and type 2 devices.

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