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SiGe HBTs and BiCMOS Technology for Present and Future Millimeter-Wave Systems

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ABSTRACT This paper gives an overall picture from BiCMOS technologies up to THz systems integration, which were developed in the European Research project TARANTO. The European high performance BiCMOS technology platforms are presented, which have special advantages for addressing applications in the submillimeter-wave and THz range. The status of the technology process is reviewed and the integration challenges are examined. A detailed discussion on millimeter-wave characterization and modeling is given with emphasis on harmonic distortion analysis, power and noise figure measurements up to 190 GHz and 325 GHz respectively and S-parameter measurements up to 500 GHz. The results of electrical compact models of active (HBTs) and passive components are presented together with benchmark circuit blocks for model verification. BiCMOS-enabled systems and applications with focus on future wireless communication systems and high-speed optical transmission systems up to resulting net data rates of 1.55 Tbit/s are presented.

INDEX TERMS Heterojunction bipolar transistors (HBTs), high-frequency measurements, millimeter wave, SiGe, technologies, terahertz, modeling, wireless communication systems, high-speed optical transmission system.

I. INTRODUCTION

The COVID-19 crises taught us that performant communication systems for widespread use of home office, video conferences, etc. are of utmost importance for keeping economy alive, even under shutdown conditions. Furthermore, the notion of resilience is gaining importance in the political sphere and is currently resonating with the general public due to the COVID-19 crisis. Mastering the value chain of the territory's

strategic sectors such as the communication system is an important issue, at least at the European level.

The actually running European Research project TARANTO [1] already addresses this concern. In fact, this project aimed at the establishment of the next BiCMOS technology platforms with improved SiGe Heterojunction Bipolar Transistor (HBT) performances and Higher Integration level needed to address High Speed & High Data Rate communication systems. High performance BiCMOS technology platforms are the key enabler of those applications which require the combination of high-performance radio-frequency (RF) front-ends with the high computational power and low power consumption of advanced CMOS nodes. The ever increasing demand for the transmission of high data rates for smart communication systems, with data-processing needed close to the front-ends calls for RF front-ends with ever higher operating frequencies (>100 GHz), high bandwidth, low noise, high linearity and sufficient output power in the millimeter-wave (mmW) range, combined with improved power-added efficiency (PAE). Also a high performance computation power is needed for data conditioning, close to the RF front-end. The superior high-frequency performance of SiGe HBTs facilitates the integration of these RF functionalities on smart electronic chips with a performance that is not in reach of even most advanced pure CMOS technologies in the near future, while the combination of HBTs and CMOS allows the right combination of analog and digital performance. TARANTO thus further strengthens the leading position of the European semiconductor industry in SiGe BiCMOS technology (this position is actually tackled by the DARPA funded research project T-Music [2]). It provides a solid industrial base for the development of new products in areas such as telecommunications, home electronics, and car electronics which are of key importance for Europe's high-tech industries.

This paper will summarize the main findings of the TARANTO project. It is organized as follows. Section II is devoted to technology and gives an overview of SiGe HBT development and BiCMOS process integration at the European level. Section III is dedicated to mmW characterization and modeling. Power measurement up to 190 GHz and NF-measurement up to 325 GHz are addressed as well as S-parameter measurements up to 500 GHz. The harmonic distortion of high speed SiGe HBTs are analyzed and the modeling and design of passive devices are presented. Finally benchmark circuit blocks for model verification close this section. The section IV presents BiCMOS-enabled systems and applications with focus on future wireless communication systems and high-speed optical transmission systems.

II. SIGE HBT DEVELOPMENT AND BICMOS PROCESS INTEGRATION

Today, the most advanced industrial processes in production offer transit frequencies f_T up to 300 GHz and maximum oscillations frequencies f_{MAX} close to 400 GHz [3]–[6]. The highest reported f_{MAX} for a SiGe HBT is 720 GHz in a bipolar only process [7]. This demonstrates that significant improvements for future industrial processes can be expected, if the concepts to improve the RF-properties of the SiGe HBTs used in [7] can also be applied for next generation BiCMOS production technologies. The aim of the TARANTO project for the industrial partners Infineon and STMicroelectronics is the development of next generation BiCMOS technology platforms with SiGe HBTs reaching f_{MAX} values of 500 to 600 GHz. The goal of IHP is to demonstrate, that the record SiGe HBT performance of [7] is also possible in a BiCMOS flow, which is compatible to the needs of industrial mass production. Based on their experience form previous technologies, the approaches to achieve a high f_{MAX} differ in detail for the partners. However, there is one common feature of all concepts: the use of a mono-crystalline base link between intrinsic SiGe base and the external base electrode to minimize the base resistance of the SiGe HBTs. The next sections briefly describe the different concepts of IHP, Infineon and STMicroelectronics for SiGe HBT optimization and the RF-performance achieved up to now.

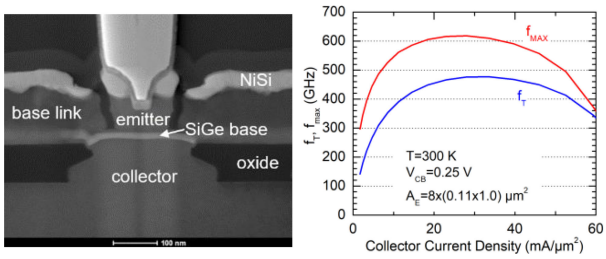

FIGURE 1. TEM cross-section of an EEB NSEG SiGe HBT with 110 nm emitter width in 130 nm BiCMOS process (left) and measured f_T/f_{MAX} vs. collector current density (right).

A. HIGH-SPEED SiGe HBTS OF IHP

IHP has investigated various device concepts for SiGe HBTs with respect to their potential for highest RF performance. The fastest devices were achieved in a process with non-selective epitaxial growth (NSEG) of the SiGe base and elevated extrinsic base (EEB) regions formed in a separate selective epitaxial process. Optimization of this device concept in a bipolar-only process flow resulted in the demonstration of peak f_T/f_{MAX} values of 505 GHz/720 GHz and ring oscillator gate delays of 1.34ps which are best values reported for SiGe HBTs so far [7]. The challenges of realizing this performance level in a BiCMOS process include the adaptation of the HBT to the thermal constraints of the CMOS process. Moreover, a NiSi process with low sheet resistance and low contact resistance to base and emitter was developed that is compatible with the 130 nm baseline CMOS process. As an intermediate result, HBTs with peak f_T/f_{MAX} values of 470 GHz/610 GHz have been demonstrated in the BiCMOS process (Fig. 1) [8].

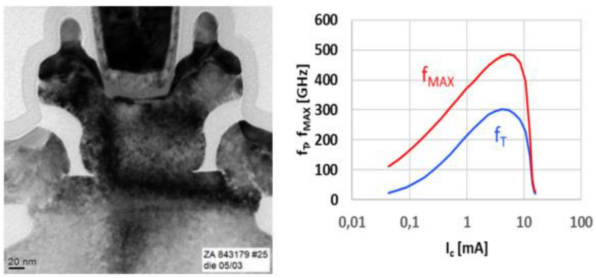

FIGURE 2. TEM cross-section of an EBL SEG SiGe HBT in 90 nm BiCMOS flow (left) and measured RF-performance as function of collector current (right). Emitter area is 120 nm x 2.73 μm.

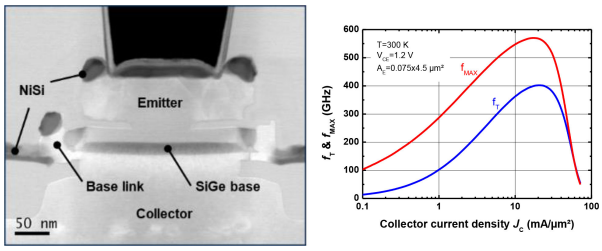

FIGURE 3. TEM cross-section of the EXBIC SiGe HBT in 55 nm BiCMOS flow (left) and tentative RF-performance from SPICE models based on TCAD (right).

B. COMMON SiGe HBT DEVELOPMENT OF IHP AND INFINEON

While the double-polysilicon self-aligned (DPSA) device concept with selective epitaxial grow (SEG) is widely used in current industrial BiCMOS platforms further performance enhancement beyond 400 GHz f_{MAX} turned out to be very difficult in this architecture. Its primary drawback is that extrinsic-to-intrinsic base link and intrinsic base are formed simultaneously and cannot be decoupled. In an attempt to overcome this limitation, a separate epitaxial step was introduced for the formation of the base link [9]. This partially mono-crystalline epitaxial base link (EBL) has facilitated a significant reduction of the extrinsic base resistance. The applicability of this new concept in an industrial BiCMOS environment has been studied in joint fabrication runs of IHP and Infineon where IHP processed the EBL HBT module and Infineon the collector module, deep and shallow trench isolation, CMOS and metallization [10]. EBL HBTs of this joint process flow demonstrated f_{MAX} values up to 575 GHz indicating a significant performance advantage over the classical DPSA concept.

C. INDUSTRIAL SiGe BICMOS PLATFORM DEVELOPMENT AT INFINEON

Starting point for the development at Infineon was the production technology B11HFC with a 370 GHz f_{MAX} SiGe HBT integrated in a 130 nm CMOS platform [4]. To achieve the performance target for the next generation B12HFC, Infineon replaced the double-polysilicon self-aligned device configuration used in B11HFC by the SEG EBL concept invented by IHP [9]. The results from common wafer runs to transfer this concept from IHP to Infineon are shown in the previous section. As a first step to fabricate the SEG EBL device in its own fabrication lines, Infineon developed the necessary unit process steps and integrated the device in its 130 nm platform used for B11HFC. The details of this work are described in [11]. In a next step the transition from the 130 nm CMOS node to the more advanced 90 nm was done. The result can be seen in Fig. 2, which shows a TEM cross-section of the SiGe HBT and the measured f_T and f_{MAX}, which are 300 GHz and 480 GHz, respectively. To close the performance-gap compared to the results shown in the previous section, further lateral scaling and an improved doping of the base link epitaxy will be evaluated.

D. INDUSTRIAL SiGe BiCMOS PLATFORM DEVELOPMENT AT STMICROELECTRONICS

Developments at STMicroelectronics started from the 55-nm BiCMOS platform currently in production, which high-speed SiGe HBT features 320 GHz f_T and 370 GHz f_{MAX} [3]. Final objective is to offer a 400 GHz f_T / 600 GHz f_{MAX} HBT on same CMOS node. Three major process changes are implemented to reach this objective. The first one is the modification of the process thermal budget with the reduction of the spike annealing temperature and the addition of a millisecond annealing. It allows to increase the f_T of the SiGe HBT thanks to a reduction of dopants diffusion and a better activation of these dopants. Process conditions have also been defined in order to not degrade the performances of CMOS transistors [12]. The second change applies to the extrinsic collector module with the replacement of the buried layer by an implanted collector [13], which reduces both the cost and the cycle time of the technology. A Super Shallow Trench Isolation (SSTI) is implemented to reduce the base-collector capacitance. Finally, a STMicroelectronics proprietary SiGe HBT architecture, called EXBIC (for Epitaxial eXtrinsic Base Isolated from the Collector) [14], is being developed to address the f_{MAX} challenge. The key feature of this architecture, common to the IHP and Infineon ones, is a boron in-situ doped epitaxial base link used to reduce the extrinsic base resistance. As shown on Fig. 3, targeted SiGe HBT architecture is now available on silicon but electrical results are not reaching yet the simulated ones.

III. MILLIMETER-WAVE CHARACTERIZATION AND MODELLING

A. POWER AND NOISE MEASUREMENTS BEYOND 100 GHZ

1) NOISE MEASUREMENTS UP TO 325 GHZ

In high frequency (HF) applications the noise level is of major importance to ensure good performance of integrated devices. The noise performance of a device is characterized by the noise figure (NF) along with the other noise parameters. For this purpose, high frequency noise measurement (>110 GHz) are crucial for the characterization of integrated circuit

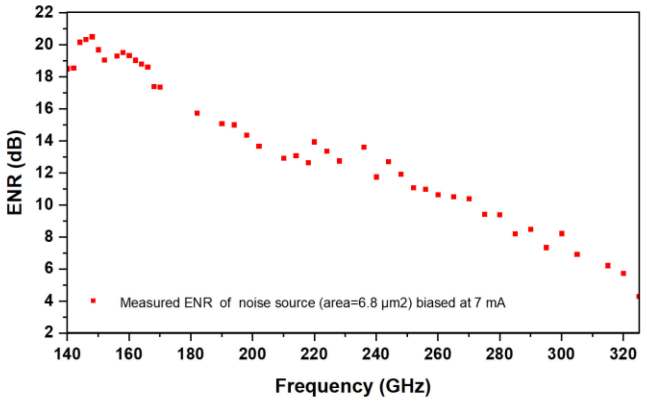

FIGURE 4. Measured ENR value of the noise source (area = 6.8 μm^2) at 7 mA in the frequency range 130-325 GHz.

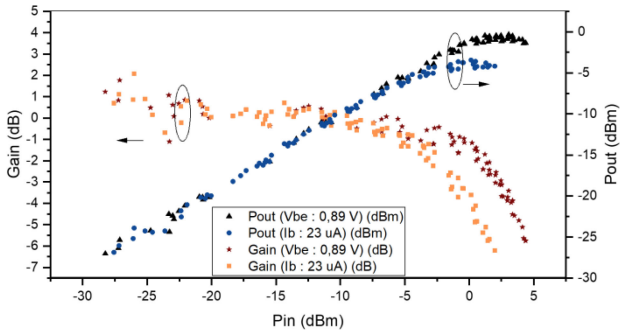

FIGURE 5. Power measurements of HBT SiGe:C (Le = 5.56 μm – We = 0.2 μm – Ne = 1) @ 191 GHz under 50 Ω.

designs in the mmW range. Among important issues for noise characterization at such high frequency range is the commercial availability of the noise source [15]. Thus, a HF noise source with an adequate output noise power level is required to perform such characterization. For this purpose, a new integrated silicon based diode noise source using the STMicroelectronics SiGe BiCMOS 55 nm technology was developed.

Noise sources are usually characterized in terms of the Excess Noise Ratio (ENR), which is defined as the generated noise level above the thermal noise floor. A noise measurement setup was reported consisting of a silicon-based diode noise source, a noise receiver and a noise figure meter (NFM) [15], [16]. The output noise power of the diode was measured in two states; P_{hoc} when the diode source is reverse biased near the avalanche region, and P_{cold} when the diode source is in the OFF state. After extracting the noise figure of the noise receiver using cryogenic Hot/Cold measurements [15], [16], the Excess noise ratio of the noise source was then extracted using Y-method. The integrated diode noise source achieved a tunable ENR level up to 20 dB in the 130 GHz to 325 GHz frequency range as shown in Fig. 4.

To test the potentiality of the noise measurements setup, the ENR was extracted for several biasing currents (1 mA up to 7 mA) for several diode sizes as described in [16]. Moreover, the noise source was used to extract the NF of active devices (Packaged LNA) up to 260 GHz [15]. Beyond this initial proof of concept of silicon-noise source the electrical model of this noise source was also developed in [16].

2) POWER MEASUREMENTS UP TO 191 GHZ

The need of power characterization of active devices at mmW range can be easily understood by the increasing and rapid evolution of technologies that target high frequencies [17]. Because of this evolution, development of new test benches is required to implement nonlinear accurate models of the new components.

Following previous work of a complete integrated load-pull solution on silicon [18], the use of an external source seems to be more useful to provide more flexibility for on-wafer measurement of active components covering the frequency range from 185 to 191 GHz. However, the tuner used to synthetize the different loads at the output of the active DUT (Device Under Test) must be always integrated with the DUT at such high frequencies to avoid the probe losses and hence increase the Smith chart area covered. This new test bench can measure injected and reflected power to determine the non-linear $|S_{11}|$ parameter. The procedure was to perform a waveguide calibration to validate offset power plans. The accuracy was estimated after measuring a known device and analyzing standing wave phenomena inside the cavity of the coupler used inside the setup. Then, an ISS (Impedance Standard Substrate) kit is used to calibrate the measurement planes at the input of the on-wafer DUT, which means to consider the probe losses. A well-known integrated tuner has been measured to prove the high versatility of this test bench [19].

Power measurement between 185 and 191 GHz of HBT SiGe:C from STMicroelectronics under 50 Ω is thus achieved. The power gain (GP) value measured at low power is validated by comparing |S21| dB value, obtained with the VNA. Voltage-controlled and current-controlled DUT shows notable differences. This has been made measurable thanks to the high dynamic range of the power source and detectors that are able to reach the non-linear region of the DUT. Power measurements of an HBT at 191 GHz are shown on Fig. 5 for two bias points (constant V_{BE} and constant I_B).

Design of integrated tuners are ongoing to obtain a full load-pull setup. Final objective is the validation of power features of the new generations of HBT SiGe:C in sub mmW range.

B. S-PARAMETER MEASUREMENT UP TO 500 GHZ

To enable integrated circuit design in the millimeter and sub-millimeter-wave ranges, accurate device characterization at such high frequencies becomes indispensable. After demonstration for InP HBT characterization up to 750 GHz in [20], SiGe HBT characterization was demonstrated up to 500 GHz in [21] using an on-wafer TRL calibration kit design and de-embedding test structures at the transistor's terminals at the lowest metal layer of the complex BiCMOS Back-End-Of-Line (BEOL). However, as discussed in [21], achieving

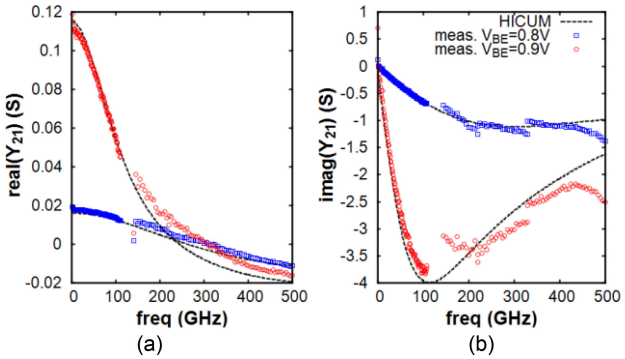

FIGURE 6. Comparison between compact model and measurement up to 500 GHz: (a) real part and (b) imaginary part of Y21 versus frequency for 0.09x4.8 μm² SiGe HBT from STMicroelectronics at $V_{CB} = 0V$.

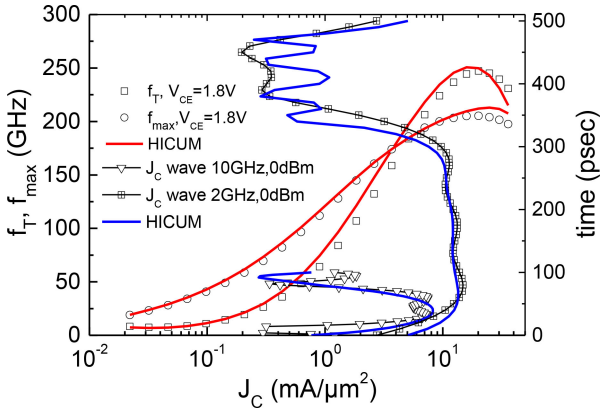

FIGURE 7. Current gain cut-off frequency f_T and maximum oscillation frequency f_{MAX} at $V_{CE} = 1.8$ V and output current density waves at quiescent $V_{BE} = 0.85$ V of incident frequency at 2 and 10 GHz.

band continuity within four frequency measurement ranges is a difficult task for device characterization. The main issues are contact deterioration due to multiple contacts on the same pads (at least one contact for each frequency band), possible probe misalignment and the appropriate design of the TRL calibration structures for on-wafer calibration.

For transistor's modelling purpose, parameter Y_{21} is particularly important since easy to correlate to the small-signal equivalent circuit parameters, such as transconductance g_m. The measured and simulated Y_{21} results up to 500 GHz are depicted in Fig. 6. The transistor under test is a BiCMOS 55 nm 0.09 × 4.8 μm² SiGe HBT from STMicroelectronics [3], featuring f_T/f_{MAX} of 315/350 GHz at $V_{CB} = 0V$ [22]. A quite good continuity between the four measurement frequency bands can be observed. The HICUM compact model parameters were extracted for this transistor. This model accurately reproduces the device's behavior up to 400 GHz. Beyond 400 GHz, agreement is not achieved between measurement and simulation. This is due to different reasons:

- The limitation of the TRL calibration method which does not correct for the coupling between probes and substrate.
- The different backprobe environment for DUT and calibration standards can no more be represented by one error term only [23].
- The lumped element method applied for de-embedding hits its limits at these high frequencies.
- Non-quasi-static (NQS) effects rising at frequencies superior to fT (∼300 GHz) need to be carefully modelled in HICUM. For that, accurate measurements above 300 GHz are needed.

C. HARMONIC DISTORTION OF HIGH SPEED SiGe HBTS

1) POWER AMPLIFIER CONSIDERATIONS

Advances of SiGe HBT performance [10], [24], [25] enabled realization of high frequency power amplification with stacked high speed power amplifiers (PA), transmitters and MIMO radars [26]–[30]. The most important component in RF transceiver is the power amplifier. It consists of an array of power-cells, which correspond to multi-finger transistors, connected in parallel. Interconnections significantly determine the performance of the PA such as power added efficiency (*PAE*), output power (P_{out}) and transducer power gain (G_T) [27]. For the increase of P_{out} due to limited BV_{CEO} in high speed SiGe HBT, more than one device can be combined in parallel. This results in an increase of the current and conditionally extends P_{out}. The condition comes from the 50Ω load connected at the terminal of the power-cell and substrate technology defined bias limit due to the substrate breakdown voltage [31]. This sets a limit on a number of transistors in parallel. To increase P_{out} for high speed HBTs with relatively low $BV_{\text{CEO}} = 1.7$V, V_{CE} can be improved using cascode configuration (common emitter CE and common base CB), exploiting concept of voltage scaling instead of current scaling. The number of cascoded HBTs is limited by the substrate breakdown voltage. Collector current and voltage clipping of PA will be reduced for parallel SiGe HBTs in cascode connection. Therefore, it is important to investigate harmonic distortion (HD) in HF HBTs with CE and CB configurations. In this work we will focus on investigation and modeling of HD of optimized to HF power cell in CE configuration.

2) RESULTS AND DISCUSSION

For compact model verification under large-signal conditions, harmonic distortion in 50Ω system was investigated in frequency and time domain using nonlinear network analyzer N5247B. For many applications, the 3rd harmonic power is the most relevant, but for capturing the large-signal time domain behavior five harmonics are typically required. Fig. 7 shows a superposition of the f_T and f_{MAX} together with transient collector current density data over a single period of a 2 GHz and 10 GHz input signal with a quiescent bias of (V_{BE}, V_{CE}) (0.85, 1.8) V. The transient data indicate the operating range of the transistor under large-signal conditions. Wave ripples in V_{BE} are due to only five available measured harmonics during Fourier transformation from frequency domain as could be shown using the compact model with more harmonics.

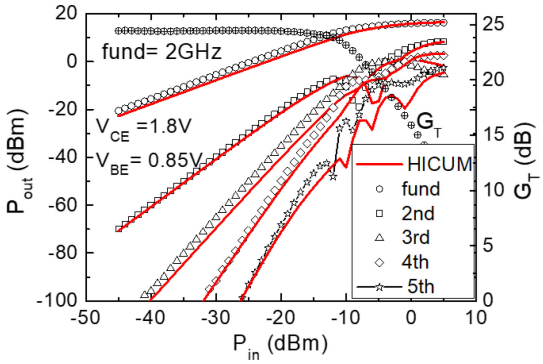

FIGURE 8. Output power and all 5 harmonics at fundamental frequency of 2 GHz and G_T (P_{in}) at V_{CE} = 1.8 V. Symbols represent measured data and lines are HICUM. CBEBEBCx2 CE power cell with emitter area of 0.13 μm × 10.16 μm × 2. [30], [31].

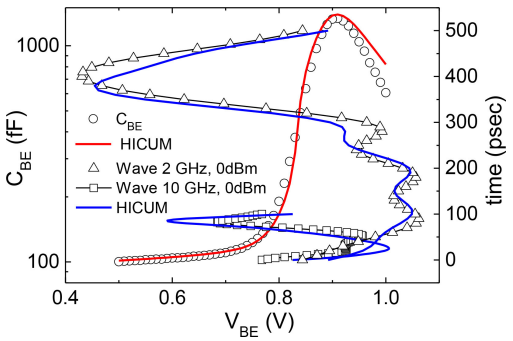

FIGURE 9. C_{BE} dependence on V_{BE} and overlaid V_{BE} waves.

Fig. 8 displays the measured output power of a power cell versus input power. The compact model agrees quite well for the measured five harmonics, making it suitable for large-signal high-frequency applications. P_{out} is linear up to $P_{in} = -10$ dBm. 1 dB compression point is −7dBm at 2 GHz of input power. There are six well known main sources of distortion in HBTs related to: $I_B(V_{BE})$, $I_C(V_{BE}, V_{BC})$, $I_{CB}(V_{BE}, V_{CB})$, $C_{BC}(V_{BC})$, $C_{BE}(V_{BE})$, $C_{SC}(V_{SC})$. Compact model based harmonic distortion analysis show that the dominant non-linearity sources beyond −10 dBm of input power in investigated SiGe power-cells are related to diffusion capacitance non-linearities $C_{BE}(V_{BE})$, see Fig. 9 and $C_{BC}(V_{BE})$ (not shown here) as well as $I_B(V_{BE})$ and $I_C(V_{BE}, V_{BC})$ non-linearity [31]. The frequency dependence of dynamic base and collector currents was observed. Compact model simulations show that at quiescent $V_{CE} = 1.8$V avalanche multiplication nonlinearity impact on P_{out} and harmonic distortion is not dominant [31], [32]. Compact model shows very good agreement for large signal data including time domain results.

D. PASSIVE DEVICES MODELLING AND DESIGN

Modern SiGe BiCMOS technologies, thanks to the MOS and HBT transistors, allow the integration of high-performance RF modules together with low-cost silicon-based logic and

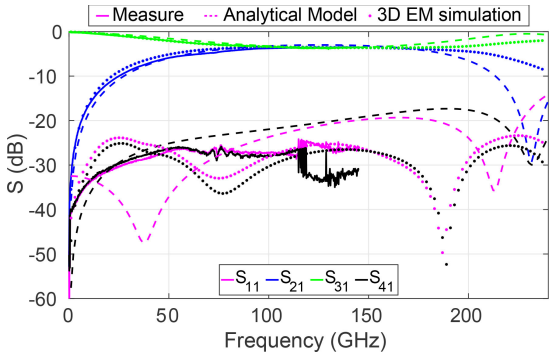

FIGURE 10. S-parameters of the 3-dB Coupler. Measurement (solid-lines), the analytical model (dashed lines) and the 3D EM simulation results (dots).

control systems on a single die. However, the performance of high-frequency RF systems is also largely determined by the performance of the passive devices of which they are composed. In this context, the design of passive structures with a high-quality factor (Q-factor) is a topic of major interest. Two conditions are necessary to reach this goal: (i) an adapted BEOL and (ii) high-performance architectures. The first condition is achieved by BEOLs with a relatively great height and featuring, at least, a thick metal, as the STMicroelectronics 55-nm BiCMOS technology [3]. On the other hand, the second condition can be achieved, for example, through the use of structures with the so-called slow-wave concept [33]. Nevertheless, the modelling of these structures (e.g., slow-wave CoPlanar Waveguides, S-CPWs, and its derivates) is not free of shortcomings due to the increased complexity, as compared to classical structures such as microstrip lines.

To overcome this issue, a first electrical model describing the behavior of the S-CPWs was proposed in [34] and subsequently improved in [35]. The latter also included a detailed methodology for analytically calculating the capacitances that make up the model. The slow-wave concept was then extended to more complex structures such as the Coupled Slow-wave CoPlanar Waveguides (CS-CPWs) [36]. To derive the electrical model of these complex structures, the capacitance calculation methodology presented in [35] was merged together with the resistance and inductance calculation proposed in [37], leading to a completely parametrical model for CS-CPWs [38].

Fig. 10 presents the S-parameters of a 3-dB coupler designed in the STMicroelectronics 55-nm BiCMOS technology. Measurements were carried out from 1 GHz to 145 GHz, and 3D EM simulations and analytical model simulations from 1 GHz to 240 GHz. The three datasets show remarkable agreement. In addition, the 3-dB coupler reports high performance thanks to the slow-wave concept, with measurements showing a return-loss and isolation greater than 20 dB throughout the whole considered frequency band, and a coupling insertion loss of 3.6 dB together with at the through port insertion loss of 3.7 dB. These results correspond to the state-of-the-art.

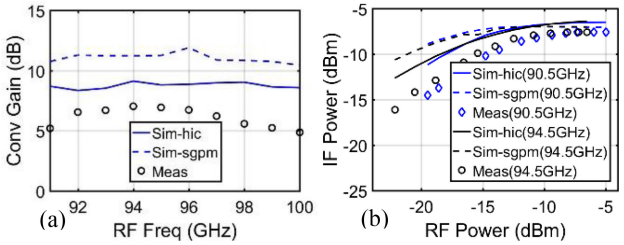

FIGURE 11. **(a) Conversion gain and (b) IF output power of the mixer as function of RF input power. Comparison between measurement (symbols) and simulation (lines) using two different transistor models.**

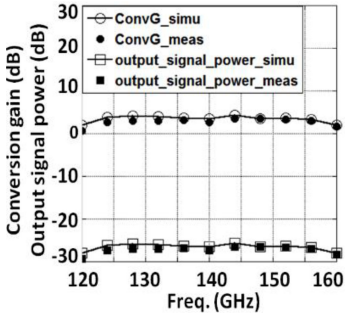

FIGURE 12. **Measured versus simulated conversion gain and output signal power of the quadruple frequency multiplier.**

E. BENCHMARK CIRCUIT BLOCKS FOR MODEL VERIFICATION

The increasing demand for mm-wave and sub-mm-wave, i.e., high frequency (HF) applications has been the main driving force behind the recent progress in SiGe:C HBT BiCMOS technology. Requirements such as high bandwidth and long battery life for mobile devices have led to the pursuit of low-power HF front-ends. Advanced SiGe HBTs have become attractive candidates here since they enable a significant reduction in power consumption due to (i) their high operating frequencies in saturation, i.e., at forward biased base-collector junction, and (ii) their integration with digital CMOS [24], [39].

Efficient high-frequency circuit design relies on accurate models for active and passive devices. Their verification beyond the device level has been pursued by designing basic HF circuit building blocks with a relatively low device count and the following goals in mind:

i) Verification of models under a variety of realistic circuit operating conditions;
ii) Identification of model shortcomings as early as possible in a process development stage;
iii) Performance evaluation of the process technology in terms of its suitability for target applications.

Several benchmark circuits have been designed [40]–[43]. The results of two circuits will be briefly discussed below.

1) W-BAND LOW-POWER MMW DIRECT DOWN CONVERTER

A low-power mixer was designed with HBTs operating in the saturation region. Standard Gilbert cell topology was used and both mixing quad and transconductance pair are biased with 0.7 V supply voltage which is accomplished by using a transformer to couple the transconductance and switching stage. The mixer provides more than 5 dB conversion gain within a 9 GHz (i.e., 91–100 GHz) wide frequency band. The overall DC power consumption of the mixer is only 21.8 mW. Fig. 11 shows the performance of the mixer. Details of the work can be found in [41].

2) LOW-POWER 120–160 GHZ ACTIVE FREQUENCY QUADRUPLER

The low-power frequency quadrupler consists of two doublers, each based on a double-balanced Gilbert cell mixer and a common-emitter single-stage power amplifier, which are cascaded via a power splitter. The quadrupler provides a conversion gain of 4 dB and output power of −26 dBm over the frequency range from 120–160 GHz.

The entire circuit, including output buffer stages and power amplifiers, consumes just 230 mW DC power. As shown in Fig. 12, excellent agreement is observed between measurement and simulation.

IV. BiCMOS-ENABLED SYSTEMS AND APPLICATIONS

A. FUTURE WIRELESS COMMUNICATION SYSTEMS

1) FRONTHAULING AND LAST MILE

Introducing mmW technologies in the 5th generation of wireless communication systems (“5G”) enables the development of cost efficient high bitrate fixed wireless access (FWA) solutions offering up to several 100 Mbit/s to e.g., private homes and offices and avoiding costly deployment of fiber infrastructure. At this, network planning and deployment need to consider the specific propagation characteristics of mmW radiation, which are mainly characterized by the need for line of sight (LoS) links and a limited reach spanning several 100 m in typical deployment scenarios. In such scenarios, introduction of mmW repeaters can bring significant coverage improvement at low costs [44]. Unlike solutions based on Integrated Access and Backhauling (IAB) technologies, repeaters offer highly energy efficient and lean low-cost solutions at the cost of multi-hop capability and dynamic flexibility. Depending on the deployment situation hetero deployments (repeater and IAB) might be economically favorable.

In pre-cursor experiments we could successfully demonstrate the 5G-compliant transmission of a 500 MHz wide 256 QAM signal (5 carriers) via a 28/39 GHz [45].

Within TARANTO we investigate SiGe-BiCMOS based transceiver concepts for a mmW repeater providing FWA to a number of households by a controlled grid of mmW-beams operating at 28 GHz and backhauling to a donor via a 39 GHz fronthauling connection. Considering the harsh cost constraints for communication gear in the access network segment going along with the tough technical requirements on phase noise, bandwidth and spectral purity implied by 5G compliant operation, integrated solutions based on SiGe

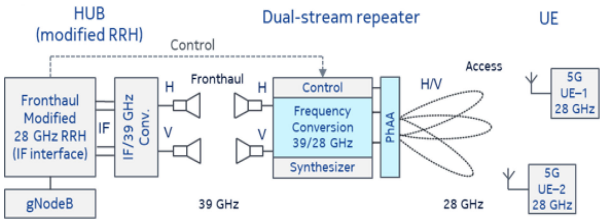

FIGURE 13. Demo Setup for Beamforming mmW Repeater including Donor(left) and UE (right).

BiCMOS technologies which support integrated CMOS based on-chip signal processing offer a promising solution.

The dual stream repeater (in the center of Fig. 13) supports two orthogonal polarizations ('H' and 'V'). The underlying RFICs are realized in IHP's SiGe-BICMOS SG13S and Infineon's B11HFC and B12HFC. They comprise a variety of functions like e.g., 28 GHz- and 39 GHz LNAs and PAs, 28 GHz single channel phase shifter, 39/28 GHz frequency converter, 39 GHz vector modulator phase shifter, VGA and SPDT switches. Each phase shifter RFIC integrates four dual-polarized transceivers and is mounted and connected to a 2x2 antenna array module on the back of the PCB. With all this, the addressed use case offers a wide field and excellent opportunity for assessment of the technology performance and quality of device models.

The frequency converter RFIC additionally supports the extraction of the 3 GHz wide auxiliary control channel which is needed for the remote control of the repeater's Time Domain Duplex (TDD) and beam switching functions by the donor. To this purpose the control signals are extracted in this demonstrator setup from the modified remote radio head (RRH) and modulated onto a 3-GHz wide sub-channel. In an alternative scenario the control channel information may be transmitted via unlicensed mmW-band. In the repeater the control information gets extracted from the control channel and is fed to an FPGA which performs decoding and repeater control. In a later version, such function could be performed by the CMOS section of the SiGe-BiCMOS RFIC.

2) ACCESS TECHNOLOGIES

The access network is the last-stage link towards the users. This part of the network is typically flexible and functionally diverse to support user mobility and multiple applications and services. The evolution of different mobile-communication generations was driven by the increasing demands on data-rate, mobility, reliability, latency and power efficiency. The 5th generation (5G) that offers up to 10 Gb/s connectivity, is currently being rolled-out. An extrapolation of performance trends of previous generations indicates that the next generation (6G) might hit the market by 2030, offering 100 Gb/s connectivity with sub-ms latency between user equipment and access point while consuming at least 5 times less power [46]. This will enable new applications and services such as wireless data passages and intuitive augmented reality enabled by smart glasses.

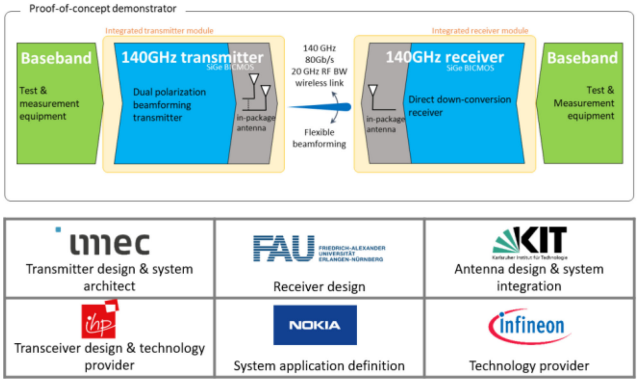

FIGURE 14. Integrated 6G transceiver system demonstrator.

However, many technological hurdles need to be solved to build the 6G access infrastructure and user equipment. The envisioned data rates require the use of new frequency bands in the sub-THz range, and the D-band (110–170 GHz) is a good candidate given the availability of high aggregate bandwidths and reasonable atmospheric absorption. These higher frequency bands, however, come with severe challenges for the design of the integrated radio. In TARANTO, we tackle some of these challenges via innovation in 140 GHz transceiver circuitry and antenna-and-packaging solutions. The goal is to demonstrate a flexible beamforming system streaming data at 80 Gb/s over a wireless link of up to 10 meters. The system, illustrated in Fig. 14, is a compact, densely integrated and power-efficient solution which aims to support future product integration. The circuits were designed in Infineon's and IHP's BiCMOS technology (B11HFC and SG13G2). These technologies support high speed operation and come at low cost. This is essential as the access network is the most cost-sensitive segment of the entire telecommunication network.

The transmitter features transmission paths for two polarizations, comprising frequency multiplication, IQ-modulation and power amplification, all integrated on chip. The realizations described in [47], [48], showcase the power amplifier's P_{sat} of 18 dBm and a sub-THz radiator that achieves 27 dBm of EIRP at 140 GHz. A dual-polarized receiver architecture has been designed, which directly down-converts the sub-THz signal towards baseband. The coupled line circuit and the broadband low noise amplifier design are described in [49], [50]. Additional beamforming circuits are presented in [51], [52]. The chips are then integrated into a chip-scale fanout package which also includes high-efficiency dielectric resonator antennas [48]. The chips are interfaced to the antenna elements through quasi-coaxial vertical via transitions to achieve the most compact stack-up while supporting future antenna-array scalability. The electrical and mechanical connection is achieved via double-stacked gold stud bumps and the thermal evacuation is considered during the entire design. An indicative assembly of the transmitter module is illustrated in Fig. 15 (left), showing that two chips are enclosed in a scalable package to achieve flexible beamforming. Optional hemi-elliptically shaped Teflon lenses, positioned centrically

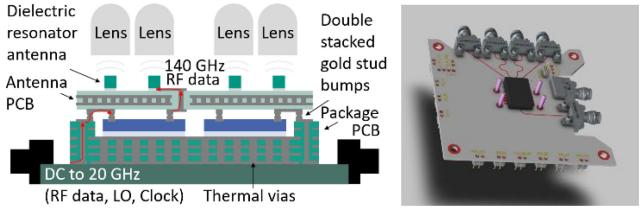

FIGURE 15. Transmitter module stackup (left) and mockup (right).

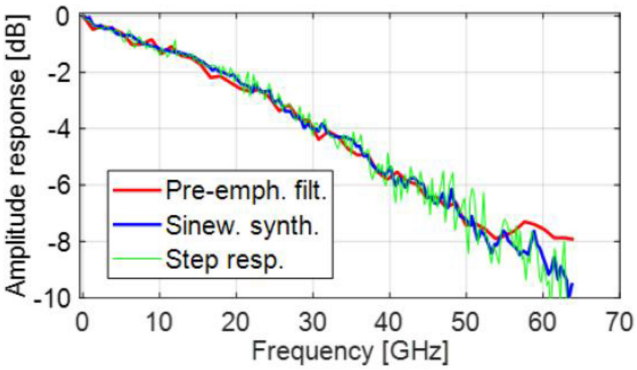

FIGURE 16. Frequency characteristic of the DAC5.

above each antenna by means of the studs illustrated in Fig. 15 (right), can be added to enhance the antenna gain and keep some beam-steering capability at the same time. The modules are currently assembled and will be measured afterwards.

B. HIGH-SPEED OPTICAL TRANSMISSION SYSTEM

High-speed optical transmission systems are nowadays based on coherent transmission of high-order QAM-modulated data streams applying constellation shaping, e.g., probabilistic constellation shaping [53], [54]. Generation of the required analog multilevel waveforms is achieved using digital-to-analog converters (DAC) on the transmitter side and for receiving the data signals digital-to-analog converters (ADC) are used on the receiver side.

Within TARANTO, the project partner Micram designed a high-speed DAC chip, the DAC5, supporting a tuneable sampling rate of up to 128 GSa/s in STMicroelectronics's BiCMOS055 technology featuring high-speed bipolar transistors ($f_T = 325$ GHz, $f_{max} = 375$ GHz). The CMOS part of the chip contains memory that can hold 512 kSamples and the low speed circuit part. The high-speed part is designed in bipolar technology.

The analog frequency characteristic of the packaged DAC5 module was measured to be down 3 dB at 24 GHz, 6 dB at 43 GHz and eventually 10 dB at 64 GHz as shown in Fig. 16.

The physical resolution of the DAC5 is 8 bits and the effective number of bits (ENoB) was found to be ~4 at the Nyquist frequency with SINaD characterization method, see Fig. 17.

At Nokia Bell Labs, the ENoB was determined with broadband data signals and confirmed the measurement results of Micram.

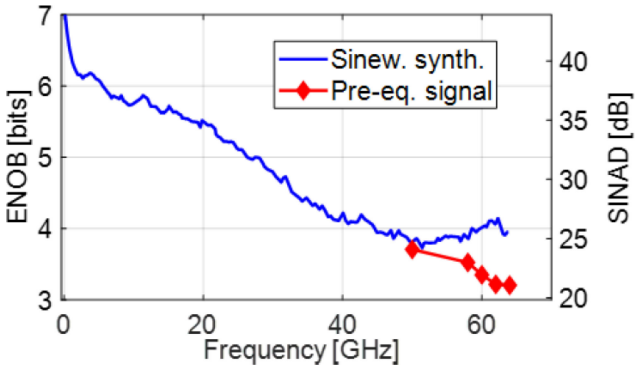

FIGURE 17. ENoB and SINAD versus frequency.

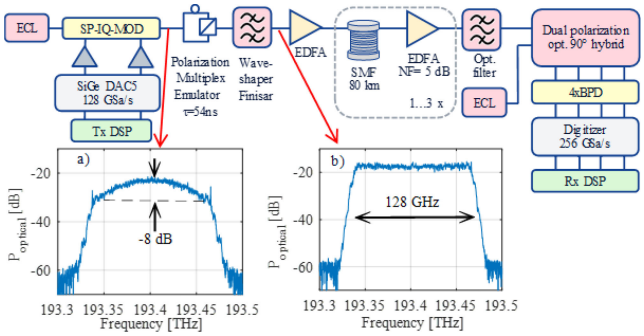

FIGURE 18. Experimental setup of the optical transmission system.

For the high-speed coherent optical transmission experiment, which is depicted in Fig. 18, linear pre-filters for the electrical path containing the DACs and the modulator driver amplifiers are derived that lead to the best Q-factors at the output. The pre-filters are applied to the 128 GBd digital PCS 256 QAM data signals, which have an entropy of 7.5 bits/symbol at 1 sample/symbol, before uploading to the DACs memory. The light of an external cavity laser is modulated by a single polarization IQ-modulator and a polarization multiplexing emulator with more than 6900 symbols delay generates the dual-polarization signal. The frequency response of the IQ-modulator is compensated for by a programmable optical filter, see insets a) and b) of Fig. 18 for the optical spectrum before and after filtering.

The transmission link consists of 1 to 3 spans of standard single mode fiber each having a length of 80 km and followed by an EDFA. At the receiver the optical signal is down converted to baseband by mixing with the light of the local oscillator laser in a 90° hybrid and balanced photodiodes convert it to electrical signals which are digitized by a real time oscilloscope. The data are stored on a PC and data aided digital signal processing is applied to recover the original QAM symbols. For a more detailed description please refer to [55], [56].

In Fig. 19 the results of the optical transmission experiments are summarized showing the information rate and net bit rate after FEC decoding versus the transmission distance.

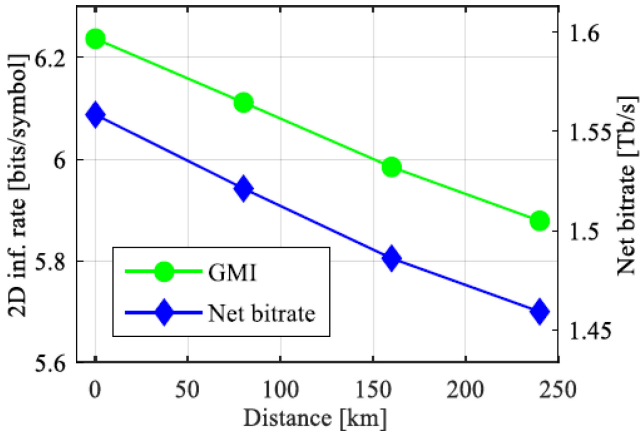

FIGURE 19. Information rate and net bit rate versus transmission distance.

The resulting net data rates of 1.55 Tbit/s in back-to-back, 1.5 Tbit/s after 160 km and 1.47 Tbit/s after 240 km fiber transmission are the highest demonstrated net rates per wavelength to date.

V. CONCLUSION

High performance BiCMOS technology platforms providing HBTs with f_{MAX} up to 500GHz and beyond are presented. It is shown that these technology platforms are key enablers for high speed & high data rate communication systems, which require high integration level. For successful design of those complex systems, accurate mmW characterizations with emphasis on harmonic distortion analysis, power and noise figure measurements up to 190 GHz and 325 GHz respectively and S-parameter measurements up to 500 GHz have been carried out. Excellent results have been achieved comparing the measured results to electrical compact models of active (HBTs) and passive components as well as from benchmark circuit blocks for model verification. Finally, BiCMOS-enabled systems and applications with focus on future wireless communication systems and high-speed optical transmission systems up to resulting net data rates of 1.55 Tbit/s demonstrate the superior potential of BiCMOS technology platforms.

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