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A SiGe BiCMOS Amplifier-Frequency Doubler Chain Operating for 284–328 GHz

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Abstract

This work describes the development of an amplifier frequency doubler chain (AFDC) operating at around 300 GHz based on SiGe BiCMOS technology. The driver amplifier is based on the differential cascode configuration, which employs coupled-line transformers for compact design. The frequency doubler is based on the class-B topology, which is known for exhibiting a large output power with low DC power consumption. The integrated AFDC, which consists of the frequency doubler and the preceding driver amplifier, exhibited a measured peak output power and DC-to-RF efficiency of −0.9 dBm and 0.97%, respectively, along with a conversion gain of −0.1 dB. It operates from 284 to 328 GHz with a 0-dBm input signal, consuming a total DC power of only 84 mW. The chip size is 720 × 310 μm^2, excluding RF and DC pads.

Key Words: Amplifier, Frequency Doubler, Heterojunction Bipolar Transistor (HBT), Silicon Germanium.

I. INTRODUCTION

The terahertz frequency range (100 GHz–10 THz) is highly promising in a wide range of applications, such as ultra-high-data-rate communication and ultra-high-resolution radar systems [1]. In particular, the WR3.4 band (220–330 GHz) attracts great interest since it corresponds to an atmospheric window with low attenuation while providing a sufficiently high frequency band. Silicon (Si)-based technologies, which are widely employed for various microwave and millimeter-wave band applications, remain as a preferred option for circuit designs even in this vastly raised frequency range, as they continue to benefit from advantages such as a high integration level and compatibility with other circuit blocks. While there has been a barrier for these technologies to enter the THz arena due to the device's speed limit, the recent improvements in Si-based technologies have enabled their application to various THz systems with sufficient feasibility. Recently, there have been a growing number of reports on SiGe technology being applied to WR3.4 band systems, including a 240-GHz I/Q transceiver with 100-Gbps data-rate [2], a broadband 210–270 frequency modulated continuous wave (FMCW) radar [3], etc. For these high-frequency systems, which employ transmitters or local oscillators as core components with signal generation, two key performance parameters are power and bandwidth. They restrict the link distance and data rate capability, respectively. Naturally, it is desired that sufficient output power is maintained across the entire operating range with a wide bandwidth, which is a crucial aspect for THz system performance [4, 5]. Most often, however, there is a trade-off between the output power and the bandwidth,

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making it challenging to achieve a wide bandwidth with consistently large output power. That challenge also applies to frequency multipliers, one of the key THz components to obtain high-frequency signal generation. The purpose of this work is to develop a frequency multiplier operating at around 300 GHz with a high output power with a wide operation bandwidth.

In this work, to attain the technical goal, we have developed an amplifier-frequency doubler chain (AFDC) based on SiGe BiCMOS technology. The proposed circuit consists of a one-stage driver amplifier (DA) and a frequency doubler (FD) intended for high power and wideband performances.

II. Circuit Design

In the proposed AFDC designed in this work, a differential 150-GHz DA is integrated with a balanced 300-GHz FD, as shown in Fig. 1. One issue with using a FD is that the input power needs to be high enough to obtain a reasonable power level at the output of the circuit [6]. To cope with this challenge, placing a DA before the FD is often practiced, which is also the case for the proposed circuit. The design details of the components developed in this work are provided below, starting with DA and followed by FD and integrated AFDC. All circuit designs are based on the HICUM transistor model together with ADS Momentum full-electromagnetic simulator.

1. 150-GHz Driver Amplifier

The DA operating around 150 GHz is based on a differential cascode topology, as shown on the left in Fig. 1. Since only a single DA stage will be integrated with the FD, mid-size transistors ($A_E = 6 \times (0.07 \times 0.9\ \mu m^2)$) have been selected for Q_1–Q_4, consequently satisfying the gain and output power requirement. The input matching to the differential 100-Ω is achieved with transmission lines TL_1 and TL_2, DC block capacitors C_1 (100 fF), and high-impedance resistors R_1 (500 Ω). It is noted that the parasitic inductance arising from the RF-block resistors R_2 and the bias line at the base nodes of the stacked stage transistors Q_3 and Q_4 causes a stability problem in the circuit. To mitigate this issue, the base nodes of Q_3 and Q_4 need to be shorted by a bypass capacitor. The metal-insulator-metal (MIM) capacitors, located at the top metal level as offered by the foundry, tend to induce extra inductance and resistance as they need stacked via structures all the way down to the device level. In this work, therefore, RF-short capacitors C_2 (150 fF) were implemented using a metal-oxide-metal (MOM) structure that employs M2 (ground level) and M1 levels as the metal plates, requiring only a single via level down to the device.

Employed for the output matching of the DA is a differential transformer TR_1, which is preferred to the transmission lines with the relatively low output collector impedance of the cascode structure, leading to a compact design. The transformer TR_1 is based on an edge-coupling structure built on the thick metal level. The optimum matching point was selected by adjusting the line width (6 μm), spacing between lines (3 μm), and line length (130 μm). To avoid inter-stage feedback between DA and FD, which may cause circuit instability, a series resistor R_3 (12 Ω) was inserted at the injection point of the collector bias V_{CC_DA} [7]. The simulated *S*-parameters of the DA are plotted at Fig. 2. The peak S_{21} is 11.4 dB at 150 GHz and the 3-dB bandwidth is 27 GHz (135–162 GHz). In the simulation, the

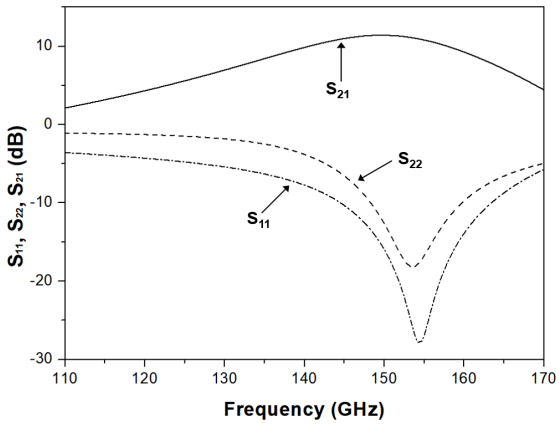


Fig. 2. Simulated *S*-parameters of the driver amplifier.

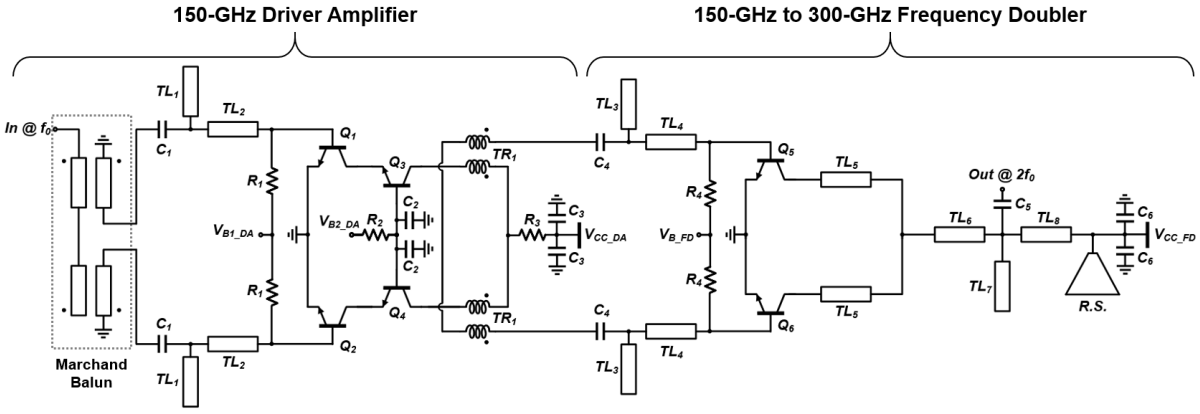


Fig. 1. Schematic of the amplifier frequency doubler chain (AFDC) proposed in this work.

DA yields a saturated output power of 10.5 dBm.

To enable the measurement of the DA with the differential architecture at this frequency, a coupled-line-based Marchand balun was inserted at the input as well as at the output. The optimum line width and spacing were selected to guarantee the operation bandwidth wide enough to fully contain the DA bandwidth. Fig. 3 shows the *S*-parameter simulation results with full-EM simulation. It indicates an insertion loss lower than 1.6 dB and a phase imbalance smaller than 7.5° within the full operation bandwidth of the DA. The layout of the balun is also included in Fig. 3 as an inset.

2. 300-GHz Frequency Doubler

For frequency doublers, the balanced structure is widely employed in favor of the high conversion gain as well as the effective odd-harmonic suppression [8]. In addition, assuming a sufficient input power with a common-emitter structure, a class-B type doubler with a low base bias can boost the output power and DC-to-RF efficiency [9]. As an effort to better visualize the effect of the base bias V_{B_FD} on the output power and bandwidth, a simulation was carried out with V_{B_FD} variation of 0.4 V to 0.7 V. The results are provided in Fig. 4. Note that the cases with $V_{B\_FD} > 0.7$ V are excluded from the simulation as they exceed the turn-on voltage of the transistor. Fig. 4(a) presents the simulated output power with the input power varied up to 10 dBm with various bias points, while the input frequency is fixed at 150 GHz. For each bias point, the input was matched to the differential 100 Ω and the output was matched to the load-pull point, so that the maximum output power was achieved for each case. Fig. 4(a) indicates that the output power tends to increase with increasing bias voltage at the lower input power regime. However, with a sufficient input power above 5 dBm, the trend reverses and a slightly higher output power is achieved with a lower base bias voltage. This is consistent with the expectation for class-B operation as mentioned earlier. The output power is

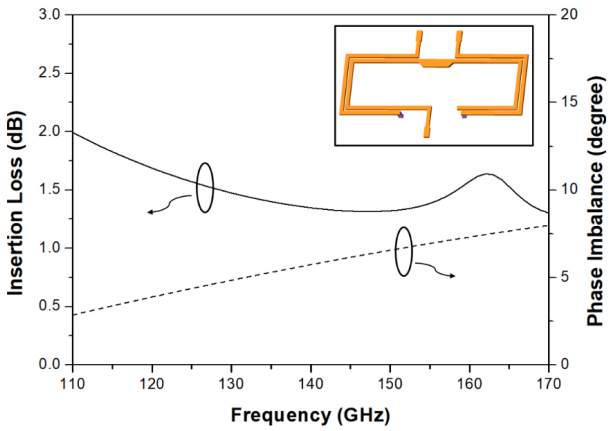
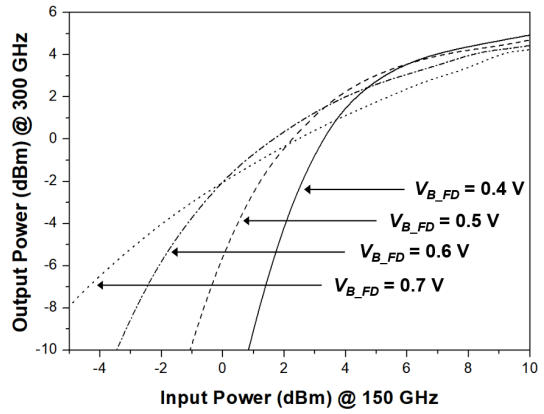
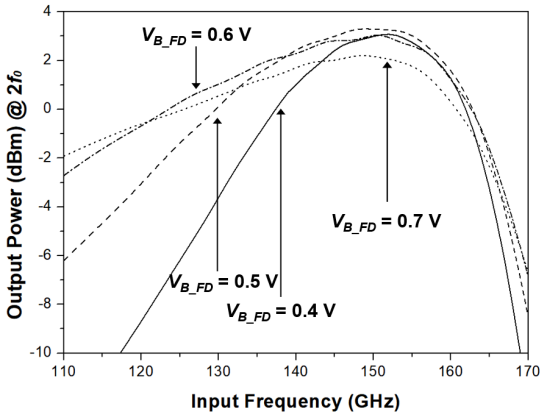


Fig. 3. Simulated insertion loss and phase imbalances for the coupled-line based Marchand balun. Also shown is the layout (inset).



(a)



(b)

Fig. 4. Simulated output power of the frequency doubler (FD) with selected bias points plotted against (a) the input power at a 150-GHz input frequency and (b) the frequency at 5 dBm input power.

plotted against the input frequency in Fig. 4(b). The input and output matchings are fixed at 150 GHz with 5 dBm input power. Since the input matching is achieved at a single frequency point of 150 GHz, the input power applied to the transistors decreases as the frequency deviates from 150 GHz on both sides. Therefore, as V_{B_FD} increases from 0.4 V to 0.7 V, the bandwidth increases since the reduction of the output power with decreasing input power level is slower for higher V_{B_FD}, as indicated by Fig. 4(a). Table 1 summarizes the peak output power and the 3-dB bandwidth with V_{B_FD} variation. In this design, V_{B_FD} of 0.6 V is selected as the optimum point between the maximum output power and bandwidth.

The schematic of the FD employed in this work is shown on the right side of Fig. 1. For the common-emitter pair composed of Q_1 and Q_2, a device size of $A_E = 4 \times (0.07 \times 0.9\ \mu m^2)$ was selected, which is around the dimension that showed the largest 2nd harmonic current. Similar to the DA input scheme, TL_3, TL_4, C_4, and R_4 serve to provide the differential 100 Ω impedance matching. The output load-pull matching was obtained using $TL_{5\text{-}8}$ and C_5. Also note that a triangle-shaped radial stub with a

Table 1. Simulated performance of the frequency doubler

	Peak P_{out} (dBm)	3-dB BW (GHz)
$V_{B\_FD} = 0.4$ V	3.08	138–164 (26)
$V_{B\_FD} = 0.5$ V	3.30	131–162 (31)
$V_{B\_FD} = 0.6$ V	3.04	124–162 (38)
$V_{B\_FD} = 0.7$ V	2.20	116–163 (47)

high Q-factor at 300 GHz is used for the first bypass capacitor [10]. Based on this design, the FD shows a maximum output power of 0.4 dBm at an input signal of 150 GHz with 8 dBm by simulation.

To verify the operation of the integrated AFDC, a simulation on the entire circuit composed of the input balun, DA, and FD was carried out. The simulation results will be described in the next section together with the measurement results for a better comparison.

III. Experimental Results

The designed AFDC was fabricated in IHP 130-nm SiGe BiCMOS technology with $f_T/f_{max} = 300$ GHz/500 GHz [11]. The chip size is 1060 μm × 550 μm and 720 μm × 310 μm with and without probing pads, respectively. The chip photo is shown in Fig. 5(a). In addition, separate circuits of DA and FD were also fabricated to characterize their individual performances. Their chip photos are presented in Fig. 5(b) and 5(c).

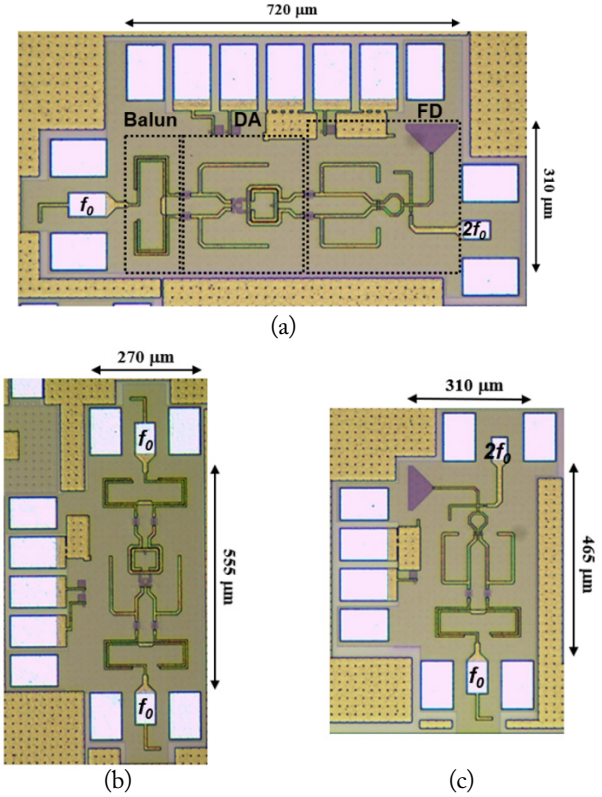


Fig. 5. Chip photo of the fabricated circuits: (a) amplifier frequency doubler chain, (b) driver amplifier (DA), and (c) frequency doubler (FD).

Fig. 6 shows the setup for measuring the output power of the fabricated circuits. The input signal is provided by a VDI WR6.5 (110–170 GHz) signal source module, which multiplies (×12) the signal from an Agilent E8257C signal generator. The output power was measured with a VDI PM5 power meter through GGB WR3.4 and WR6.5 waveguide probes, depending on the signal frequency range. It is noted that an input loss of 2.5 dB from the WR6.5 probe was compensated for in the presented data. The loss from the input balun was not subtracted, considering it as a part of the circuit. As for the output loss, all the losses that arise from the output probe (WR3.4 for FD and AFDC, WR6.5 for DA) and the waveguide transition taper (WR3.4 and WR6.5 to WR10 for FD/AFDC and DA, respectively) were compensated for in the measured results. The loss was around 4 dB for the WR3.4 probe and below 0.5 dB for the tapers.

The measured output power of the individual DA is shown in Fig. 7, which also includes simulation results for comparison. Baluns were included at both the input and output of the DA to allow single-ended measurements. Since the output balun is not integrated in the AFDC, the data without the balun loss (estimated from the simulation) are included together with the as-measured data in the plots. The input balun loss was not subtracted, as it is a part of the integrated AFDC, as mentioned earlier. As shown in Fig. 7(a), the output power was measured across the input frequency range of 130–170 GHz with a fixed input power of 0 dBm. The peak output power was 7.7 dBm (9 dBm without output balun loss) at 142 GHz and 7.3 dBm (8.6 dBm without output balun loss) at the center frequency 146 GHz. The results for the large signal characteristic at 146 GHz are as shown in Fig. 7(b), indicating a saturated output power of 9 dBm (10.3 dBm without output balun loss). These results were all obtained at $V_{B1\_DA} = 0.9$ V, $V_{B2\_DA} = 2.2$ V, $V_{CC} = 4$ V, $I_{CC} = 14$ mA.

Next, the measurement results of the individual FD are presented. The measured output power over the output frequency range of 260–340 GHz (input frequency range of 130–170

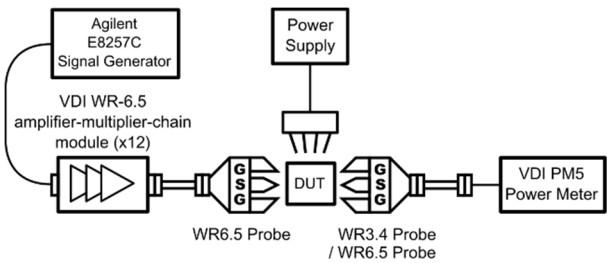


Fig. 6. Setup for the output power measurement. Output probing is based on: a WR3.4 probe for FD, WR6.5 probe for DA, and fundamental-mode leakage measurement of FD.

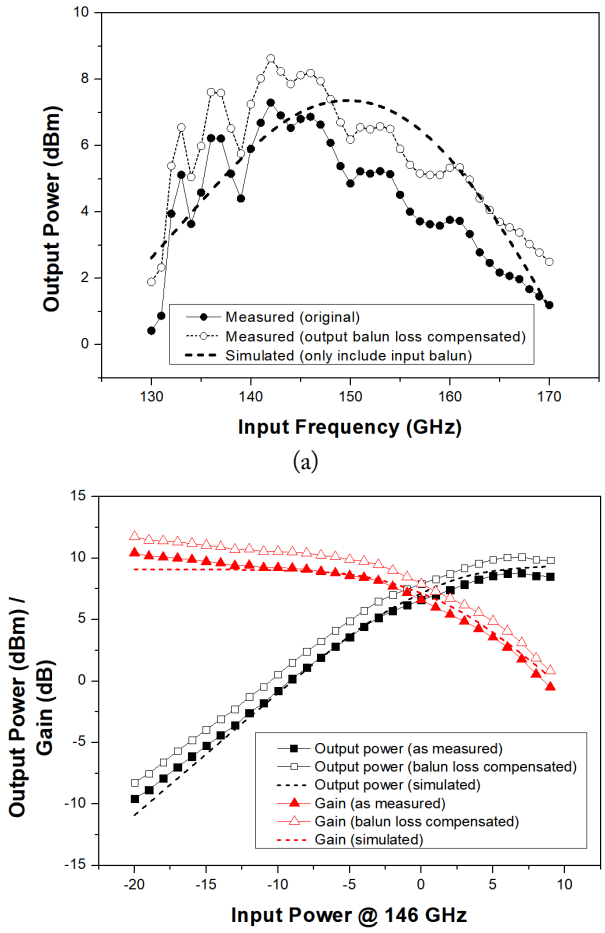


Fig. 7. Measured and simulated output power of driver amplifier against (a) the input frequency at 0 dBm input power and (b) the input power at 146 GHz input frequency. The results without the balun loss (estimated from the simulation) are also presented.

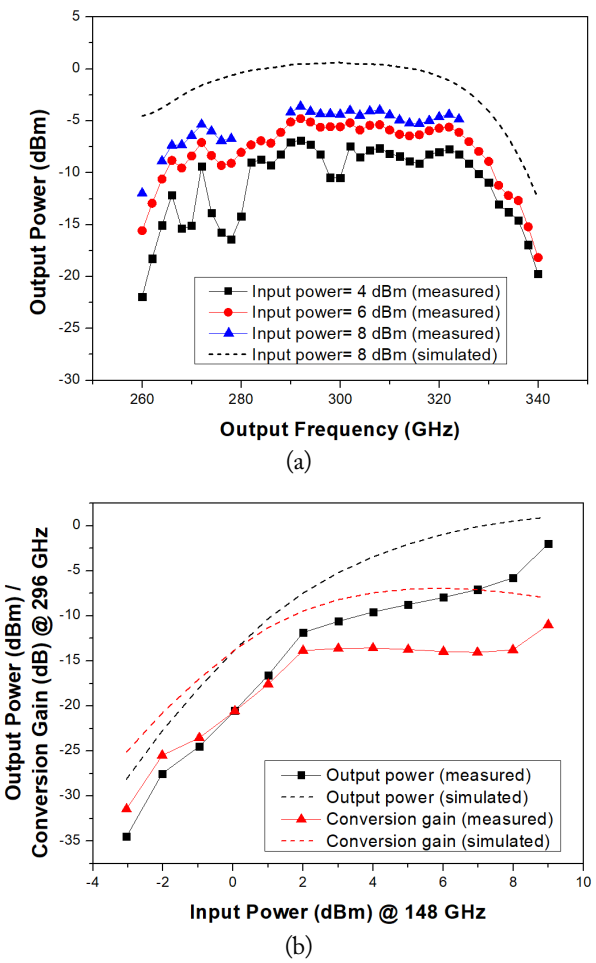
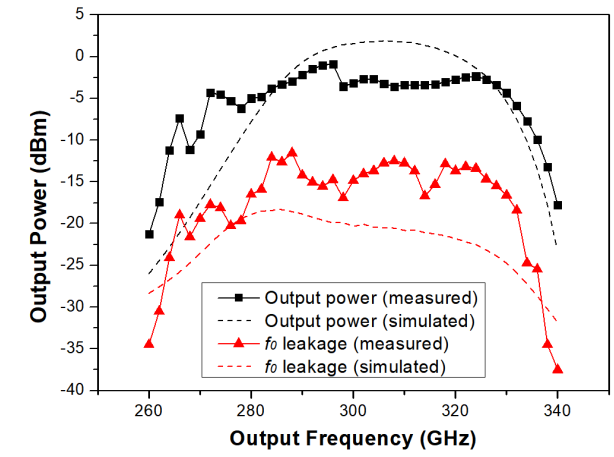


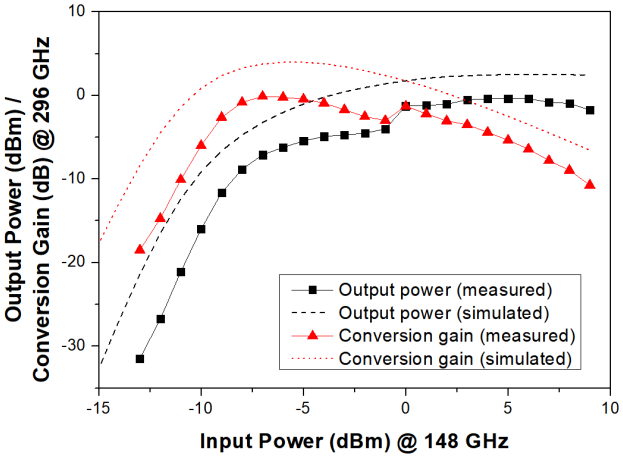
Fig. 8. Measured and simulated output power of frequency doubler against (a) output frequency at selected input power level of 4/6/8 dBm (for the curve with 8-dBm input power, data points are missing for some frequency ranges due to the limited input power of the signal source) and (b) input power at 148 GHz input frequency.

GHz) is shown in Fig. 8(a) with three input power levels of 4, 6, and 8 dBm. It is noted that for certain frequency ranges, an input power level of 8 dBm was not available with the WR6.5 source module used as the input signal source due to the frequency-dependent maximum output power limit. Hence, on the curve corresponding to the 8-dBm input power in Fig. 8(a), some data points are absent. The measurement shows a peak output power of −3.6 dBm at 292 GHz. The 3-dB bandwidth is measured to be 34 GHz (290–324 GHz) with 8 dBm input power (it could be larger if 8-dBm input power were available for frequency points near the upper boundary of the bandwidth). The results for the large signal characteristic at 296 GHz are as shown in Fig. 8(b), indicating a maximum output power measured as −2 dBm. It is observed in the plot that when the input power rises from 8 to 9 dBm, the output power showed a rather rapid increase from −5.8 to −2 dBm. Such a boost was observed consistently, even for the AFDC measurement to be discussed later. Hence, it is believed to be a true response of the FD and part of its large signal characteristic. It is noted that an input balun was inserted at the input of the FD, as was the case for the DA, and the loss from the balun is not compensated for in the data presented in Fig. 8. Hence, the actual input power arriving at the physical front-end of the FD (after the input balun) will be slightly smaller (estimated to be 1.6 dB from the simulation) than what is shown in the figure. The bias conditions for the measurement were $V_{B\_FD} = 0.66$ V, $V_{CC} = 2$ V, $I_{CC} = 14$ mA.

Finally, the measurement results of AFDC are discussed based on the data presented in Fig. 9. For these data, the same optimized bias conditions used for the individual circuit measurement were applied. Fig. 9(a) shows the output power measured over the frequency range of 260–340 GHz with 0 dBm input power. The maximum measured output power was −0.9 dBm at 296 GHz, and the 3-dB bandwidth was 44 GHz (284–328 GHz). Also shown in Fig. 9(a) is the leakage power to the fundamental mode (f_0), which was measured through a WR6.5



(a)



(b)

Fig. 9. Measurement results of the AFDC: (a) output power and fundamental-mode (f_0) leakage versus frequency and (b) output power and conversion gain versus input power at 148 GHz.

probe at the same output node. The result shows a suppression ratio of more than 8.3 dBc across the entire frequency range measured. When compared to the simulation, the measurement exhibits a slightly lower output power and higher fundamental-mode leakage, which may be ascribed to the phase and gain imbalance of the actual circuit, including the input balun. In Fig. 9(b), the output power measured with the input power swept up to 9 dBm with a fixed output frequency of 296 GHz is presented. It shows a maximum output power and conversion gain of −0.4 dBm and −0.1 dB, respectively. One may observe a substantial increase in the output power when the input power increases from −1 to 0 dBm. This point roughly coincides with the input power at the FD front-end of around 8–9 dBm, indicating that it arises from the same cause observed with the individual FD circuit. The total DC power consumption was 84 mW at 300 GHz with P_{in} = 0 dBm, leading to a maximum DC-to-RF efficiency of 0.97%. Table 2 compares the performance of the AFDC developed in this work with the recently reported frequency multiplier-based signal sources in SiGe BiCMOS technology operating above 200 GHz [7–9, 12, 13]. The AFDC in this work shows the widest 3-dB bandwidth and one of the highest DC-to-RF efficiency values.

IV. Conclusion

A WR3.4 AFDC, which comprises a 284–328 GHz FD integrated with a DA, has been successfully developed based on 130-nm SiGe BiCMOS technology. The integrated circuit exhibited an output power of −0.9 dBm at 296 GHz and a 3-dB bandwidth of 44 GHz. Separate circuits for the individual FD and DA were also fabricated and characterized. The developed

Table 2. Comparison of frequency multiplier based sources in SiGe BiCMOS operating over 200 GHz

	Shopov et al. [8]	Oejefors et al. [9]	Sarmah et al. [12]	Schmalz et al. [13]	Eissa et al. [7]	This work
Technology	55-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS
f_T/f_{max} (GHz)	330/350	250/380	300/450	300/450	300/500	300/500
Circuit	VCO + amplifier + doubler (×2)	Amplifier + doubler (×2)	Multiplier (×16) + amplifier	VCO + amplifier + doubler (×2)	Multiplier (×8) + amplifier	Amplifier + doubler (×2)
Center frequency (GHz)	247.5	318	250	245	255	296
3-dB BW (GHz)	27	20	30	22	40	44
Peak P_{out} (dBm)	7.2	−1	2.5	2	0	−0.9
P_{DC} (mW)	386	424	700	290	430	84
DC-to-RF efficiency (%)	1.30	0.19	0.14	0.54	0.40	0.97
Area (mm^2)	NA	0.516	0.98	0.32	0.98	0.223

NA = not applicable.

AFDC is expected to be well suited for various applications that require high power and wideband near 300 GHz.

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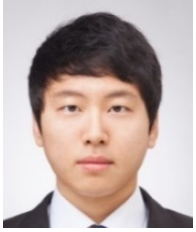
Junghwan Yoo



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