Differential-Mode Power Detection for Built-In Self-Test of SiGe Automotive Radar Transceiver Front Ends

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***Abstract*— Recently, the feasibility of differential-mode power detection for built-in self-test (BIST) in millimeter-wave SiGe transceiver front ends has been demonstrated. In this work, a system analysis of typical BIST scenarios is performed. Specifications for the input power levels as well as the accuracy of power detectors are derived from this analysis. A need for at least two different differential detector architectures is identified. Two detectors are derived from the differential power measurement concept, analyzed, and implemented in the 76–81-GHz automotive radar frequency band. They feature a low power consumption of 500 μW and, to the authors' best knowledge, the lowest published circuit areas of approximately 0.005 mm^2 while still being input matched to the differential 100 Ω system impedance. Both these characteristics are essential to keep the overhead of the BIST minimal. With dynamic ranges of 30 dB and up to 46 dB for the two different architectures, the differential power detector concept can achieve sufficient performance for BIST applications. The robustness against process and temperature effects as well as noise is analyzed and reported for both detectors.**

***Index Terms*— Automotive radar, built-in self-test (BIST), differential power measurement, millimeter wave, power detector, SiGe.**

I. Introduction

THE proliferation of automotive radar in the 76–81 GHz bands has paved the way for mass-market millimeter-wave circuits in silicon technologies [1], [2], [3]. While the predicted adoption of millimeter-wave frequencies for 5G communications has not manifested yet, they remain a hot candidate for 6G applications [4], [5], [6]. Promising research results on radar and communications circuits at 60 [7], [8], [9], [10], [11], 120 [7], [12], [13], [14], and 140 GHz [15], [16], [17], [18], [19] have recently been published, demonstrating the technical feasibility of future high-volume millimeter-wave applications. When deploying large numbers of integrated circuits, testability becomes an important concern. As shipping defective products to customers is not acceptable from a quality perspective, every single IC has to be tested for correct functionality. At millimeter waves, this test is complicated and time-consuming. Due to the limited availability of automated test equipment at these high frequencies, often, complete characterization is only performed on one test batch. The manufactured circuits are then assumed to deliver their millimeter-wave performance as long as the process parameters are within specification. In this environment, off-loading certain parts of the test onto the IC itself, i.e., by implementing built-in self-test (BIST) functions, becomes an attractive proposition.

The authors have recently [20] demonstrated the feasibility of differential-mode square-law power detection between 76 and 81 GHz. However, a clear perspective what role this type of detector might play in BIST applications compared to traditional single-ended architectures, e.g., [21], [22], is missing as of today. To remedy this, we analyze typical BIST scenarios found in the literature. From this analysis, specifications for the detectors, power levels at the detector input, as well as requirements on the sensitivity and accuracy are derived. Comparing different approaches to in situ power measurement of differential circuits under test (CUTs), it is found that detectors that are sensitive to the differential mode of a signal under test can be a vital tool when implementing BIST for these circuits.

To cover all projected test scenarios, at least one square law and one peak detector with as large a dynamic range as possible are required. Accuracy of the power measurement is essential in BIST applications. The detector has to be either robust against temperature and process effects as well as noise or calibration without significant overhead has to be possible. In addition, the power and area overhead of the test have to be kept to a minimum. The, to the authors' knowledge, only other previously published differential power detector in the millimeter-wave range [23], while providing tuning functionality to cope with variation, unfortunately has a low dynamic range and shows significant frequency dependence. Both need to be improved upon.

Consequently, we present two differential detector architectures. The first, providing square law and peak detection,

Manuscript received 21 August 2023; revised 20 November 2023; accepted 27 December 2023. Date of publication 25 January 2024; date of current version 7 August 2024. *(Corresponding author: Yannick Wenger.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TMTT.2024.3354124.

Digital Object Identifier 10.1109/TMTT.2024.3354124

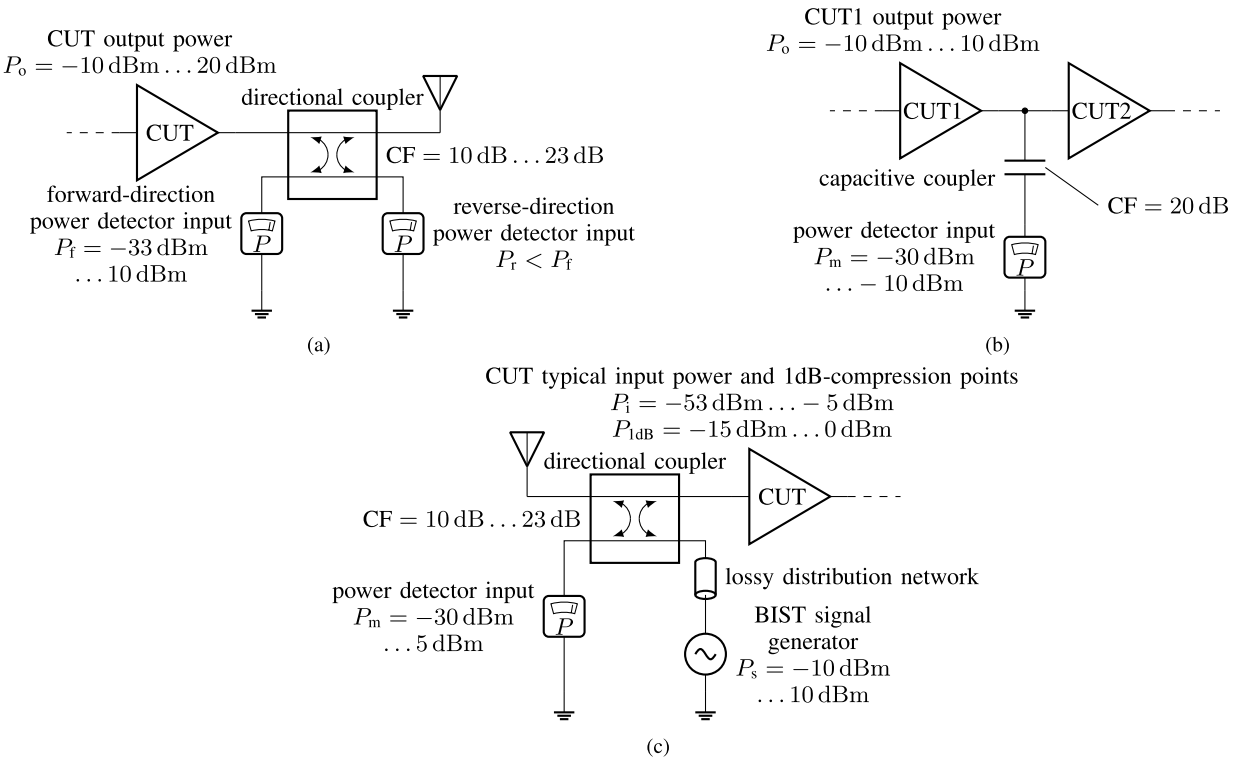

Fig. 1. Typical application scenarios for power measurement in a millimeter-wave transceiver. (a) Measurement of forward and reflected power with a directional coupler, often found in transmitter test, (b) interstage power measurement using a capacitive coupler, and (c) test signal injection into a receiver. CF: coupling factor. CUT: circuit under test.

can cope with input powers as high as 14 dBm while the other, a square-law detector, is well suited for low-power signals. Both detectors are resistively matched at their input. Hence, they can be very compact because large-area matching networks are not required. Temperature and process-dependent effects for both architectures are investigated. This article presents noise analysis of differential power detectors for the first time in the literature. We show that the lower limit of the dynamic range of square-law detectors is dominated by offset effects over noise.

Section II contains the BIST system analysis. The two differential power detector architectures, in the following referred to as common-collector-based (CC-based) and common-emitter-based (CE-based) detectors, are derived in Section III. In Sections IV–VI, the nonideal behavior of both circuits regarding process/temperature variation, noise, and the frequency dependence of their input impedance is analyzed. Based on these results, a test structure for either circuit is developed in Section VII. Experimental results are reported in Section VIII, showing that both detectors are suited for BIST applications. Finally, Section IX concludes this work with finishing remarks and an outlook on power detection in millimeter-wave BIST.

II. BIST System Considerations

A. Waveforms—Peak or Square-Law Detector?

Power detectors broadly fall into two categories. A peak detector's output is proportional to the amplitude of the measured signal; the output of a square-law detector, on the other hand, is proportional to the signal power. This means that the power of modulated waveforms can be measured with this type of detector [24]. Consequently, the design of a test system has to start with an analysis of the signals that have to be captured by the power sensors. If the CUT has a test mode, where dedicated, purely sinusoidal signals are injected into the CUT, both types of detector are adequate. In more complex test scenarios, e.g., when live-monitoring a transceiver, the matter becomes less clear cut. Frequency-modulated continuous-wave (FMCW) radar and its variants are the standard modulation scheme for automotive radars today [3]. In these modulation schemes, the envelope of the high-frequency signal is constant, and peak detection is sufficient. More complex modulations, such as pseudorandom noise (PRN) sequences or orthogonal frequency-division multiplexing (OFDM), have been proposed for automotive radar [2]. A test system handling these waveforms has to rely on square-law detectors.

B. Power Levels in Typical Test Scenarios

In a second step, the expected power levels at the detector input have to be identified. Transistor-based power detectors in SiGe feature dynamic ranges between 30 and 40 dB [21], [22]. To find out whether this is sufficient for BIST purposes, a study of different test approaches is performed. Fig. 1 shows several typical application scenarios of BIST in millimeter-wave transceivers. Variations or combinations of these examples are common in practice.

The first example, Fig. 1(a), is a configuration often found at transmitter outputs to measure the output power of the

power amplifier (PA), e.g., [25], [26], [27], [28]. A directional coupler is placed between the output of the PA and the antenna. Power detectors on the coupled ports measure the forward power P_f as well as the reflected power P_r. In FMCW radars, the PA is usually driven close to saturation [29]. Reported saturated output powers of SiGe automotive radar transmitters are slightly below 20 dBm [26], [30], [31], [32]. Sometimes, the output power is adjustable as in [26] where it can be as low as −10 dBm. In addition, when considering PRN or OFDM radar, the average output power will approximately be 2 dB [33] or 6 dB [32] below the peak. Consequently, a range from −10 to 20 dBm should be considered. Coupling factors of directional couplers proposed for BIST range between 10 and 23 dB [26], [28], [34], [35].

Taking these values into account, the lowest signal powers the detector measuring in the forward direction has to handle are slightly below −30 dBm. The required dynamic range can be as high as 40 dB. Reflected power levels will generally be weaker compared to the ones in the forward direction. When the matching is good, there is barely any reflection; in case of full reflection, for example, when the connection between coupler and antenna fails, the signal will experience two times the loss between coupler and antenna on top of the coupling factor before arriving at the detector. Due to the limited dynamic range of power detectors quoted above, using different detectors each optimized to the expected power level should be considered.

Fig. 1(b) shows a second application scenario. A capacitive coupler is placed in between CUT1 and CUT2. If the signal chain is unidirectional, the signal fed to the power detector via the coupler will largely depend on the output power of CUT1. A low coupling factor ensures that the signal path under test does not experience significant loading. This approach can be a good choice to measure signals at important nodes within the transceiver, for example, in the LO distribution chain [26]. The area overhead is reduced compared to a directional coupler. Typical power levels inside LO distribution chains vary between −10 and 10 dBm [25], [26], [30], [36]; capacitive couplers are usually designed to a coupling factor of approximately 20 dB [34], [37]. The resulting requirements on the power detector are somewhat relaxed compared to the previous case with levels between −30 and −10 dBm.

In Fig. 1(c), a test signal is injected into the CUT, typically the input of a receiver, via a directional coupler. The injected power can be inferred from the power reading of the detector on the through port and the coupling factor. In contrast to the other two approaches, the power at the detector input is higher than at the CUT. Both dedicated test signal generators [26] as well as loopback from the transmitter output [27] have been used in practice to generate the test signal.

If the compression behavior of the CUT is to be tested, the test signal generator has to be able to produce a large amount of power. Reported input compression points for receivers with low-noise amplifiers (LNAs) at their input lie between −15 and −10 dBm [30], [38]. It seems feasible to generate these power levels even including routing losses and the coupling loss. Mixer-first architectures have compression points around 0 dBm [25], [26], [36]. Driving these receivers into saturation will likely stretch the power consumption budget of the test signal generation.

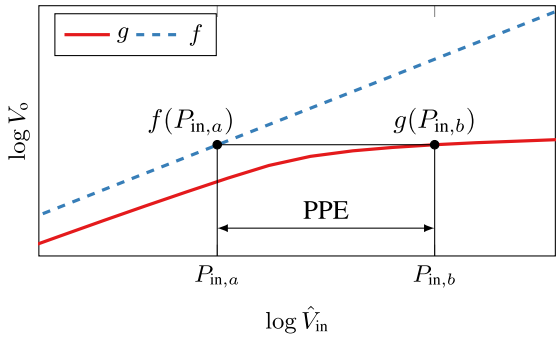

Fig. 2. Definition of the PPE.

The lower power limit of this test configuration will in practice be set by the sensitivity of the power detector. Typical radar receivers can process input signals as low as −90 dBm [30], [39]. Considering a 20-dB coupler, this would mean −70 dBm at the detector input. This is close the sensitivity limit of commercial high-performance detectors for test and measurement applications [40] and, therefore, an unrealistic target for the simple detectors used in on-chip BIST.

Assuming that the test signal is either generated by re-using the CUT output signal from Fig. 1(a) or the signal chain in Fig. 1(b) and adding generous routing losses, power levels between −30 and 5 dB at the power detector are a good estimate. For example, in [26], the detector measures approximately −28 dBm in the test mode, which results in −50 dBm being injected into the receiver.

C. Power Measurement Accuracy

After identifying the power levels at the detector input, we have to consider the accuracy with which these powers have to be determined. Besides the power of the input signal, several factors influence the output voltage of a power detector, e.g., input frequency, noise, matching, process, and temperature shifts. A single measure to judge the accuracy of the detector under all of these influences is desirable. Furthermore, the measure should be valid for both square-law and peak detectors. In this article, we will use the power prediction error (PPE), the ratio of the power predicted from the detector output, and the actual power at the detector input. For a formal definition, consider Fig. 2. The input power $P_{\mathrm{in},a}$ is determined from the output of a detector by inverting the ideal characteristic f shown in blue. However, due to different nonidealities, the detector in reality exhibits the behavior of curve g shown in red. The actual power at the input of the detector is $P_{\mathrm{in},b}$. We define

$$\mathrm{PPE} = 10 \cdot \lg\left[\frac{f^{-1}(g(P_{\mathrm{in}}))}{P_{\mathrm{in}}}\right] \mathrm{dB} \tag{1}$$

where f^{-1} denotes the inverse function of f and $\lg(\bullet)$ is the logarithm with base ten.

Typical specifications for power measurement uncertainty found in the literature are ±0.5 or ±1 dB [41], [42]. The output power of published automotive radar transmitters varies

by approximately 3 dB over process, temperature, and frequency [25], [26], [36]. Gain tuning ranges of amplifiers inside the signal chain are usually significantly larger than this. The same is true for the impact of catastrophic faults such as accidental open or short circuits. Keeping to a ±1-dB specification for the power measurement accuracy should enable the detector to at least capture the most relevant of these effects. Tighter standards pose higher demand on the design and calibration of the detector resulting in unnecessary overhead.

As will be shown in the analysis of the power detector circuits proposed next, the effects of noise as well as process and temperature variation on the PPE depend significantly on the detector architecture. They will be covered in detail next. Matching, on the other hand, can be considered in a generalized manner. This is because it influences the power of the signal at the input of the detector before the detector function itself is applied. For a matched detector connected to a directional coupler as in Fig. 1(a) or (c), the PPE can be calculated from the reflection coefficient Γ of the detector

$$\mathrm{PPE} = 20 \cdot \lg |1 + \Gamma| \ \mathrm{dB}. \tag{2}$$

With an input return loss better than 20 dB, the PPE is naturally better than ±1 dB. For worse matching, (2) can be used to correct the error when the frequency is known, which is the case in many BIST applications. As long as the detector is sufficiently well matched to suppress excessive reflections, it is fine in practice. When pairing a detector with a capacitive coupler [Fig. 1(b)], the value of the detector's input impedance impacts the insertion loss of the coupler due to the voltage division between the coupler and the detector.

D. Differential CUTs

Inside the integrated radar transceiver, most circuit blocks employ differential signaling [26], [36], [38], [43]. Sometimes, even the antennas are differential [30]. Typical millimeter-wave power detectors, on the other hand, are circuits with single-ended high-frequency inputs, e.g., [21], [22]. This poses the question of whether it is possible to correctly determine the power of a differential CUT with conventional single-ended detectors. For simplicity, assume sinusoidal positive and negative signals under test (an extension to periodic signals can be found in [24]), given by

$$v_p(t) = \hat{V}_p \cos(\omega t + \varphi) \tag{3}$$

$$v_n(t) = \hat{V}_n \cos(\omega t + \vartheta) \tag{4}$$

where $\hat{V}_p$ and $\hat{V}_n$ are the amplitudes of the respective signals and φ and ϑ are their phases. The differential-mode signal comprised of v_p and v_n is found as

$$v_{\mathrm{dm}}(t) = v_p(t) - v_n(t) = \hat{V}_{\mathrm{dm}} \cos(\omega t + \delta). \tag{5}$$

Substituting (3) and (4) into (5) and using basic trigonometric identities, one finds

$$\hat{V}_{\mathrm{dm}} = \sqrt{\hat{V}_p^2 + \hat{V}_n^2 + 2\hat{V}_p \hat{V}_n \cos(\varphi - \vartheta)} \tag{6}$$

$$\delta = \arctan\left(\frac{\hat{V}_p \sin(\varphi) - \hat{V}_n \sin(\vartheta)}{\hat{V}_p \cos(\varphi) - \hat{V}_n \cos(\vartheta)}\right). \tag{7}$$

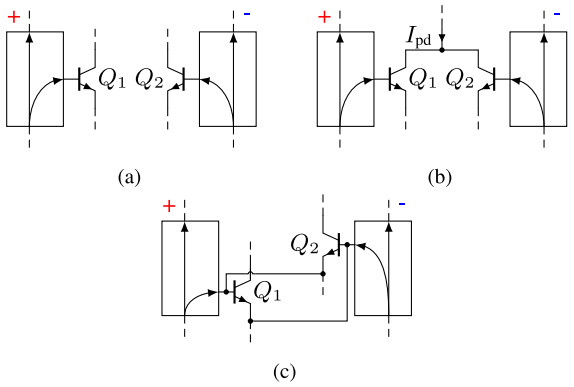

Fig. 3. Measuring the power on a differential signal line with (a) two single-ended detectors, (b) pseudo-differential detector, or (c) differential detector.

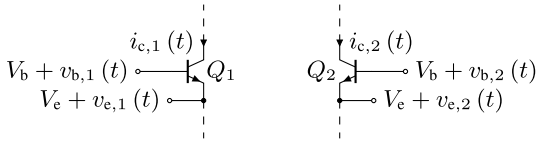

Fig. 4. Current and voltage definitions in differential power detectors.

In the case of perfectly balanced signals, $\hat{V}_p = \hat{V}_n$, $\varphi - \vartheta = \pi$, and (6) simplifies to the well known $\hat{V}_{\mathrm{dm}} = 2\hat{V}_p$. Imbalances in the single-ended amplitudes and phases both influence the differential amplitude. To measure the differential-mode power accurately, the power detector circuit has to be sensitive to the phase relation φ–ϑ in addition to the amplitudes $\hat{V}_p$ and $\hat{V}_n$.

We can now analyze the obvious approach of attaching two single-ended power detectors to the positive and negative signal lines of the differential CUT, as shown in Fig. 3(a). The signals at the power detector transistors are defined in Fig. 4. In this case

$$\begin{aligned} v_{b,1}(t) &= v_p(t) \\ v_{b,2}(t) &= v_n(t) \\ v_{e,1}(t) &= v_{e,2}(t) = 0. \end{aligned}$$

The latter condition is either assured by connecting the emitters of Q_1 and Q_2 to ground or by using a low-pass filter depending on the detector architecture. Adopting the bipolar transistor's voltage–current (I–V) relation, we find for the collector current of Q_1

$$i_{c,1}(t) = I_s \exp\left(\frac{V_b - V_e}{V_T}\right) \exp\left(\frac{\hat{V}_p}{V_T} \cos(\omega t + \varphi)\right) \tag{8}$$

where I_s is the reverse saturation current and $V_T = kT/q$ is the thermal voltage. The following series expansion holds for complex $\underline{z}$ and real ϕ [44]:

$$\exp\left(\underline{z} \cos(\phi)\right) = \mathbb{I}_0(\underline{z}) + 2\sum_{n=1}^{\infty} \mathbb{I}_n(\underline{z}) \cos(n\phi). \tag{9}$$

$\mathbb{I}_n(\bullet)$ is the modified Bessel function of the first kind with order n. Application of (9) to (8) and integration over one

period yields the time average $I_{c,1}$ of the collector current

$$I_{c,1} = \frac{\omega}{2\pi}\int_0^{2\pi/\omega} i_{c,1}(t)\,\mathrm{d}t = I_s\,\exp\left(\frac{V_b - V_e}{V_T}\right)\mathbb{I}_0\left(\frac{\hat{V}_p}{V_T}\right). \tag{10}$$

The current through Q_2 is found in the same way as

$$I_{c,2} = I_s\,\exp\left(\frac{V_b - V_e}{V_T}\right)\mathbb{I}_0\left(\frac{\hat{V}_n}{V_T}\right). \tag{11}$$

If an imbalance in the differential signal occurs that is solely caused by unequal amplitudes, $\hat{V}_p \neq \hat{V}_n$, the currents $I_{c,1}$ and $I_{c,2}$ carry sufficient information to detect the issue. However, if a fault shifts the two single-ended signals out of phase, $\phi - \theta \neq \pi$, the impact on the differential voltage and power according to (6) is not detected by the arrangement in Fig. 3(a).

Sometimes, the pseudo-differential configuration of Fig. 3(b) is encountered. Unfortunately, it does not help to remedy the issue. The collector currents of Q_1 and Q_2 still adhere to (10) and (11), which do not contain information on φ and ϑ. Even worse, in the current of the pseudo-differential detector, both collector currents are summed

$$I_{\mathrm{pd}} = I_{c,1} + I_{c,2}. \tag{12}$$

Consequently, this architecture cannot even identify the amplitudes on each of the two signal lines. For example, if we assume that $\hat{V}_p = \hat{V}_n = \hat{V}$ during normal, fault-free operation, a major fault causing $\hat{V}_p = 0$ and $\hat{V}_n = 2\cdot\hat{V}$, would go completely undetected by the pseudo-differential configuration. The pseudo-differential detector is clearly inferior to using two single-ended detectors.

A detector that is sensitive to the true differential-mode amplitude is shown in Fig. 3(c). The concept was originally proposed in [45] where it was demonstrated up to approximately 10 GHz. The main innovation compared to the other two approaches is that the two single-ended components of the differential signal are both applied to the same transistor. In the case of Q_1, the positive signal is coupled to the base, while the negative one is fed to the emitter. Unfortunately, this results in unequal loading of the two signal paths. Adding a second transistor, Q_2, where the connection of the positive and negative signals to base and emitter is reversed compared to Q_1, solves this problem.

We can, again, refer to Fig. 4 to calculate the collector currents. In contrast to the single-ended detectors, the voltages at the base and emitter are now given by

$$v_{b,1}(t) = v_{e,2}(t) = v_p(t)$$
$$v_{b,2}(t) = v_{e,1}(t) = v_n(t).$$

This changes (8) to

$$i_{c,1}(t) = I_s\,\exp\left(\frac{V_b - V_e}{V_T}\right)\exp\left(\frac{v_p(t) - v_n(t)}{V_T}\right). \tag{13}$$

Applying the definition of the differential voltage (5)–(7) as well as (9) and (10) yields

$$I_{c,1} = I_s\,\exp\left(\frac{V_b - V_e}{V_T}\right)\mathbb{I}_0\left(\frac{\hat{V}_{\mathrm{dm}}}{V_T}\right) \tag{14}$$

$$= I_s\,\exp\left(\frac{V_b - V_e}{V_T}\right)\mathbb{I}_0\left(\frac{-\hat{V}_{\mathrm{dm}}}{V_T}\right) = I_{c,2}. \tag{15}$$

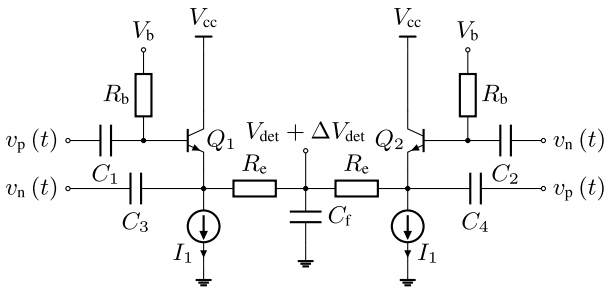

Fig. 5. CC-based detector concept.

Both collector currents are equal because $\mathbb{I}_0(\bullet)$ is an even function.

The currents in this detector contain information on the actual differential signal amplitude and can therefore detect not only imbalances introduced by the amplitudes $\hat{V}_p$ and $\hat{V}_n$ but also when the phases φ and ϑ are not at a perfect 180°. With this detector architecture, it becomes therefore possible to detect faults in differential CUTs that are invisible to more commonly used approaches. The main challenges when realizing millimeter-wave circuits using this architecture lie in the cross-coupled routing of the high-frequency signals. If layout parasitics introduce significant phase imbalances, this might overlay the phase offsets in the signal under test. Consequently, the detector implemented in the original publication [45] could only be experimentally demonstrated up to 20 GHz. In this work, we demonstrate differential power detectors up to 81 GHz.

III. Differential Power Detectors

As we have seen, the current flowing in the transistors from Fig. 3(c) contains information on the differential-mode power of the input signal. In the following, we will develop two detectors from this concept, which will be called CC-based, with the output node at the transistors' emitters, and CE-based where the output is taken from the collectors. The goal is to cover all, or at least most, test scenarios from Section II with these two detectors.

A. CC-Based Detector

The first option to turn the concept from Fig. 4 into a complete power detector circuit with voltage output is by combining it with the so-called "Meyer detector" from [46]. We will call this the CC-based, variant in the following as the output of the circuit shown in Fig. 5 is at the emitter of Q_1 and Q_2. The main characteristic of this architecture is that the time-average current in the two transistors is fixed by a constant current source I_1. Together with the bias voltage V_b, this current source establishes the operating point of the circuit. Because the current is fixed, the application of the high-frequency input signals causes the voltage at the emitters of Q_1 and Q_2 to rise. Emitter resistors R_e are used to form the output voltage V_{det} from these emitter voltages. No zero-frequency current component flows through these resistors as long as the circuit is symmetric. The large filter capacitor C_f presents a short circuit for time-dependent common-mode

voltage components, removing them from the output node. Furthermore, as resistor R_e is usually small (see Section VI), the nonideal finite impedance of the current source I_1 does not impact the common-mode behavior as long as it is sufficiently high at the operating frequency. For differential signals, V_{det} is at virtual ground.

Because of the current sources, $I_{c,1} = I_{c,2}$ from (14) and (15) equals I_1

$$I_1 = I_s \exp\left(\frac{V_b - V_{\text{det}} - \Delta V_{\text{det}}}{V_T}\right)\mathbb{I}_0\left(\frac{\hat{V}_{\text{dm}}}{V_T}\right). \tag{16}$$

As no current is flowing in R_e, $V_e = V_{\text{det}} + \Delta V_{\text{det}}$. Solving this equation for the output voltage $V_{\text{det}} + \Delta V_{\text{det}}$ results in

$$V_{\text{det}} + \Delta V_{\text{det}} = V_b - V_T \ln\left(\frac{I_1/I_s}{\mathbb{I}_0\left(\hat{V}_{\text{dm}}/V_T\right)}\right). \tag{17}$$

To find the change in output voltage due to high-frequency excitation, ΔV_{det}, a reference level has to be established

$$V_{\text{ref}} = V_{\text{det}}(\hat{V}_{\text{dm}} = 0) = V_b - V_T \ln\left(\frac{I_1}{I_s}\right). \tag{18}$$

That results in the following input–output characteristic for the CC-based detector:

$$\Delta V_{\text{det}} = V_T \ln\left(\mathbb{I}_0\left(\frac{\hat{V}_{\text{dm}}}{V_T}\right)\right). \tag{19}$$

Although (19) is not very intuitive, it can already provide important insight. The circuit behavior cannot be influenced by design choices as long as I_1 is low enough to keep the transistors out of high-level injection, which would invalidate the current characteristic applied in (13).

There are two approximations for the logarithm of the Bessel function that result in equations for the square-law and peak detector ranges of the circuit

$$\ln\left(\mathbb{I}_0(x)\right) \approx \begin{cases} \dfrac{x^2}{4} - \dfrac{x^4}{64} + \cdots, & x \ll 1 \\ x - \ln\sqrt{2\pi x}, & x \gg 1. \end{cases} \tag{20}$$

The first approximation is a simple series expansion for small arguments, whereas the second is based on an approximation of the Bessel function for large arguments that can be found in literature [44]. Using these two approximations on (19) yields

$$\Delta V_{\text{det}} \approx \begin{cases} \dfrac{V_T}{4}\left(\dfrac{\hat{V}_{\text{dm}}}{V_T}\right)^2, & \hat{V}_{\text{dm}} \ll V_T \\ \hat{V}_{\text{dm}} - V_T \ln\sqrt{2\pi\,\hat{V}_{\text{dm}}/V_T}, & \hat{V}_{\text{dm}} \gg V_T. \end{cases} \tag{21}$$

This shows that the CC-based detector has two operation ranges. For weak input signals, it exhibits a square-law behavior. When the input signal gets larger, it morphs into a peak detector. Meyer [46] showed that the peak detector model is not sufficiently accurate when the logarithmic correction term is omitted.

The normalized complete model for the CC-based detector from (19) is plotted in Fig. 6 together with its approximations (21) at 300 K. We can use the PPE defined in (1) to judge the quality of the approximations. Assuming that PPE $\leq \pm 1$ dB as an acceptable error, the square-law model follows

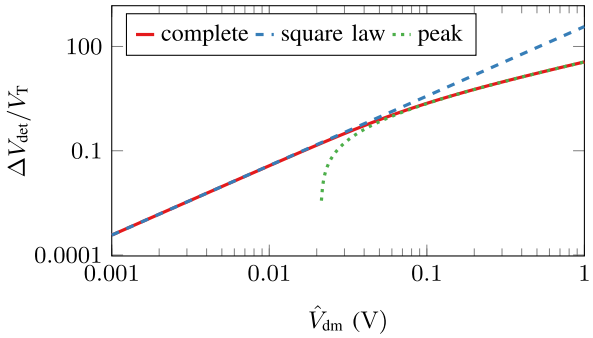

Fig. 6. Plots of the models for the CC-based detector.

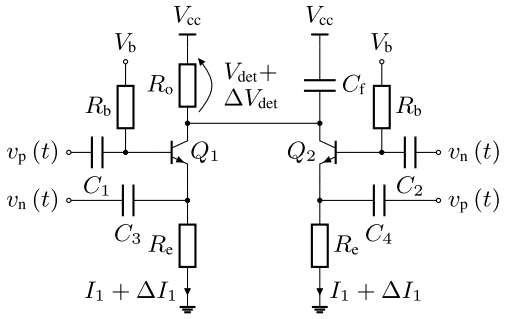

Fig. 7. CE-based detector concept.

the complete model up to an input amplitude of approximately 60 mV, whereas the peak detector approximation is valid for amplitudes larger than 40 mV. As we will discuss in the following, in practice, the lower limit of the square-law range is set by mismatch and noise. The upper end of the peak detector range is bounded by the base–emitter voltage of Q_1 and Q_2, i.e., $\Delta V_{\text{det}} < V_b - V_{\text{det}}$. This also means that when $V_b = V_{\text{cc}}$ and when using a low-voltage current source, the supply voltage of this circuit can be quite low without impacting the dynamic range of the detector. Hence, the architecture is especially interesting for low-voltage, low-power operation.

B. CE-Based Detector

The second architecture derived from the differential power detector concept is given in Fig. 7. It will be called CE-based, architecture in the following. In contrast to the CC-based circuit, the current in the transistors is not fixed and a load resistor R_o at the shorted collectors of Q_1 and Q_2 is used to convert the current into an output voltage. The filter capacitor C_f is placed in parallel with the output resistor. Small resistors R_e are connected between the emitters of Q_1, Q_2, and ground, allowing the emitter potential to change with the input signals.

From (14) and (15), the quiescent current in each of the two transistors is equal to I_1 when $V_b = V_T \ln(I_1/I_s) + R_e I_1$. This leads to

$$I_1 + \Delta I_1 = I_1 \exp\left(\frac{R_e I_1 - R_e(I_1 + \Delta I_1)}{V_T}\right)\mathbb{I}_0\left(\frac{\hat{V}_{\text{dm}}}{V_T}\right) \tag{22}$$

because $V_e = R_e(I_1 + \Delta I_1)$. The change in current ΔI_1 can be found with the help of the principal branch of the Lambert W

function W_0 [47]. This function, also called product logarithm, is the inverse of $f(x) = x \cdot \exp(x)$

$$\Delta I_1 = \frac{V_T}{R_e} W_0\left(\frac{R_e I_1}{V_T} \exp\left(\frac{R_e I_1}{V_T}\right) \mathbb{I}_0\left(\frac{\hat{V}_{\mathrm{dm}}}{V_T}\right)\right) - I_1. \quad (23)$$

The most complete equation for the change in output voltage due to the high-frequency excitation is found multiplying ΔI_1 by $2R_o$

$$\Delta V_{\mathrm{det}} = 2R_o\left[\frac{V_T}{R_e} W_0\left(\frac{R_e I_1}{V_T} \exp\left(\frac{R_e I_1}{V_T}\right) \mathbb{I}_0\left(\frac{\hat{V}_{\mathrm{dm}}}{V_T}\right)\right) - I_1\right]. \quad (24)$$

Implicitly assumed is a reference level for this detector architecture given by

$$V_{\mathrm{ref}} = 2R_o I_1. \quad (25)$$

In contrast to the CC-based architecture, series approximation for small arguments is the only option to simplify (24)

$$W_0(a\,\mathbb{I}_0(x)) \approx W_0(a) + \frac{1}{2}\frac{W_0(a)}{1+W_0(a)}\frac{x^2}{2} - \cdots \quad (26)$$

Application of this approximation gives the desired square-law characteristic

$$\Delta V_{\mathrm{det}} \approx \frac{1}{2}\frac{R_o I_1}{1+\frac{R_e I_1}{V_T}}\left(\frac{\hat{V}_{\mathrm{dm}}}{V_T}\right)^2 \quad (27)$$

$$\approx \frac{1}{2} R_o I_1 \left(\frac{\hat{V}_{\mathrm{dm}}}{V_T}\right)^2, \quad R_e I_1 \ll V_T. \quad (28)$$

The second approximation (28) assumes that the feedback introduced by R_e is negligible. This will often be the case in practice: As explained before, I_1 should be chosen low so that the transistor's current characteristic is not impacted by high-level injection. In addition, we will see in Section VI that setting $R_e = 50\ \Omega$ is beneficial for wideband input matching.

In contrast to the CC-based detector, the CE-based detector allows tuning of the output voltage range via R_o and I_1. Furthermore, the ratio of both detectors' output voltages in the square-law range, (28) divided by (21), is

$$\frac{\Delta V_{\mathrm{det,CE}}}{\Delta V_{\mathrm{det,CC}}} = \frac{2R_o I_1}{V_T}. \quad (29)$$

For the same input power, the CE-based detector typically has a higher output voltage than the CC-based one (output resistors are in the kiloohm range with quiescent currents of tens of microamperes, $V_T \approx 26$ mV at room temperature).

Both models (24) and (28) normalized to $2R_o I_1$ are shown in Fig. 8 at $T = 300$ K, $R_e = 50\ \Omega$, and $I_1 = 20\ \mu$A. The error in amplitude measurement using the square-law model is below 1 dB for $\hat{V}_{\mathrm{dm}} < 55$ mV, which is comparable to the CC-based detector. However, in both simulation and measurement, larger square-law ranges than this can be observed (see Section VIII). The reason for this behavior, not found in the other architecture, stems from the fact that the collector current in the transistors is not constant. High-level injection effects already influence the I–V characteristic of the transistor for currents around ≈100 μA.

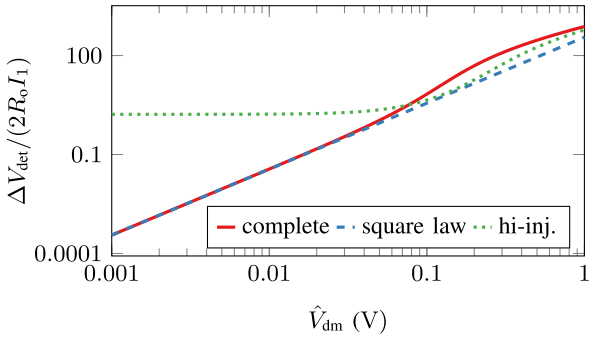

Fig. 8. Plots of the models for the CE-based detector.

A simplified model for the collector current under high-level injection conditions is [48]

$$I_{c,\mathrm{hi}} = \sqrt{I_s I_K}\,\exp\left(\frac{V_{\mathrm{be}}}{2V_T}\right) \quad (30)$$

where I_K is the high-level injection knee current. This changes the detector output equation to

$$\Delta V_{\mathrm{det,hi}} = 2R_o\left[\frac{2V_T}{R_e}\cdot W_0\left(\frac{R_e}{2V_T}\sqrt{I_1 I_K \exp\left(\frac{R_e I_1}{V_T}\right)}\,\mathbb{I}_0\left(\frac{\hat{V}_{\mathrm{dm}}}{V_T}\right)\right) - I_1\right]. \quad (31)$$

This model is also plotted in Fig. 8 assuming that $I_K = 150\ \mu$A. In reality, the current characteristic of the transistor transitions smoothly from the Shockley equation to the high-level injection characteristic resulting in a smooth transition between models (24) and (31). In effect, the square-law range of the detector gets extended to up to $\hat{V}_{\mathrm{dm}} \approx 200$ mV as the onset of high-level injection effects counters the steeper slope predicted by the complete model around $\hat{V}_{\mathrm{dm}} = 0.1$ V in Fig. 8. The result is a significantly wider square-law range compared to the CC-based architecture. Much higher inputs are difficult to achieve in practice as the supply voltage, which is capped due to reliability concerns and limits the maximum value of $V_{\mathrm{det}} + \Delta V_{\mathrm{det}}$.

IV. Temperature and Process Variation

Temperature effects on the detector characteristic in both circuits are well captured by (21) and (28). Because (28) contains a $1/V_T^2$-term, the largest temperature dependence is expected from the CE-based detector. In its square-law range, the CC-based detector is slightly more robust against temperature variation as one occurrence of V_T cancels in (21). When this detector is driven into its peak range, the temperature variation becomes even less because only the logarithmic correction contains V_T-dependent terms. Due to the $\hat{V}_{\mathrm{dm}}/V_T$-ratio under the logarithm, the temperature dependence in the peak range decreases with input power. Finally, the crossover-point between the two operating regions also varies with temperature because the approximations depend on the same $\hat{V}_{\mathrm{dm}}/V_T$-ratio.

Fig. 9 shows the PPE over input power in the automotive temperature range (−40 °C − 125 °C) calculated from the

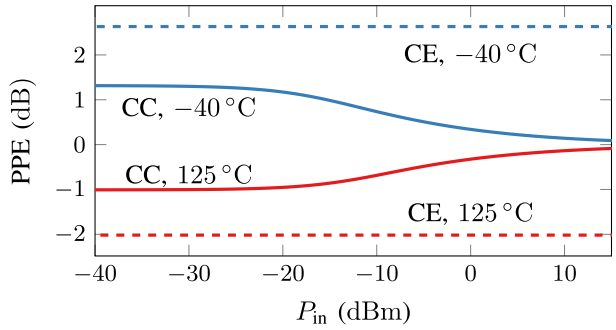

Fig. 9. Temperature dependence of both detector types.

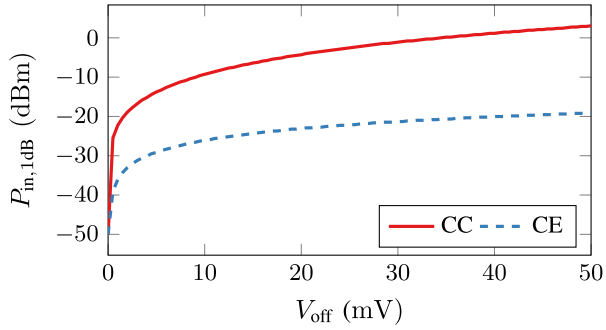

Fig. 10. Input power at which |PPE| ≤ 1 dB depending on the offset voltage.

model equations. For the CE-based detector, the uncertainty is larger than 4 dB. In accordance with the analysis above, the CC-based detector fares better, almost staying within ±1 dB in its square-law range, improving with input power. The error is the lowest when the detector is deep into its peak range. Clearly, the temperature errors of square-law detectors are so large that temperature compensation [28], [49], [50] is required to keep the accuracy specifications discussed in Section II-C.

In contrast to temperature effects, process shifts are not well-covered by (21) and (28). In fact, (21) for the CC-based detector does not contain any process-dependent terms. For the CE-based detector, some variation due to the output resistor R_o and the quiescent current I_1 can be expected. Nevertheless, process variation influences the detector characteristic by shifting the operating points of the detector, either directly via the I–V curves of the hetero-junction bipolar transistors (HBTs) or the bias resistors. In addition, the mismatch between the two halves of the detectors disturbs the symmetry that has been assumed in the model derivations. These effects are analyzed with simulations and measurements in Section VIII.

A very important process-dependent effect, limiting the detectors' dynamic range toward low input powers, is reference offset. This happens when the reference voltage (18) and (25) is not equal to the detector output voltage at zero input power

$$V_{\text{off}} = V_{\text{det}}(\hat{V}_{\text{dm}} = 0) - V_{\text{ref}}. \tag{32}$$

This offset voltage appears as an additive term in ΔV_{det}, see (21) and (28). In effect, the input amplitude can only be detected when the $\hat{V}_{\text{dm}}$-dependent terms are much larger than V_{off}.

Fig. 10 shows this effect. It plots the minimum power for which |PPE| is smaller than 1 dB depending on the offset value. Even in the CE-based detector, which has the higher output voltage for small inputs according to (29), the minimum detectable input power is limited to approximately −30 dBm for realistic offset values $\lesssim$10 mV. The CC-based detector performs much worse having trouble to detect powers smaller than −10 dBm for the same offset. Consequently, offset calibration [50] is a very important step to ensure that square-law detectors can reliably cover all BIST use cases discussed in Section II-B. For small input powers, the CE-based architecture is the better choice as it is more robust against residual offset.

V. Noise

When it comes to noise analysis, the main point of interest is the output voltage noise of the detectors. It is measured at much lower frequencies compared to the input signal. In BIST, the time available to take a measurement is in the millisecond range [51]. Accordingly, the noise power at the detector output can be reduced by averaging over this time period. In all application scenarios from Fig. 1, the signal-to-noise ratio at the detector input is high; the nonlinear noise conversion in the detector can be neglected (see [52] for a derivation of the noise conversion in both square-law and peak detectors).

Beginning with the CC-based detector, in the relevant frequency range the input coupling capacitors C_1–C_4 from Fig. 5 can be considered open. The same is true for the filter capacitor C_f. It is large enough to remove high-frequency content from the output voltages. However, due to area constraints, it cannot be large enough to be relevant below approximately 10 MHz. The noise equivalent model of the CC-based detector in Fig. 11(b) considers the noise of resistors R_b and R_e and the shot noise of Q_1. In practice, the current source I_1 is implemented using an nMOS current mirror. Its noise contribution is dominated by flicker noise and can be modeled by a drain-referred current source (g_{MOS} is the transconductance of the current mirror transistor, K is the flicker noise fitting parameter, C_{ox} is the gate capacitance per unit area, and W and L are the transistor's width and length, respectively). The output resistances of both transistors are neglected in the following.

Due to the circuit's symmetry, we can find the noise at the detector output via the Norton equivalent of both circuit halves along the vertical symmetry axis. It is given as

$$\overline{v_{\text{det}}^2} = 2\,\overline{i_n^2} \cdot \left(\frac{Z_n}{2}\right)^2 \tag{33}$$

$$= \frac{(kT)^2}{q\,I_1} + 2\,kT(R_e + R_b) + \left(\frac{g_{\text{MOS}}}{g_m}\right)^2 \frac{K}{2WLC_{\text{ox}}} \frac{1}{f} \tag{34}$$

where $g_m = I_1/V_T$ is the transconductance of Q_1. For ΔV_{det}, the noise of the reference level, having the same spectral density as (34), effectively doubles the noise in the output characteristic

$$\overline{\Delta v_{\text{det}}^2} = 2 \cdot \overline{v_{\text{det}}^2}. \tag{35}$$

The main noise contributors are the flicker noise of the nMOS current source together with the noise of the base resistor R_b. The latter has to be large to isolate the high-frequency

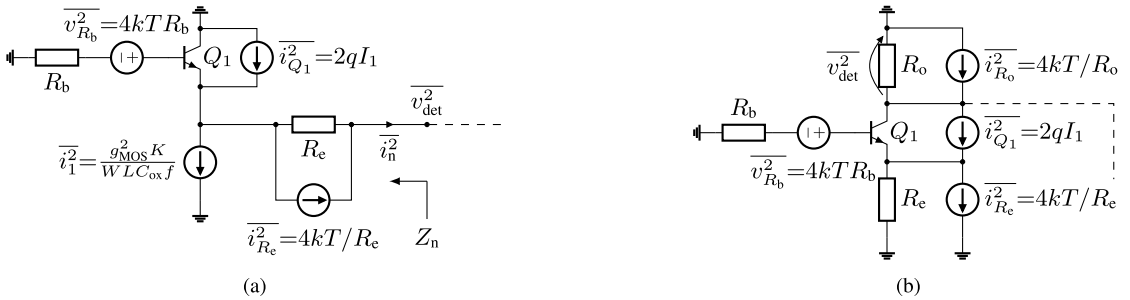

Fig. 11. Equivalent circuits for output noise calculation of (a) CC- and (b) CE-based detectors.

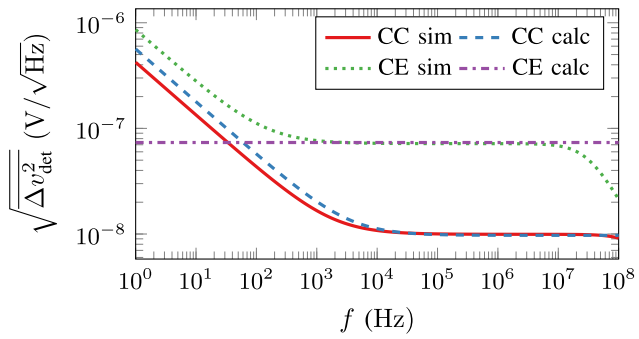

Fig. 12. Output noise voltage densities of both detectors comparing the simulations to the hand-calculation models.

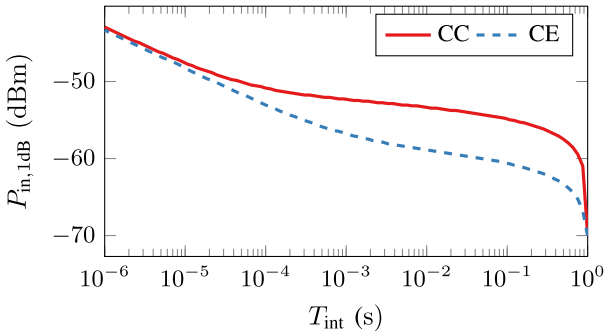

Fig. 13. Input power at which |PPE| $\leq$ 1 dB depending on the noise integration time, i.e., the measurement duration, for both detectors.

input signal from the bias voltage. In case a reduction of the output noise is desired, the resistor can be replaced with a reactive bias tee at the expense of a reduced high-frequency bandwidth (refer to the following for an analysis of the input impedance). Another measure to reduce the noise is to implement the current source with a bipolar current mirror, which drastically lowers its flicker noise contribution but requires a larger supply voltage. Unfortunately, the typically small bias currents in power detectors result in a low transconductance g_m of Q_1. Consequently, the suppression of the current source flicker noise as well as the shot noise from Q_1 is rather low.

The CC-based detector is simulated with $I_1 = 20\ \mu$A, $R_e = 50\ \Omega$, and $R_b = 5\ \text{k}\Omega$. The dimensions of the nMOS in the current source are $W = L = 5\ \mu$m, and the flicker noise coefficient K is determined from the simulation. Fig. 12 compares hand-calculation model and simulation. The model hits the simulation very well except for a small difference at low frequencies due to the omission of the flicker noise of the HBT.

Fig. 11(b) shows the equivalent circuit model of the CE-based detector, which has been constructed under the same assumptions as for the CC-based circuit. The output resistances seen in the collectors of the HBTs can be assumed infinite, while the noise contributions of their collector currents add. This leads to

$$\overline{v_{\text{det}}^2} = \left(\frac{R_o}{1+g_m R_e}\right)^2 4qI_1 + \cdots + \left(\frac{g_m R_o}{1+g_m R_e}\right)^2 8kT\,(R_e+R_b) + 4kT\,R_o. \quad (36)$$

Again, the noise spectral density of ΔV_{det} is calculated according to (35).

For the typical low bias currents and small emitter resistors, $g_m \cdot R_e \ll 1$. It becomes clear that the CE-based detector suffers from a higher noise floor compared to the CC-based circuit. This is mainly due to the output resistor appearing as a "gain term." Luckily, the significant flicker noise contribution from the MOS transistor that plagues the CC-based detector is not present in the CE-based circuit. Fig. 12 also contains the spectral densities of hand calculation and simulation for the CE-based detector alongside the CC-based results discussed previously. The noise floor is correctly predicted by (36). At low frequencies, the simulation and hand-calculation models diverge because the HBT's flicker noise contribution was omitted in the hand calculation. However, due to the low flicker noise corner of the device, the error in the integrated output noise is insignificant.

Talking in terms of PPE, noise presents a lower limit to the dynamic range of the square-law ranges of both power detectors that is similar to the effect of the offset discussed in Section IV. If we integrate the simulated noise spectral densities shown in Fig. 12 for different measurement durations, we can find a lower boundary for the input power for which |PPE| $\leq$ 1 dB. This minimum input power depending on the integration time is plotted in Fig. 13. Even for very short time spans of 1 μs per power measurement, the sensitivity of both detectors is around -43 dB. Compared to Fig. 10, for a lot of practical measurement durations and offset values, the lowest detectable power is dominated by offset and not by noise. After offset compensation, the CE-based detector is better suited to detecting low-power signals as the current source flicker noise in the CC-based detector drives up the overall noise level in the relevant frequency range.

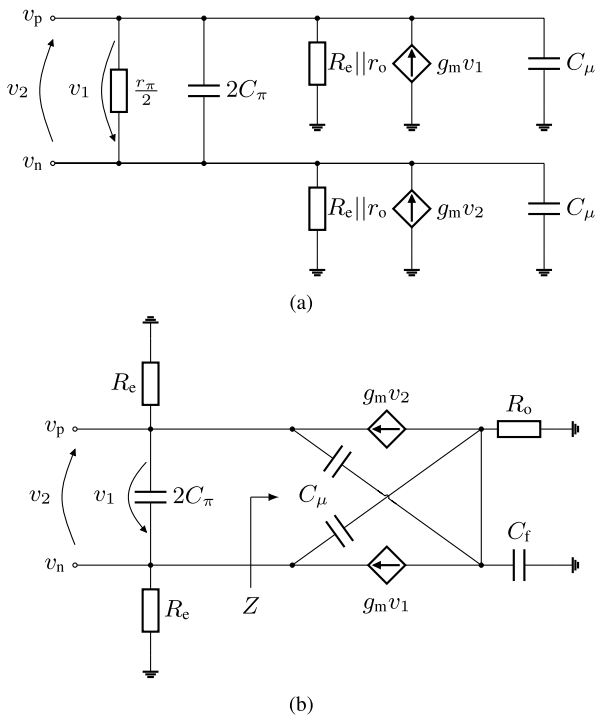

Fig. 14. Small-signal equivalent circuits for calculating the differential-mode input impedances of (a) CC- and (b) CE-based detectors.

VI. Input Impedances

As discussed in Section II, the input impedance of a detector can determine for which application it is best suited. As we will see next, the differential detector architecture lends itself to scenarios requiring matched interfaces. Nonetheless, they could also be used in conjunction with a sufficiently high-impedance coupler.

Differential-mode small-signal equivalent circuits of both detectors are given in Fig. 14, where the small-signal parameters of the transistors have their usual meanings. The corresponding common-mode representations are not shown but can easily be derived. Note that the small-signal input impedance of a power detector has to be taken with a grain of salt as the small-signal parameters are a function of the time-average terminal voltages and currents that change with input power.

Beginning with Fig. 14(a) for the differential-mode of the CC-based detector, r_π and r_o can be neglected from the start as they are typically much larger than R_e. This results in

$$Z_{\text{dm,CC}} = \frac{2\left(R_e||\frac{1}{2g_m}\right)}{1+j\omega\left(R_e||\frac{1}{2g_m}\right)(4C_\pi+C_\mu)}. \tag{37}$$

The transconductance $g_m = I_1/V_T$ will be small for the typically small bias currents in the detector. Therefore, setting $R_e = 50\ \Omega$ ensures wideband differential-mode input matching to a 100-Ω system impedance as the intrinsic capacitances of modern HBTs are also very small.

Calculating the common-mode impedance of the CC-based detector yields

$$Z_{\text{cm,CC}} = \frac{1}{j\omega(2C_\mu+C_f)}\frac{1+j\omega\frac{R_e}{2}C_f}{1+j\omega\frac{R_e}{2}\frac{2C_\mu C_f}{2C_\mu+C_f}}. \tag{38}$$

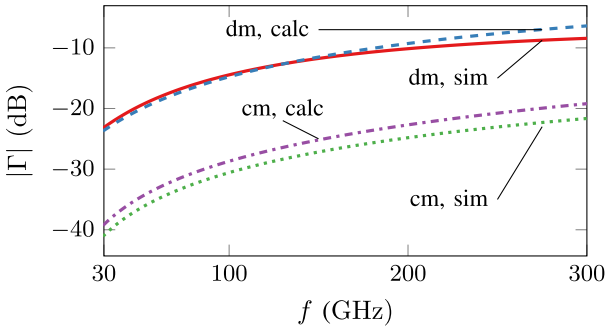

Fig. 15. Comparison of the simulated to the calculated differential- and common-mode input reflection coefficients (same for both architectures).

As the filter capacitor C_f has to be very large to remove all time-varying signal components from the output, this simplifies to

$$Z_{\text{cm,CC}} \xrightarrow{C_f\to\infty} \frac{R_e}{2}\frac{1}{1+j\omega R_e C_\mu} \tag{39}$$

which shows that for $R_e = 50\ \Omega$, the detector is matched in both modes.

Finding the differential-mode input impedance of the CE-based detector from Fig. 14(b) is a little more involved due to the cross-coupled C_μ. For $C_f \gg C_\mu$, the impedance Z seen into the emitters is given by

$$Z \approx \frac{1/g_m}{1+j\omega\frac{C_\mu}{2g_m}}. \tag{40}$$

The input impedance can then be found as the parallel combination $Z_{\text{dm,CE}} = 2(R_e||1/(j\omega 4C_\pi)||Z/2)$

$$Z_{\text{dm,CE}} \approx \frac{2\left(R_e||\frac{1}{2g_m}\right)}{1+j\omega\left(R_e||\frac{1}{2g_m}\right)(4C_\pi+C_\mu)} \tag{41}$$

which is the same result as for the CC-based detector (37).

Finally, the CE-based detector's common-mode input impedance is found as

$$Z_{\text{cm,CE}} = \frac{\frac{R_e}{2}\left(1+j\omega(C_f+2C_\mu)\right)}{1+j\omega\left(R_o(C_f+2C_\mu)R_eC_\mu\right)+(j\omega)^2R_oR_eC_\mu C_f}. \tag{42}$$

For $C_f \gg C_\mu$ and $R_o \gg R_e$, this impedance, too, is formally the same as the one of the CC-based detector

$$Z_{\text{cm,CE}} \approx \frac{R_e}{2}\frac{1}{1+j\omega R_eC_\mu}. \tag{43}$$

Equations (37), (39), (41), and (43) reveal an important characteristic of the differential power detector architecture that makes it very suitable for BIST. The detector achieves good input matching in both differential and common modes by setting R_e to 50 Ω. This means that large-area matching networks are not required and the detectors can be very compact.

Both detectors are simulated for $I_1 = 20\ \mu$A at 300 K, which gives $1/g_m \approx 1.3\ \text{k}\Omega \gg 50\ \Omega$. The intrinsic capacitances C_μ and C_π in this operating point take values of approximately 2.4 fF (for minimum-size HBTs), and C_f is set to an ideal ac short. Fig. 15 compares the simulated

differential- and common-mode input reflection coefficients to those calculated with (37) and (41), and (38) and (42) in the millimeter-wave frequency range. The numeric differences between the two detector architectures are so small that only one simulated and calculated curve is shown for each mode. The agreement between the simulations and simple hand calculations is very good. Up to 200 GHz, the simulations predict a differential-mode input reflection coefficient better than −10 dB, whereas the matching in common mode is below −20 dB at least up to 300 GHz. In practice, the parasitics of the circuit layout have to be controlled accurately to achieve this degree of performance. If better matching is required, as discussed in Section II-C, a parallel inductance at the input can improve the matching further by resonating with the parasitic transistor capacitances at the expense of bandwidth and circuit area.

VII. Circuit Implementations

For experimental verification, more practical versions of the two circuit concepts from Figs. 5 and 7 are developed. Their schematics are shown in Fig. 16. Both circuits are operated from a 3.3-V supply and contain a reference path, which is identical to the main path but not connected to the high-frequency excitation, to establish the reference levels (18) and (25). All input coupling capacitors C_1–C_4 are set to 200 fF and C_f is 300 fF, its size mainly limited by space constraints in the layout that is designed for compatibility with the directional couplers published in [35]. The bias voltages V_1, V_b, and V_{cas} are generated on-chip to establish the bias currents I_1 in transistors Q_1 and Q_2. $R_e = 50\ \Omega$ ensures that the detectors are matched at their inputs. At the same time, the value is low enough to support the approximation (28) in the CE-based detector. Minimum-size HBTs are chosen to minimize the parasitic capacitances C_μ and C_π that influence the cutoff frequencies of the differential-mode input impedances (37) and (41).

According to (21) and (29), the CC-based detector of Fig. 16(a) is naturally suited to process larger input signals. It is impossible to influence its input–output behavior with design choices other than setting the quiescent current to a value low enough to not introduce high-level injection effects. MOS transistors M with both width and length equal to 5 μm are used to establish a bias current $I_1 = 20\ \mu$A. The large transistor dimensions in the current source help to minimize the flicker noise contribution in (34).

As the CE-based detector allows for more flexibility in its design, see (28), it is targeted to cover the lower part of the potential input power range. To safely cover all use cases from Section II, a minimum input power of at least −40 dBm is desirable. To be compatible with the 3.3-V supply voltage, a system requirement, the cascode transistors Q_5 have to be added to the detector [53] as the collector–emitter breakdown voltage of the HBTs is only 1.6 V. Unfortunately, this limits the voltage swing at the output nodes if the output resistor R_o is directly attached to the collectors of Q_5. Because there is a margin in the lower input power limit due to noise (see Fig. 13) and offset compensation is required anyway, it was decided to use the current mirrors M_1 and M_2 to decouple the output

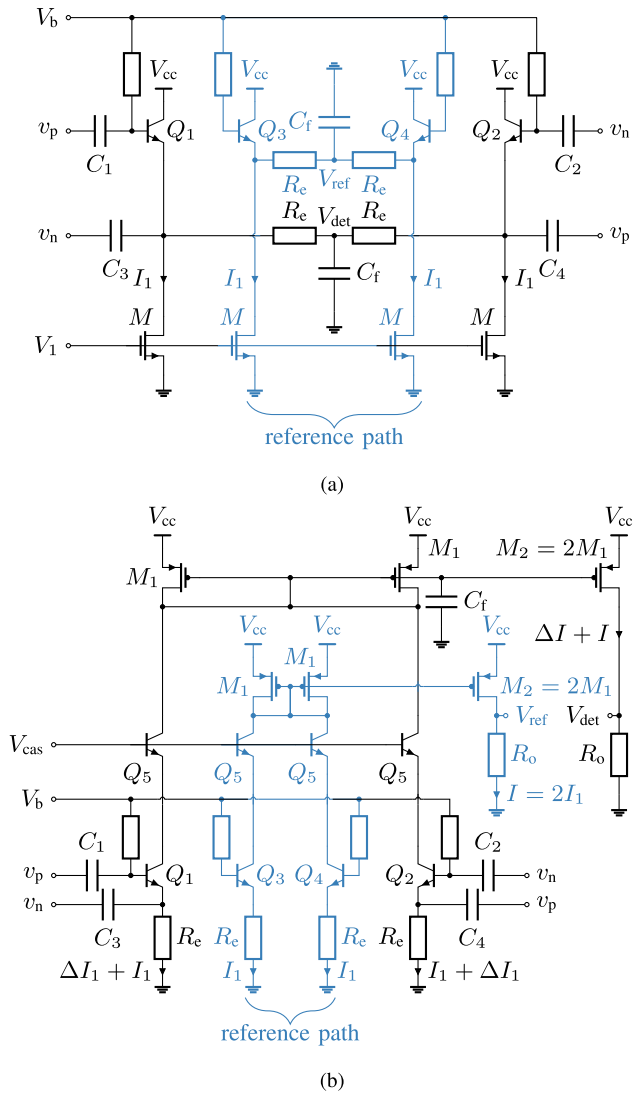

Fig. 16. Complete schematics of implemented (a) CC- and (b) CE-based (modified from [20]) detectors.

voltage from the detector core. This achieves higher maximum input power at the expense of added flicker noise and mismatch due to the current mirror. Using long-channel devices with $W_1/L_1 = 10/3\ \mu$m ensures that the penalty is minimal. For higher output voltage at the low end of the input range, the detector is biased at a slightly higher current of 30 μA than the CC-based detector according to (28). The output resistor is chosen as $R_o = 5\ \text{k}\Omega$.

For the layout of the detectors, two conflicting requirements have to be considered. The main and reference paths need to be located closely to each other to ensure good matching and thermal coupling between them. However, it is imperative that no high-frequency signal leaks into the reference path. Another important consideration is that the cross-coupled connections from the input signals to the base–emitter junctions and the emitter resistors have to be as electrically short and symmetric as possible. Parasitic inductances can introduce imbalances into the differential signal and limit the operating frequency range by affecting the input impedances.

Fig. 17(a) shows the layout of the input coupling network of both detectors. It was decided to use the fourth metal

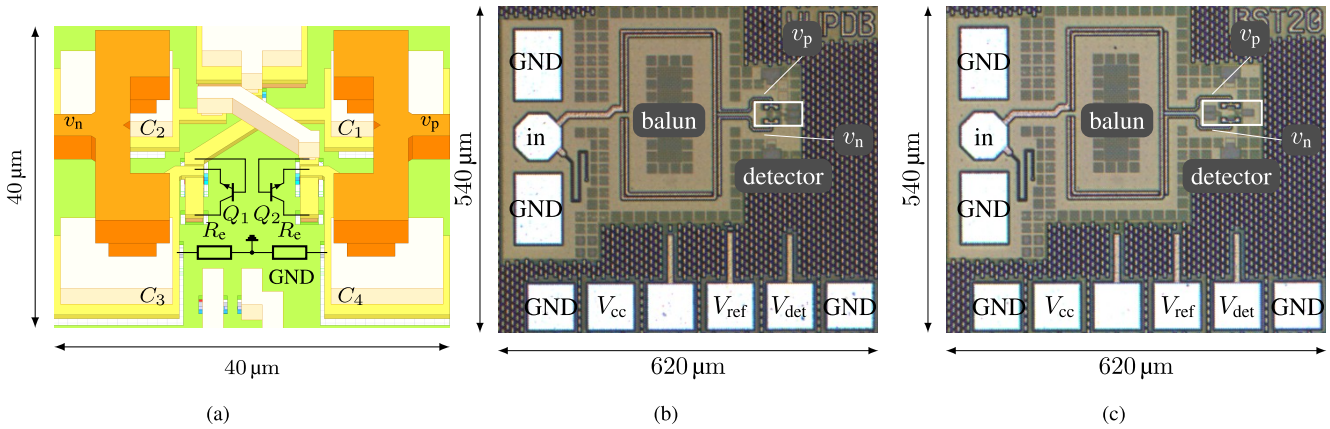

Fig. 17. (a) Layout of the input coupling network (from [20]) and fabricated test structures for (b) CC-based and (c) CE-based (from [20]) detectors.

layer (green) as the ground plane. This enables placing the transistors and resistors of the reference path below the ground plane right next to the main path devices. The HBTs and emitter resistors are placed in-between the coupling capacitors C_1–C_4 onto which the two input signals v_p and v_n are split. From the capacitors, the signals are routed to the base and emitter contacts of Q_1 and Q_2 as well as the emitter resistors. All these connections are shorter than 15 μm and therefore less than $\lambda/100$ at 81 GHz. The only asymmetry in the layout is introduced via the connections between C_1 and C_2 and the bases of Q_1 and Q_2. As these are also short, no significant impact on the performance is observed.

VIII. Experimental Results

Test structures for both detectors (see Fig. 17) were fabricated in IHP's SG13G2 SiGe technology with $f_T/f_{\max} = 300$ GHz/500 GHz [54]. The detector cores themselves only occupy a die area of 50 $\times$ 70 μm (CC-based) and 50 $\times$ 105 μm (CE-based). As discussed before, the low area consumption can largely be attributed to the fact that input matching is achieved by setting R_e to 50 Ω.

Because millimeter-wave measurement equipment is mostly single-ended, it was decided to place the Marchand balun presented in [30] in front of the detectors. The balun loss of 2.1 dB and the insertion losses introduced by cables and probes of 2.7 dB are deembedded from all measurements except where specified otherwise. At 81 GHz, the simulated differential-to-common-mode conversion of the balun is -27 dB, low enough not to introduce significant error. Unfortunately, the balun could not be deembedded from the reflection coefficient measurements so that the small-signal input impedance calculations cannot be verified directly. To match the hand-calculated input–output characteristics to simulation and measurement another 0.5 dB of loss due to the input coupling capacitors has to be included.

A. Input–Output Characteristics

Nine samples of each detector have been measured using a Keysight PNA-X whose frequency range has been extended up to 120 GHz with the corresponding Keysight modules. Their input–output behavior at 79 GHz is given in Fig. 18 together

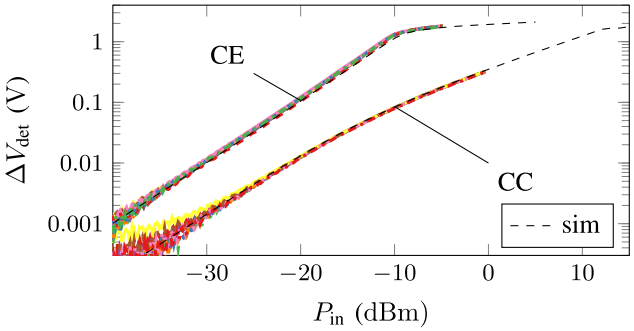

Fig. 18. Measured input–output characteristics of the CC-based and CE-based detectors at 79 GHz. The CC-based circuit transitions from square law to peak detector behavior around -17 dBm, whereas the CE-based architecture constitutes a pure square-law detector.

with the simulation result. The maximum available power of the measurement system was limited to approximately 0 dBm at the detector input. For the CC-based detector, this means that the transition between the square-law and peak detector ranges is covered by the measurement. However, the upper end of the peak detector range has to be inferred from the simulation. The dynamic range of the CE-based detector is completely covered. After removal of the offset (see Section VIII-C) from the curves in Fig. 18, the lower end of the dynamic range is limited by the noise of the detectors and the measurement system.

In the case of the CC-based detector, the PPE between simulation and all measured samples is within the ±1-dB range for $P_{in} \gtrsim -32$ dBm. The upper end of the square-law range is around -15 dBm, which is close to the theoretically predicted value, calculated in Section III. This results in a square-law dynamic range of 17 dB. The measurement shows peak detector behavior between -21 and 0 dBm. The simulation predicts the detector saturating around 14 dBm of input power. If this upper limit is accurate, the peak detector dynamic range is 35 dB. As expected, the CE-based detector is better suited for small input signals as all measured samples are already within PPE $= \pm 1$ dB around $P_{in} = -37$ dBm. The upper limit of this detector's square-law range is around -7 dBm, yielding 30 dB of dynamic range. The measured dynamic ranges of both detectors are well suited to cover all application cases from Section II.

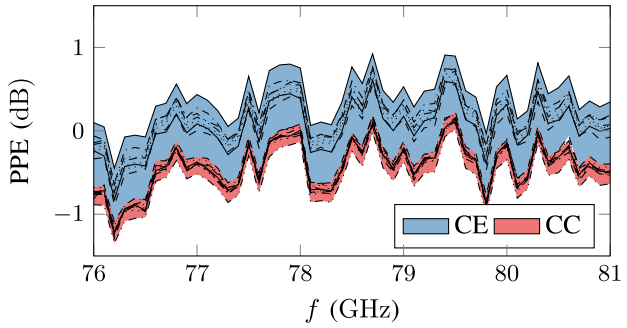

Fig. 19. Measured frequency behavior of the CC-based (at $P_{\text{in}} = -16.8$ dBm) and CE-based (at $P_{\text{in}} = -26.8$ dBm) detectors. Black curves are the measured samples, while the red and blue curves visualize the spread of the PPE over these samples.

B. Frequency Behavior

In a BIST context, the frequency of the signal under test is sometimes not known exactly. In the worst case, the previously discussed input–output curves at 79 GHz might have to be used to extract the power of a signal at 76 or 81 GHz. To characterize the error that can be expected from this approach, a fixed input power is applied to the detector while sweeping the frequency. Comparing the output power calculated from the input–output characteristics (Fig. 18), to the applied power, the PPE over frequency can be calculated. Note that this PPE includes the effect of the frequency-dependent input impedance from (2). Accordingly, a stable PPE over frequency validates the flat frequency characteristic of the input impedance shown in Fig. 15.

Fig. 19 shows a plot of the resulting PPE curves for all nine samples of both circuits in the automotive radar band. The input power is adjusted for the two different architectures to achieve the same $\Delta V_{\text{det}} \approx 25$ mV (P_{in} is -16.8 dBm for the CC-based and -26.8 dBm for the CE-based detector). In the 76–81 GHz band, the error is largely within ± 1 dB. The CC-based circuits dip slightly below -1 dB around 76.2 GHz. However, the errors of this detector are not centered around 0 dB. Consequently, choosing a different reference frequency instead of 79 GHz would improve the accuracy of the detector. The measured spikes are always located at the same frequency point independent of the sample or detector type. Consequently, they cannot be explained by noise. Because the detector is very sensitive to small input power variations, they most likely originate in the millimeter-wave signal source.

The spread of the PPE at each frequency point is larger for the CE-based detector compared to the CC-based one. This is due to the detector's larger sensitivity to process variation, which will be discussed in the following.

C. Process and Temperature Sensitivity

As discussed in Section IV, the removal of the offset voltage between the main and reference paths defined in (32) is paramount when measuring low input powers. The measured offset voltages of the nine samples for each detector are given in Table I. For the CC-based detector, the average offset voltage of the samples is only 0.5 mV. This is due to the fact that the HBTs in the main and reference paths that are laid out directly next to each other and track very well. In addition, the output voltage is the base–emitter voltage of Q_1, which logarithmically depends on the collector current. This logarithm effectively moderates offset components introduced by the mismatch in the bias currents I_1. Nevertheless, according to Fig. 10, an uncompensated offset voltage of 0.5 mV would already limit the lower end of the dynamic range to -25 dBm (as opposed to the -32 dBm determined in Section VIII-A).

TABLE I
MEASURED OFFSET VOLTAGES FOR BOTH DETECTORS

sample	CC-based (mV)	CE-based (mV)
1	1.54	−0.69
2	0.31	−4.91
3	−0.75	−7.72
4	−0.69	−26.46
5	0.01	−15.82
6	0.45	−14.04
7	1.55	−3.70
8	1.11	−5.78
9	0.98	−14.12

The offsets for the CE-based detector samples, given in Table I, show a larger spread compared to the CC-based one with a mean of -10 mV. This is in part due to the addition of the current mirrors M_1–M_2 in Fig. 16(b). As discussed in Section VII, the current mirror improves the upper end of the dynamic range at the expense of offset. In addition, as shown in (25) and (28), in this architecture, the value of the output resistor R_o and the bias current I_1 directly appear in the output and reference voltage. Therefore, a mismatch in their values between main and reference paths directly appears as offset. According to Fig. 10, an offset voltage of 10 mV limits the minimum input power to -26 dBm. With a measured minimum input power of -37 dBm (Section VIII-A), this means that removal of the offset improves the dynamic range of the CE-based samples by 11 dB on average.

Fig. 20(a) shows the PPE of the nine CC-based detector samples at 79 GHz over input power. Overlaid in red and blue are the maximum error ranges determined from the corner and a 1000-run Monte Carlo (MC) simulation. In these simulations, the process variation of all devices in the circuit has been included. Offset compensation was performed for the MC results and the measurements. As the error range predicted by process corners is larger than the one from MC simulation, this architecture is more susceptible to global process variations that affect all devices in the same way as opposed to local, device-to-device mismatch. The measured samples fall well into the range predicted by the simulations. Note that the measured sample-to-sample spread is very close to 0 dB. In any case, the PPE over process variations is well within ± 1 dB inside the detector's dynamic range.

The equivalent plots for the CE-based detector are given in Fig. 20(b). In this architecture, symmetry is more important compared to the CC-based one as mismatch in the current mirrors M_1 and M_2, between the resistors R_o, and quiescent currents I_1 in main and reference paths propagate onto ΔV_{det} according to (28). As the MC simulation includes local mismatch, it predicts a larger spread than the corner simulation, which only covers global shifts (except at large power outside

TABLE II
COMPARISON OF PUBLISHED MILLIMETER-WAVE POWER DETECTORS IN SiGe

	[21]	[22]	[55]	[56]	[57]	[23]	CC-based	CE-based
single-ended/differential	se	se	se	se	se	diff	diff	diff
architecture	CC	CE	CE	CE	CB	CE	CC	CE
samples	1	1	1	1	1	1	9	9
frequency (GHz)	72-82	76-81	100-130	110-170	50-67	20-44	76-81	76-81
PPE_{freq} (dB)	−2.1-0.5	-	−2.1-0.3	0.5-1.6[f]	−0.6-0.5	−1.8-2.9	−1.3-0.2	−1.3-0.9
dynamic range (dB)	35	30	38	> 25	38[a]	20	32[a](46)[b]	30
temperature (°C)	-	-	-	-	-	-	−40-125	−40-125
static power (mW)	0.6	0.9	0.1[c]	1	0.09[d]	5.2	0.5	0.5
area (mm^2)	0.1	0.11	0.06	0.02	0.006[e]	0.24	0.004	0.005

[a] combined square-law and peak range [b] upper limit from simulation [c] excluding biasing [d] no reference path
[e] no input matching [f] includes directional coupler

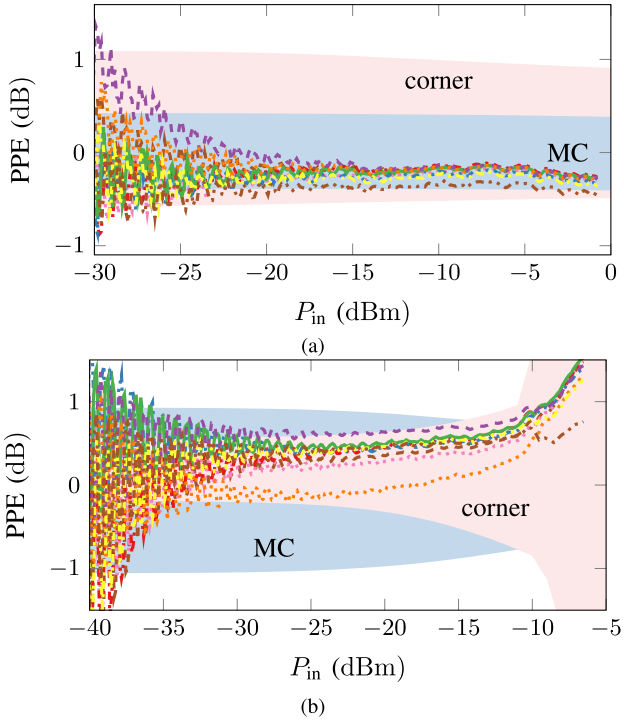

Fig. 20. Process variation of (a) CC- and (b) CE-based detectors. Lines are the measured samples. The ranges predicted by corner and MC simulation are overlaid in red and blue.

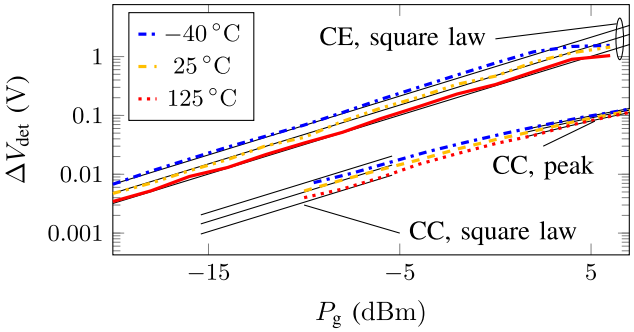

Fig. 21. Temperature dependence of both detectors in the automotive temperature range measured at 65 GHz. The measurements conform well to the theoretical behaviors overlaid in black.

the dynamic range of the detector). The measured samples fall into the narrower range predicted by the corner simulations. There is more sample-to-sample variation compared to the CC-based detector due to the aforementioned sensitivity to mismatch. Nevertheless, even the process-dependent error of the MC simulation is between −0.9 and +0.9 dB.

Due to limitations of the available measurement equipment, the temperature performance in the automotive temperature range, −40 °C to 125 °C, had to be determined at 65 GHz, below the intended band of operation. As the input–output behavior of the detectors (21) and (28) does not depend on frequency, i.e., frequency and temperature effects are not coupled, verifying the temperature characteristics predicted by these two equations at a lower frequency is unproblematic. The input tone was generated with a Keysight E8257D signal generator. For the thermal control, an ATT C200 temperature system was connected to the thermal chuck of the probe station. The diced samples were glued to a silicon wafer with thermally conductive glue to ensure that the sample temperature is the same as the chuck temperature. Because exact calibration of losses (including the balun loss) proved difficult with this measurement setup, the resulting curves in Fig. 21 refer to the available generator power P_g.

For the CC-based detector, the measurement setup was able to resolve the transition between the square-law and peak detector operating regions. In the peak detector range, the measured curves follow (21) closely. At low input power, the curves approach the square-law approximation; the models are accurate in the measured temperature range. The CE-based detector model from (28) predicts the measured curves well. Consequently, the calculated error ranges plotted in Fig. 9 are valid for the practical detector circuits. Compared to the process variation, which is largely within ±1 dB, as reported above, the temperature dependence has to be considered the main source of error, especially for square-law detectors. As already stated in Section IV, either analog [46], [49] or digital [20], [28] temperature compensation has to be used to achieve sufficient accuracy over temperature in practice.

IX. CONCLUSION AND DISCUSSION

From the system analysis in Section II, we have seen that the requirements that the BIST system is placed on power detection are difficult to cover with one single detector architecture. In a BIST covering the complete millimeter-wave transceiver, many detectors will have to be placed throughout the signal chain. The repeatability of the power

measurement, i.e., the stability and ease of calibration of the detectors, therefore becomes an important concern together with their performance. In this vein, Table II compares the two proposed power detectors to other published millimeter-wave detectors in SiGe. The work from [23] is the only other differential implementation above 30 GHz known to the authors. Its dynamic range is lower than all other circuits. The output voltage varies significantly with input frequency making it unsuitable for accurate power measurement.

Due to being extracted over multiple samples, the numbers for dynamic range and frequency variation of the proposed detectors are on the conservative side. Yet, they are competitive in dynamic range with the single-ended implementations. If the simulated upper input power of the CC-based detector is accurate, this architecture has the largest range of all architectures. When it comes to the PPE over frequency of the detector core, only the common-base circuit from [57] provides better frequency stability in its bandwidth. The D-band detector from [56] is integrated with a directional coupler, which is designed specifically to negate the frequency dependence of the detector core. As this approach achieves a very good frequency stability over a large bandwidth, the systematic codesign of detectors and coupler should be a focus of future research.

The static power consumption of both architectures is slightly lower compared to the two other detectors in the automotive radar frequency range [21], [22] although the differential approach naturally draws twice the current of a single-ended detector. In [55], only the power consumption of detector core and reference path is given leaving out the bias network, whereas work [57] is very low power as the detector does not contain a reference path. Finally, the proposed detectors have the smallest area footprint while delivering matched inputs because the input matching is achieved via R_e (in the table, care has been taken to extract the area of core detector and matching network for each published circuit where it was possible). A small area footprint is critical in a BIST context to minimize the overhead of the self-test.

The theoretical as well as measurement results in this work show that the main sources of error are process and temperature induced. These have a significant impact on the accuracy of transistor-based power detectors. In practice, the different error terms add up, meaning that the power measurement uncertainty without trimming or calibration will usually be in the range of several decibels. Without calibration of the offset term between the reference and main paths, the dynamic range of the detectors is severely limited. Future work should try to focus on robust detector architectures and low-overhead compensation of these effects.

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