Configurable Fault Tolerant Circuits and System Level Integration for Self-Awareness

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I. Introduction

Scaling minimum features of ICs down to the 10nm- area and below has allowed high integration rates in electronics. Scaling at supply voltages of 1V and below also implies a rising level of stress which drives aging effects that reduce switching speed and the expected life time. Additionally, vulnerability from particle radiation is increased. Hence, fault detection and on-line correction become a must for many applications. So far, focus has been on detection and correction of transient faults, such as single-event upsets (SEUs) and single event transients (SETs) induced by radiation [1]. The next problem of concern is stress-induced aging, where parameter deterioration plays a major role [2].

Methods targeting delay faults, single-event upsets and single-event transients work by observing the signal behavior in time without duplicating hardware [3] [4]. However, some faults are difficult to detect if they do not match a certain fault model. For example, SETs or delays that last more than about half a clock cycle are not easy to detect, since detection relies on wrong transitions within a clock interval.

Furthermore, not only fault tolerance but self-awareness becomes also an important property. Provided that by being aware of its own healthy state allows optimized configurations regarding system operation modes and configurable hardware mechanism.

In this paper we present (II) a preliminary work of an optimized combination of a low-power fault correction mechanism based on Muller-C Element [4] with more robust methods based in self-dual properties of circuits [5]; and (III) a system level integration overview of the mentioned circuits exploring configurations possibilities and operation modes.

II. Configurable Circuits for Fault Tolerance

Self-dual circuits are circuits in which by given input and output signals, if one inverts all the bits of the input, the output will be all inverted as well. So, with adequate support, this property can also be used for error detection [5] (e.g. Fig. 1a). Muller-C element (MC) is a hardware element which passes its inputs if they are equal, but it produces the previously stored value if inputs differ [4]. Thus, the MC potentially corrects transient glitches in the input signals (e.g. Fig. 1b).

Combining the properties of the circuits explained above may lead to a HW element with useful configuration options. Which means different levels of fault detection and correction options. The circuit of the Fig. 2 illustrates one of the possible combinations. It mainly adds the necessary control logic, plus an extra clock signal to allow signal inversion and fast re-execution under the self-dual logic using the double inverted clock scheme. Finally, it has a MC element to filter short SET in the logic signals and a comparator to generate a signal in case of fault detection and to keep the rest of the system aware of any fault event. Concerning fault detection and correction, a set of operation modes could be defined as follows:

1) Fault detection plus simple fault correction: fault detection can be performed by inversion, re-execution under the self-dual circuit and then comparison. Simple fault correction of short enough glitches in signals (e.g. SETs) are performed by the Muller-C element.

2) Single event upset correction: correction of SEUs can be done by double re-execution under the self-dual circuit. This mode would demand an extra cost in time and power, since a clock stall would be necessary for the extra re-execution. However, it can be programmed to be used only in very especial situations, for instance, of high criticality requirements.

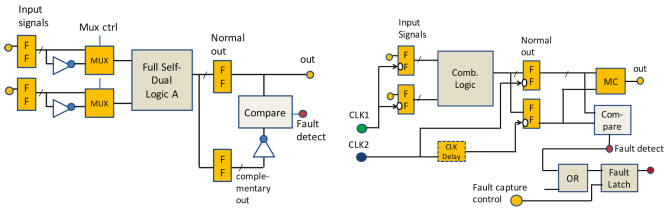

Fig. 1: (a) Self-dual circuit with fault detection capabilities, (b) Circuit using Muller-C element for SETs correction.

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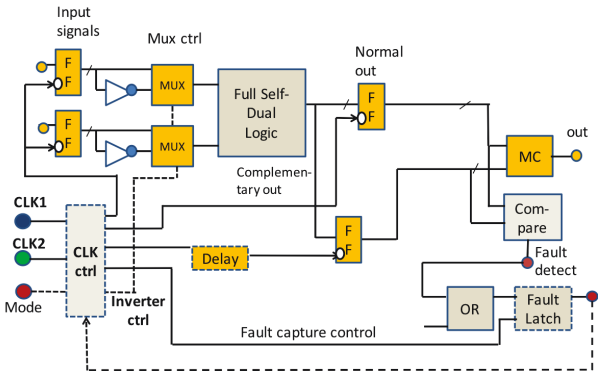

Fig. 2: Combined circuit for fault detection and correction capabilities plus operation mode control.

III. System Level Integration

As mentioned in the section II, the circuit may be configured to work in different operation modes. From the lighter one with simple fault detection to a more robust one with complex fault correction but a bigger penalty in execution time and power.

This configuration capability can be highly explored by a high-level control element running on top of an Operating System (OS) for instance. Since it is running on top level, an OS has knowledge concerning critical levels of the multiple tasks and threads which are running over itself.

Within this scenario, the fault tolerant circuit can be configured to use the lighter operation mode (II-1 - fault detection and simple fault correction) for ordinary tasks, and, in the other hand, the most expensive one (II-2 - fault correction by double re-execution) only when executing critical tasks for example.

A. Fine-grained Integration possibilities

A mechanism has been proposed in the literature for control of Functional Units (FU) inside processor designs [6]. Due to its low-latency, it becomes suitable for many situations when run-time configuration is necessary.

The Functional Units of this control mechanism can be, for example, replaced by the circuit described in the section II of this paper. In fact, it would be an extension of the existing FU, the main requirement would be, however, to extend the control logic of the units to make it self-dual. Which in most cases can be achieved with not so much instrumentation overhead [5].

The control element could be then controlled by adding just a few control signals and registers, since the whole environment for this top to down configuration is already provided by the reconfiguration mechanism.

B. Self-adaptive Multi-core System Integration

A non-standalone SRAM-based SEU monitor for the dependable mixed-critical multicore system is presented in [7]. This monitor can inquire the radiation intensity in the operating environment with negligible cost. By adopting the proposed circuit in section II into the introduced dependable multicore system, a self-adaptive mode selection can be achieved based on the upset rate of the monitor in real-time. Therefore, the single event upset correction mode can be automatically enabled during large radiation particle events; otherwise, the lighter operation mode will be selected. Thus, a dynamic trade-off between reliability, performance and power consumption during run-time can be achieved.

IV. Results

Preliminary calculations of the added control logic in the Fig. 2 show a number of 162 extra transistors per bit plus an additional overhead of 90 transistor for clock and delay control. Consider that a 1-bit Arithmetical Logical Unit (ALU) extended with self-dual properties has around 264 transistors. Thus, the control logic overhead added by the circuit is calculated to be around of 95%.

Concerning power consumption, there are at least two major concerns for this circuit: the extra power incurred by the additional clock signal, and the double re-execution in the SEU correction mode.

Finally, for the system integration of the mentioned circuit, only a few signals and registers would be necessary to perform that.

V. Conclusion

Many authors have introduced the necessity to introduce circuits and systems that have features of fault detection and correction. This paper has shown that circuits from different strategies can be combined to create new configurable ones. Such circuits can be programmed to operate in different operation modes either to detect and correct simple faults with low penalty, or to correct more complex faults but with high extra cost. Results show that such a circuit would bring an extra cost of around 95% of transistors overhead compared to original logic. However, these configurable circuits become suitable for integration in full systems, where operations modes can be defined and top to down configuration be performed according to application requirements. At the same time, self-awareness is improved, since the circuit provides awareness of events and allow high level configuration of itself.

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