Radiation Hard X-Band Phase Locked Loop and Transceiver in 0.25µm SiGe Technology

N. Uddin[a], S. Glisic[a], U. Yodprasit[a], W. Debski[a], W. Winkler[a], C. B. Sánchez[b], J. Á. D. Sánchez[c], M. Kristic[d]

[a]Silicon Radar GmbH, 15236 Frankfurt (Oder), Germany
[b]Arquimea Deutschland GmbH, 15236 Frankfurt (Oder), Germany
[c]Arquimea Ingeniería, 28918 Leganés, Spain
[d]IHP, 15236 Frankfurt (Oder), Germany

uddin@siliconradar.com

Abstract

This paper presents the experimental results of radiation hard phase-locked loop (PLL) and transceiver (TRX) chips in X-band frequency. The chips are designed and fabricated in IHP's radiation hard SiGe BiCMOS SGB25V technology having peak cutoff frequency (f_T) of 80 GHz. Total Ionizing Dose (TID) and Single Event Effect (SEE) tests have been performed for the chips. The circuit level performance degradation associated with these tests is found to be negligible.

I. Introduction

X-band frequencies (8 - 12 GHz) are used for space and satellite communication both in civil and military applications. Traditionally, discrete microwave integrated circuits implemented in III−V technologies have been combined and used for these applications due to their performance advantages over Si technologies [1]-[3]. Unfortunately, such transceiver modules are typically power hungry, large, heavy and hence costly [4], [5]. SiGe HBT technology, being inherently tolerant to TID, good integration capabilities, medium cost and superior performance over Si technology has big advantage for space and satellite communication application. Other potential application areas are space sector, miniaturized radars mounted on drones, autonomous industrial vehicles or in toys, used for navigation and obstacles avoidance, which would benefit from more compact size, lower energy consumption and ultimately much lower cost at higher production volumes. As mostly demanded, a phased locked loop (PLL) chip and a transceiver (TRX) chip are designed and implemented in SiGe BiCMOS technology. The ICs are tested under normal operation condition as well as under irradiation. The chip details are presented in the following sections.

II. X-Band Circuit Design

The SiGe BiCMOS technology used for the design is the IHP SiGe SGB25V technology with 80GHz peak cut-off frequency (f_T) and 95GHz peak maximum oscillation frequency (f_{max}). This work is a part of a Eurostars funded project of development of a radiation hard mixed-signal library for commercialization of space qualified ICs, "LIBRA". As part of analogue library, a low noise amplifier (LNA), a voltage controlled oscillator (VCO), a phase locked loop (PLL), receiver (RX) and a transceiver (TRX) cell, all in the X-band have been developed. This paper reports the design and measurement results of PLL and TRX circuits. The SiGe HBT is used in the circuit without any intentional hardening considering its robustness. NMOS layout is drawn with special layout technique to ensure radiation tolerance.

A. Phase Locked Loop (PLL)

Figure 1 shows the block diagram of the designed PLL. It consists of VCO, frequency divider, phase frequency detector and charge pump. The VCO is of differential cross-coupled type using bipolar transistors. The divider has a divide ratio of 128. The PLL circuit utilizes dual loop topology with coarse and fine tuning inputs at oscillator. The divider also utilizes bipolar transistor. The phase frequency detector (PFD) and charge pumps are designed with CMOS transistors. For radiation hardness, the layout of nmos gate is drawn with closed gate inside active region. Chip area is 1.22 mm x 0.81 mm. Figure 2 shows the realized PLL chip photo with pad names.

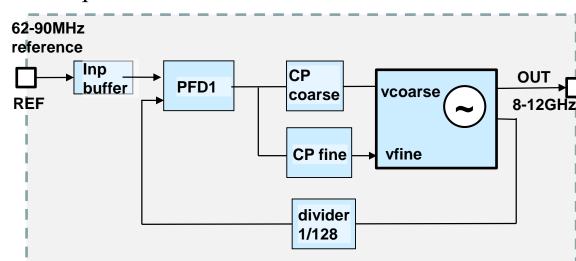

Figure 1: Simplified PLL block diagram

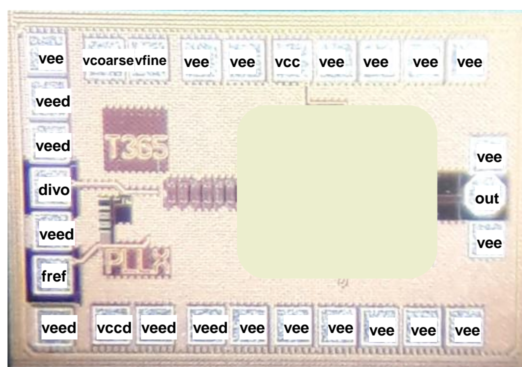

Figure 2: PLL chip photo

B. Transceiver (TRX)

Figure 3 shows the transceiver block diagram. It contains voltage controlled oscillator (VCO), power splitter, power amplifier (PA), poly-phase filter (PPF), low-noise amplifier (LAN), quadrature mixer. Built-in selftest (BIST) structure is included to test the circuit functionality without antenna and high frequency equipment. Chip area is 1.84 mm x 1.1 mm. Figure 4**Fehler! Verweisquelle konnte nicht gefunden werden.** shows the realized TRX chip photo with pad names.

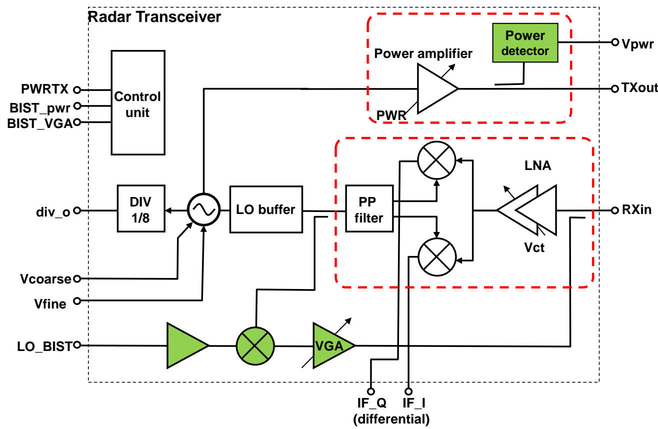

Figure 3: Simplified Transceiver block diagram

Figure 4: Transceiver chip photo

III. Electrical Test

A. Phase Locked Loop (PLL)

The realized PLL chip is wire-bonded on PCB and other components are soldered. Figure 5 shows the PLL test board. Measurement is performed with Rohde & Schwarz signal source analyser.The chip is tested as a free running VCO by changing the tuning voltage and observing the output frequency and power. The supply voltage was also changed by ± 100 mV from the nominal supply of 2.5 V. Figure 6 and Figure 7 show the measured output frequency and power of the VCO. Output frequency varies approximately from 8 GHz to 12 GHz for a tuning voltage of 0 - 3.3 V. The output power is relatively low at the lower frequency ranges (8-9.5GHz) but is stable at the upper frequency range. The divider output frequency and power are also measured and shown in Figure 8 and Figure 9. The divider output frequency varies approximately from 62.5 MHz to 90 MHz (divide ratio of 128). Divider output power is almost constant (-9.5 dBm) for the full frequency range.

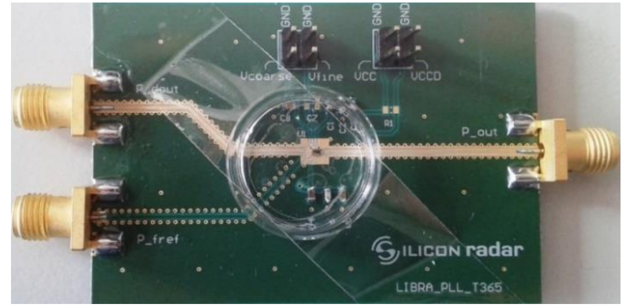

Figure 5: PLL (VCO) test board with chip mounted

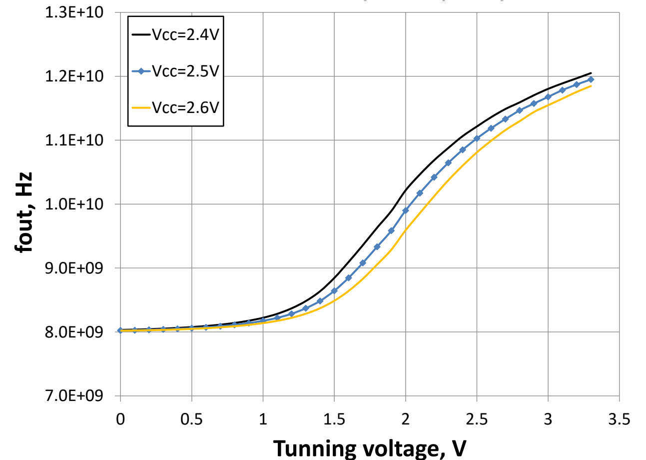

Figure 6: PLL (VCO) output frequency vs tuning voltage

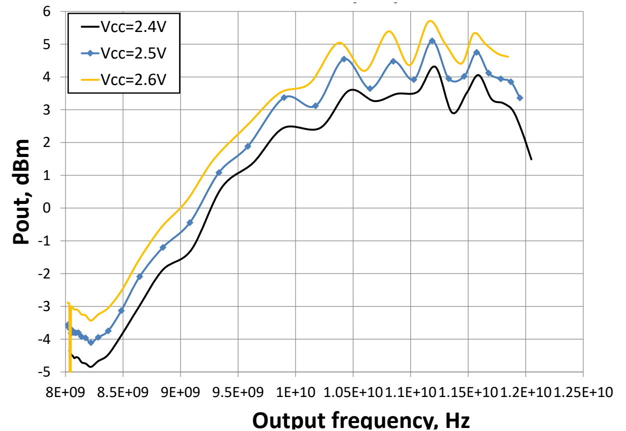

Figure 7: PLL (VCO) output power vs frequency…

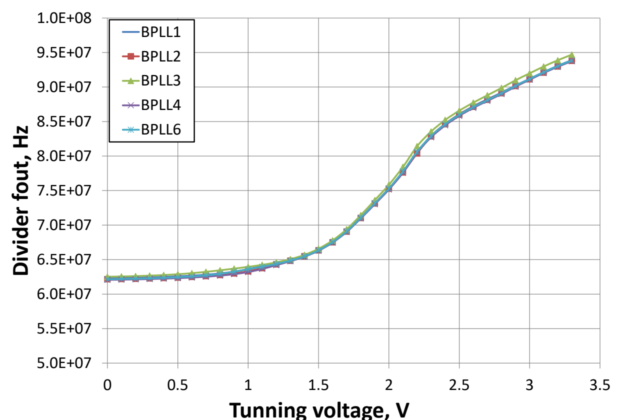

Figure 8: PLL (VCO) divider output frequency vs tuning voltage

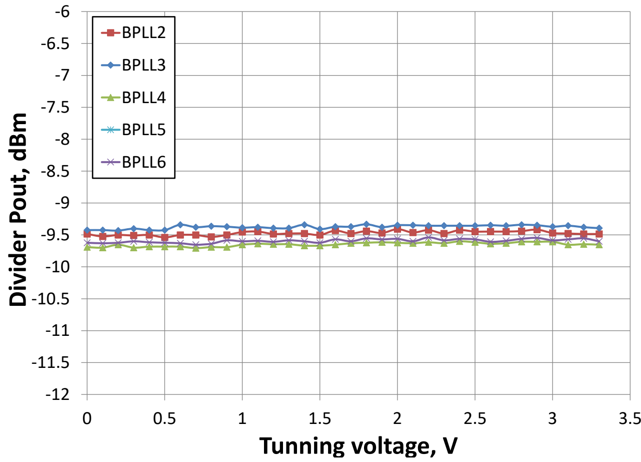

Figure 9: PLL (VCO) divider output power vs tuning voltage

The PLL functionality of the chip is not fully satisfactory. It uses on-chip loop filter and reference input block capacitor. These were not properly scaled. The locking of the PLL is measured from 8.2 GHz to 10.5 GHz for reference frequency of 256 MHz to 330 MHz which is 4th harmonics of divider output. The modification for improvement is implemented in a later design step and now under fabrication.

Table 1: PLL measurement results

	Output frequency (GHz) for PLL Boards				
Ref. Freq. (MHz)	B1	B2	B5	B6	Div. ratio
256	8.19	8.19	8.19	8.19	31.99
300	9.59	9.59	9.59	9.59	31.97
330	10.56	10.56	10.56	10.56	31.97

Measured phase noise at 9.875 GHz and 10 MHz offset is - 105 dBc.

B. *Transceiver (TRX)*

Like the PLL chip, the realized TRX chip is also wire-bonded on PCB and other components are soldered. Figure 10 shows the TRX test board with chip on board. Measurement is performed with Rohde & Schwarz signal source analyser, signal generator, oscilloscope. Firstly, the chip is tested as VCO by changing the tuning voltage and observing the output frequency and power. The supply voltage was also changed by ± 300 mV from nominal supply of 3.3 V. Figure 11 and Figure 12 show the measured output frequency and power of the TRX VCO. Output frequency varies approximately from 10.6 GHz to 12.6 GHz for a tuning voltage of 0 - 3.6 V. The TX output power is 9 dBm and stable with some exception for measurement error. The divider output frequency and power are also measured.

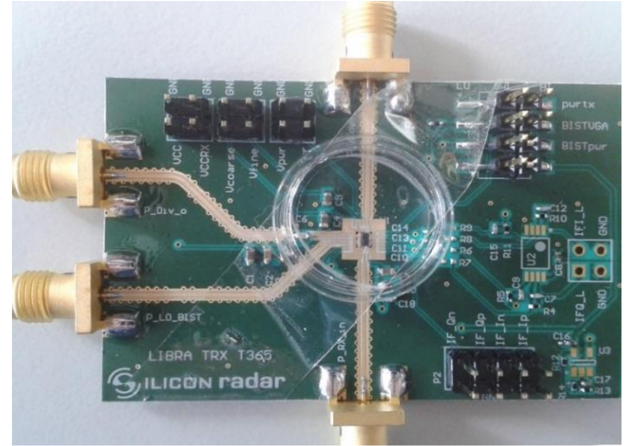
Figure 10: TRX test board with chip mounted

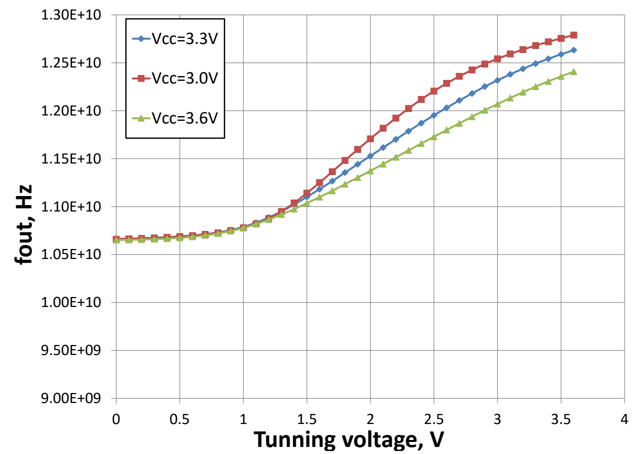

Figure 11: TX (VCO) output frequency vs tuning voltage

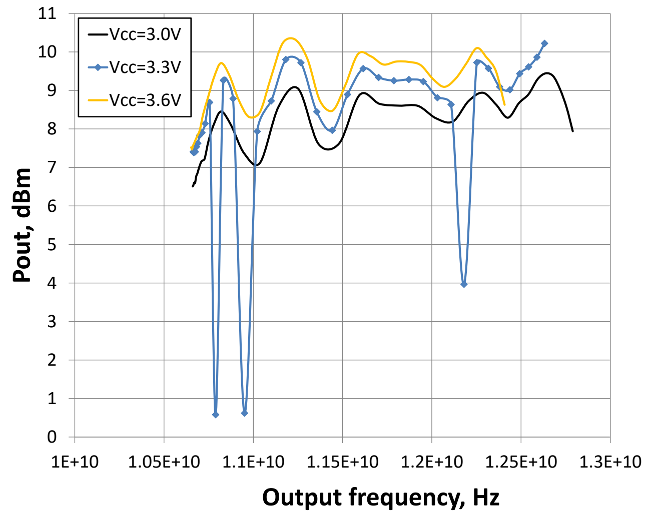

Figure 12: TX (VCO) output power vs frequency

The receiver (RX) is characterized by feeding RF signal at RX input having an offset to LO (TX) frequency. The IF outputs are measured with an oscilloscope. Figure 13 shows a sample of measured IF signal with a RX frequency of 10.713 GHz, RX input power of - 20 dBm and IF frequency of 10 MHz. The receiver (IF) gain is calculated over the RX input power. Figure 14 and Figure 15 show the measured gain for different frequency and different input power respectively.

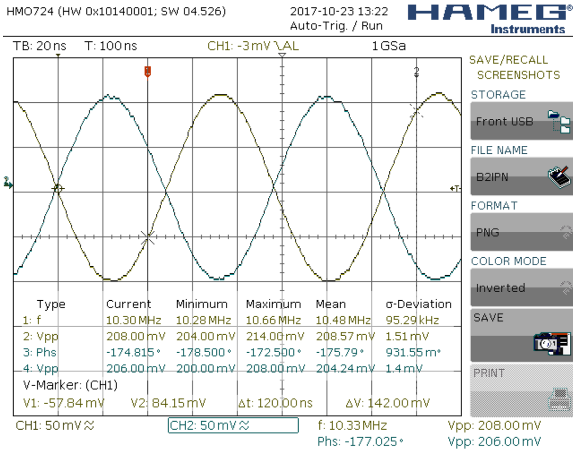

Figure 13: Measured IFIp and IFIn

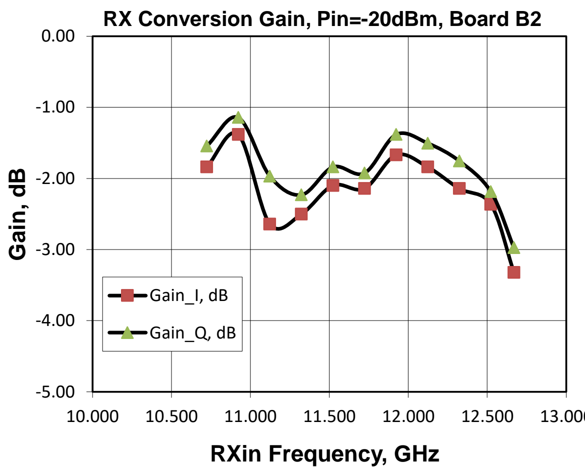

Figure 14: RX gain (single ended) vs frequency

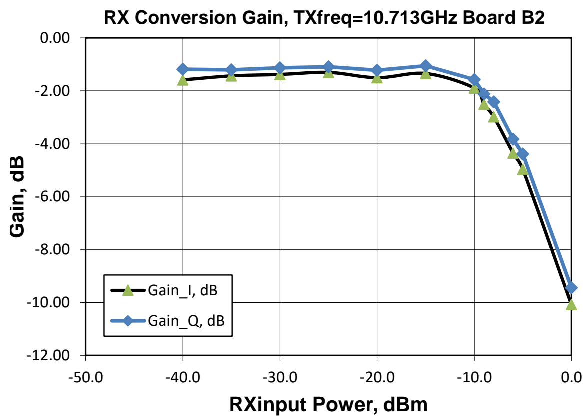

Figure 15: RX gain (single ended) vs RX input power

IV. Test Under Irradiation

After electrical characterization under normal operation condition, the chips are tested under radiation. TID test under gamma ray and SEE test under heavy ion irradiation have been performed.

A. Total Ionizing Dose (TID) Test

The realized chips are tested under TID by the Cobalt-60 gamma radiation source at Helmholtz-Zentrum Berlin, Germany. Tests were performed according to TID test method specification ESCC22900 from European Space Agency (ESA). Five of each type of chips are irradiated and measured at certain interval along with a reference chip which did not go under radiation. Five of each type of boards (total 10) are mounted on a mother board which facilitates biasing all or individual at a time and makes the measurement easy. The mother board is set vertically with respect to radiation as shown in Figure 16. DC supply cables (10 m long) are brought outside the radiation room where dc sources are placed.

Figure 16: TID radiation set up of PLL and TRX boards at HZB

Electrical measurements have been performed after accumulated dose of 25 krad, 75 krad, 150 krad, 230 krad and 300 krad, taking the boards outside the radiation room. Finally, measurement have been performed after annealing of 24 hours at 25°C and annealing of 168 hours at 100°C at IHP facility. Figure 17 to Figure 20 show the measured dc current and output frequency for both types of chips. Figure 19 shows the IF output voltage for the TRX boards. No noticeable deviation in electrical performance (current, oscillation frequency, receiver gain) have been observed in the test results.

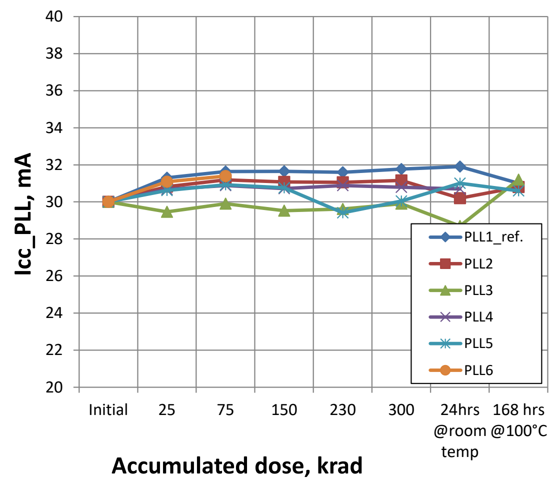

Figure 17: PLL (VCO) dc current at different accumulated dose

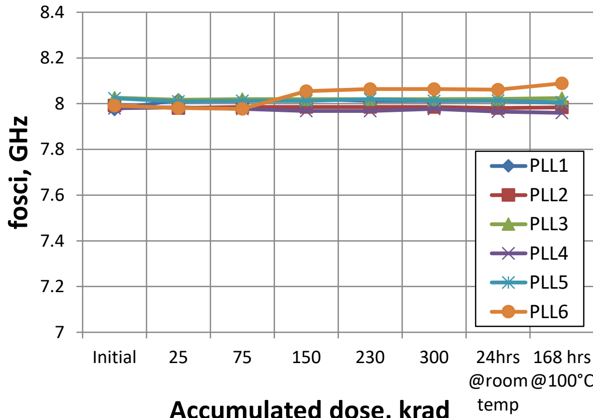

Figure 18: PLL (VCO) output frequency (Vt = 0V) at different accumulated dose

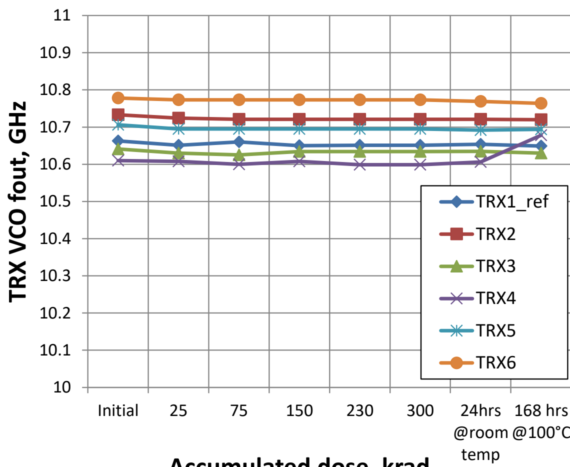

Figure 19: TRX (VCO) output frequency at different accumulated dose

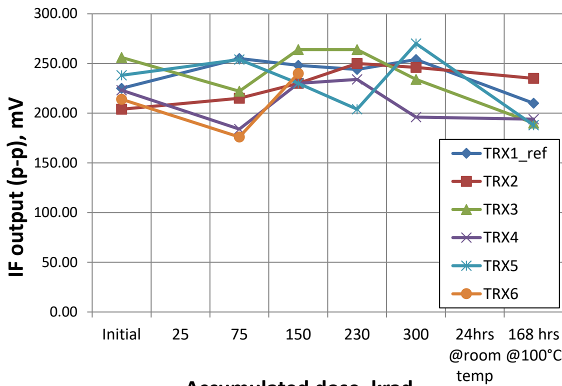

Figure 20: TRX (RX) IF output voltage at different accumulated dose

B. *Single Event Effect (SEE) Test*

The SEE test has been performed at CYCLONE110 facility in the Cyclone Resource Centre Louvain-la-Neuve, Belgium. For SEE test, a special PCB (daughter board) has been designed with the ability to connect with another FPGA driven motherboard for operation control and single event latch-up (SEL) detection developed by Arquimea. The daughter PCB accommodates both PLL and TRX chips but each of the chips can be powered and controlled separately. The daughter board along with the mother board is fixed inside the chamber, as shown in Figure 21. The chips can be heated up using heating element from back side and the temperature can be monitored using a Peltier module. The motherboard is connected to a laptop using communication box for controlling the test.

SEL monitoring: Each supply current on the boards is monitored and can be switched off (latch up protection), when reaching a predefined limit depending on the typical operating mode current. The SEL test is performed at higher temperature (100 - 110°C). Each latch up event is recorded in FPGA for later evaluation.

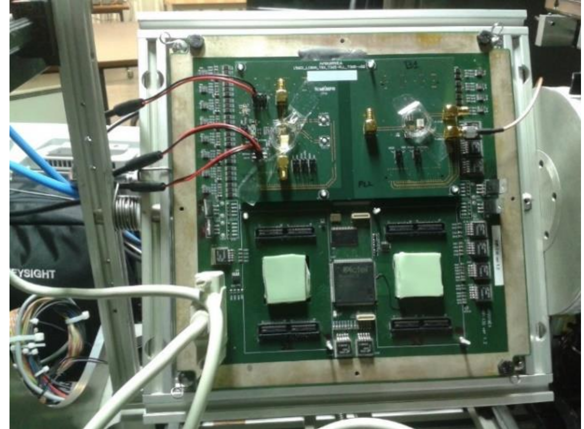

Figure 21: SEE measurement setup (inside chamber)

Figure 22: SEE measurement environment

Single event transient (SET) monitoring: SET data are collected with a digital oscilloscope connected to the DUT. The trigger levels are set so that the signal is always bracketed by the two levels, and the oscilloscope triggers only when a glitch drives the output outside the predefined level and a screenshot is saved. SET test is performed at minimum operating condition and at 25ºC temperature.

The SEE test has been performed on the effects of Xe ion irradiation with LET of 63 MeV·cm^2/mg. The experimental results indicate that the PLL (VCO) and TRX chips have not exhibited single event latch-up (SEL) and single event function transient (SET) sensitivity.

Two Upset (Transient) events are detected: one of DUT1_PLL and one for DUT2_PLL under the mentioned radiation and operation condition.

The number of single event transients detected in the test is also very low and those are at the very beginning of test start (within 1.50 minutes).

The PLL operation could not be tested due to limitation of providing reference input frequency and it is rather tested as VCO. This problem can be focused in future. Additionally, implementing a triggering related to frequency shift can be implemented to observe frequency variation.

V. Conclusion

X-band PLL and TRX are designed and fabricated in SiGe technology and tested under irradiation. Measurements show minimal degradation of performance of the chips, verifying the chips' robustness against radiation and hence are suitable for space applications.

VI. Acknowledgement

The chips are designed under the analogue cell development project which is a part of development of a rad-hard mixed-signal library for commercialization of space qualified ICs, "LIBRA" funded by Eurostars and ended in April 2018.

VII. References

[1] C. Drevon, 2000, June, "From micropackages to MCMs up to 40 GHz for space applications," IEE Sem. Packaging and Interconnects at Microwave and mm-Wave Frequency, pp. 8/1–8/4. Available: https://ieeexplore.ieee.org/document/869826/

[2] A. K. Oki, D. C. Streit, R. Lai, A. Gutierrez-Aitken, Y. C. Chen, R. Grundbacher, P. C. Grossman, T. Block, P. Chin, M. Barsky, D. Sawdai, M. Wojtowicz, E. Kaneshiro, and H. C. Yen, 2000, May "InP HBT and HEMT technology and applications," Proc. Int. Conf. Indium Phosphide and Related Materials, pp. 7–8. Available: https://ieeexplore.ieee.org/document/850216/

[3] D. Streit, R. Lai, A. Oki, and A. Gutierrez-Aitken, 2002, November, "InP HEMT and HBT technology and applications," IEEE Int. Electron Devices for Microwave and Optoelectronic Applications Symp. Dig., pp. 14–17. Available: https://ieeexplore.ieee.org/document/1174923/

[4] D. Yamauchi, R. Quon, Y.-H. Chung, M. Nishimoto, C. Romo, J. Swift,R. Grundbacher, D. Lee, and L. Liu, 2003, June, "A compact transceiver for wide bandwidth and high power K-, Ka-, and V-band applications," IEEE Microwave Symp. Dig., pp. 2015–2018. Available: https://ieeexplore.ieee.org/document/1210555/

[5] M. Karkkainen, M. Varonen, J. Riska, P. Kangaslahti, and V. Porra, 2002, June, "A set of integrated circuits for 60 GHz radio front-end," IEEE Microwave Symp. Dig., pp. 1273–1276. Available: https://ieeexplore.ieee.org/abstract/document/1011895/