Coherent ePIC Receiver for 64 GBaud QPSK in 0.25 μm Photonic BiCMOS Technology

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***Abstract*—In this paper, we present a monolithically integrated coherent receiver with on-chip grating couplers, 90° hybrid, photodiodes and transimpedance amplifiers. A transimpedance gain of 7.7 kΩ was achieved by the amplifiers. An opto-electrical 3 dB bandwidth of 34 GHz for in-phase and quadrature channel was measured. A real-time data transmission of 64 GBd-QPSK (128 Gb/s) for a single polarization was performed.**

***Index Terms*—Silicon photonics, electronic photonic integrated circuit, single chip coherent receiver, optical communications.**

I. Introduction

COHERENT systems are being discussed both for inter-datacenter and intra-datacenter fiber-optic links, e.g., [1]. Such links could use symbol rates from 56 to 64 GBd and polarization multiplexing to support the data rates of 256 Gb/s (QPSK) and 400 Gb/s (16 QAM) and provide high spectral efficiency.

Silicon photonics is preferred over competing technologies for the possibility of high level of integration and scalable low-cost production. Some silicon photonics technologies provide only "passive" photonic integrated circuits (PIC), which contain no electronic components besides photodiodes. Other technologies feature monolithic co-integration of high-speed electronics and photonics in a single electronic-photonic integrated circuit (ePIC). ePIC technologies which contain both high-performance optical devices and high-speed analog frontend electronics are attractive due to high level of integration, allowing for lower power, noise and chip size, and can further be directly combined with DSPs with on-chip high-speed data converters. This approach also allows to reduce testing and packaging costs due to smaller amount of chips used in the final assembly.

As of now coherent ePIC receivers integrating 90° hybrid, photodetectors, and transimpedance amplifiers (TIAs) on the same silicon die have only been published up to Baud rates of 28 GBd [2]. In this paper we present the first monolithic, single polarization coherent ePIC receiver operating at 64 GBd which represents more than a two-times improvement in Baud rate compared to the previous state of the art.

This article is structured in the following way: Section II gives insight into the optical and electronic design details and parameters of the chip, Section III shows the measurement setup and presents the measurement results, and finally a conclusion is provided in Section VI.

II. Chip Details

A. Chip Design

The presented coherent receiver chip was fabricated in a 0.25 μm ePIC SiGe BiCMOS technology [3], that features on-chip integration of optical and electrical components and provides 5 metal layers for interconnects. This technology combines high-performance lateral Ge photodetectors (responsivity of 0.7 A/W and bandwidth of up to 67 GHz at -2 V reverse bias voltage [4]) and heterojunction SiGe bipolar transistors (transit frequency $f_T = 190$ GHz and DC current gain $\beta = 270$). The microphotograph of the fabricated chip is shown in Fig. 1(a). The photonic and electronic parts are localized in two different areas. The photonic part performs the coherent quadrature optical signal coupling, demodulation and detection, while the electronic part contains active amplification circuits for both in-phase and quadrature channels. Each channel has its own lane of DC pads that allows to control biasing of the internal stages, set PD biasing and adjust the parameters of the feedback loop. The rest of the DC pads are used to connect power supply and ground.

Fig. 1(b) shows the corresponding block-diagram with only the I-channel being drawn, as the Q-channel has the same structure.

The size of the photonic part is mainly determined by the coupling requirements, as grating couplers (GC) have to be kept away from electronic pads to avoid the fiber array collision with bond wire connections to the leftmost pads. 4 GCs are used to provide the optical coupling into the chip. The two outer

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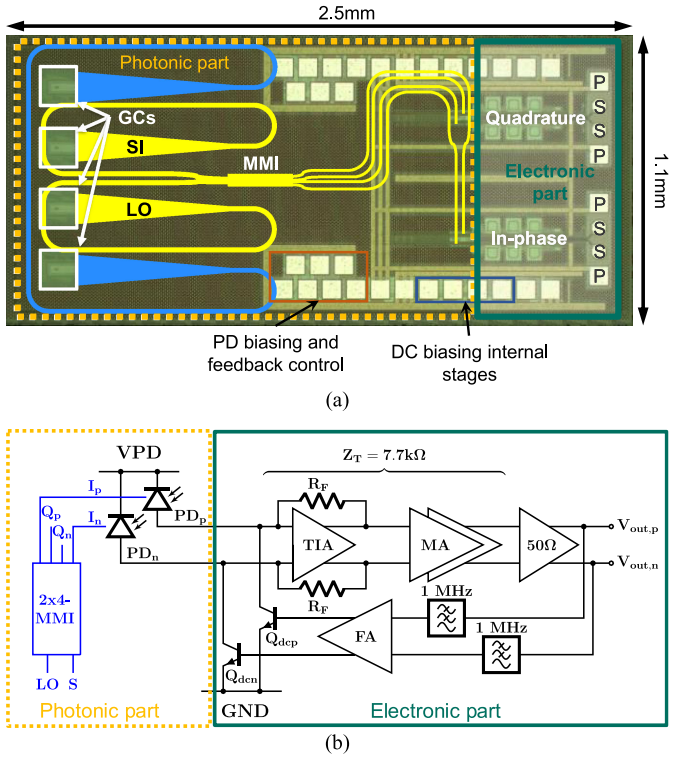


Fig. 1. (a) Photo of the fabricated chip with highlighted main components. (b) Block-diagram of one of the receiver channels with differential photodiode connection and fully-differential input stage.

couplers are connected on the chip and are used during the fiber array alignment procedure to achieve optimal and stable array coupling efficiency. The two inner GCs are routed to the quadrature demodulation structure and are used to couple to the optical signal (SI) and to the local oscillator (LO) inputs. The opto-electronic conversion for in-phase and quadrature channels is made by Ge photodiodes.

While the balanced photodetector architecture [5] is typically used in hybrid and discrete receivers to reduce the number of terminals and provide fully-matched high-performance solution, in a monolithic chip design we propose to use the differential photodiode connection, where each photodiode is directly connected to the respective input of a fully-differential TIA. A major concern in the monolithic integration of quadrature receiver is proper isolation between I- and Q-channels and suppression of external noise, because any interference acquired at the input will be significantly amplified by subsequent stages and can potentially degrade signal quality. A fully-differential input stage architecture has significant advantage over single-ended solutions in this aspect, providing a well-defined operating point, high power supply rejection as well as common mode rejection. Another reason for this choice is the fact that for monolithic integrated devices it is no longer possible to effectively measure and trim individual photodiodes or discard non-perfect devices. Therefore, process variations of diode and transistor parameters make a balanced photodetector approach less reliable and may require some sort of compensation.

The receiver amplification path consists of the fully-differential transimpedance amplifier (TIA) followed by the main amplifier (MA) that operates in limiting mode. It provides a total fixed transimpedance of 7.7 kΩ. This approach was selected because estimated input-referred noise of 15 μA_{RMS} accumulated over the targeted bandwidth would not allow the receiver to operate in linear mode and support any higher order modulation, while limiting mode of operation typically has higher bandwidth and lower noise. The 50 Ω output stage has gain close to 1 and is designed to drive the output load up to 400 mVpp of single-ended voltage swing. Output pad configuration is differential and is referenced to the power supply (PSSP pads), allowing for DC coupling to the measurement equipment when negative power supply scheme is employed. The feedback loop comprising of the low-pass filters, feedback amplifier (FA) and biasing transistors Q_{dcp} and Q_{dcn}, is used to provide a DC photocurrent and amplifiers offset compensation.

The total footprint of the chip is 1.1 mm × 2.5 mm or 2.75 mm^2. It draws 130 mA of current from 3.2 V power supply resulting in in 416 mW of total power dissipation. I- and Q-channels share common power supply and ground terminals.

B. Optical Front-End

In order to match the mode diameter of the light beam from a standard single mode fiber, the width of the GCs was set to 10 μm. The implemented GCs are polarization sensitive demanding external polarization control for proper light coupling. Since the refractive index of silicon and silicon dioxide is much higher than in a fiber, a taper for the transition into a single mode on-chip-waveguide is necessary. The height of the rib waveguide is technology-dependent and is 220 nm in the presented chip. The waveguide width of 700 nm was chosen to minimize the optical losses. The rib waveguide is surrounded with a wide slab of shallow-etched silicon with 150 nm of height. The 90° hybrid, performing the quadrature demodulation, was realized by a planar 2 × 4 multimode interferometric structure (MMI) similar to [6] [see Fig. 2(a)]. In order to conserve the area and to be more flexible with the PD photonic routing, SI and LO lines were bent and routed around their respective GCs. The MMI was optimized using Lumerical MODE Solutions^{TM} via eigenmode expansion algorithm to have minimum phase error and maximum common mode rejection ratio (CMRR), being defined as $CMRR[dBe] = 20\log_{10}[(p_n - p_k)/(p_n + p_k)]$ with p_n and p_k being powers of respective channel outputs, when power is launched from either input of the MMI [7]. A similar structure with additional 150 nm slab on the sides of the MMI was used to improve the phase error. The optimization algorithm resulted in the following dimensions: $L_{MMI} = 10\ \mu$m and $W_{MMI} = 191.2\ \mu$m for length and width respectively. The optimized device exhibits a CMRR of more than 20 dB and a phase error of less than ±6° over an optical bandwidth of 50 nm around the center wavelength 1555 nm [see Fig. 2(b)].

The 4 outputs of the hybrid are routed in a length-matched manner to PDs to avoid additional phase error between corresponding differential inputs of the receiver. The used routing approach allows to avoid any crossings, further improving the channel-to-channel isolation. In the monolithic integration approach, it is possible to place the PDs very close to the active electronic circuits. In the presented chip this distance was as

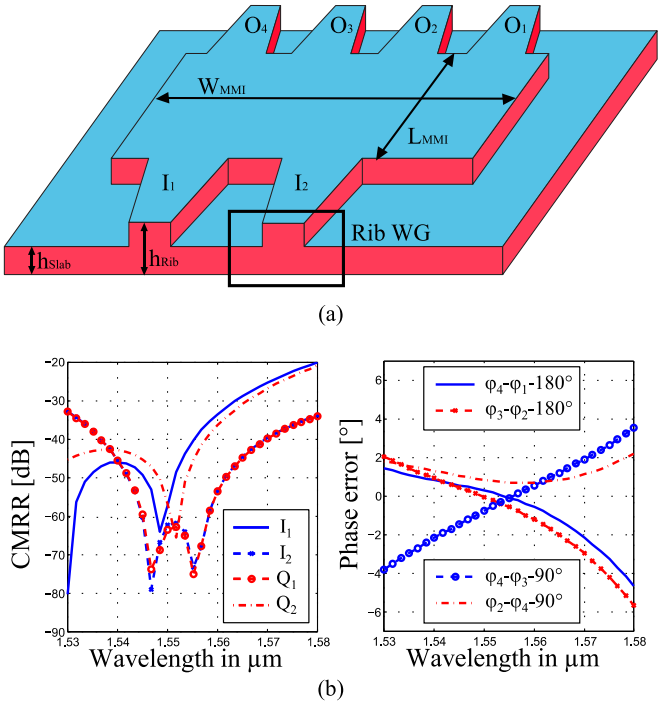


Fig. 2. (a) Si multimode interferometer with rib waveguide inputs and outputs and slab on the sides. Rib and slab height are 220 nm and 150 nm, respectively. (b) Simulation results for CMRR (left) and phase error (right).

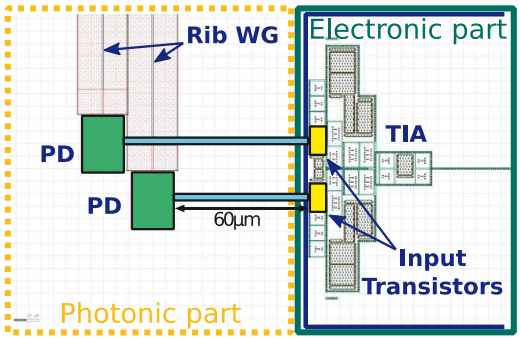


Fig. 3. Layout detail showing 60 μm interconnects between photodiodes and transimpedance amplifiers for I-channel.

low as 60 μm [see Fig. 3]. It could be further reduced down to 25–30 μm according to the design rules of the used ePIC technology, but due to our routing concept and length matching for channel symmetry, a little longer interconnects were adopted. Nevertheless, in contrast to any kind of hybrid solution, the parasitic capacitance and inductances at these sensitive nodes are significantly lower due to absence of pads and bondwires rsp. solder balls that are otherwise necessary for the connection of the PD to the TIA input. Lower input capacitance results in higher transimpedance of the first stage when assuming fixed targeted bandwidth (thus achieving lower noise), or allows to extend the bandwidth to achieve higher data rates [8].

C. Transimpedance Amplifier Stage

In order to achieve both a high transimpedance and a high bandwidth a transimpedance amplifier was used. The shunt

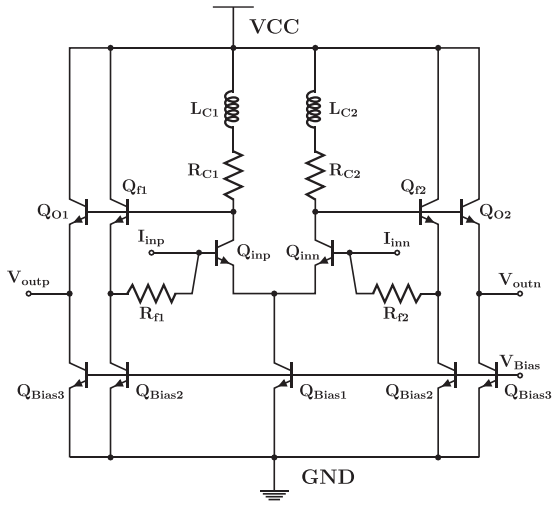


Fig. 4. Shunt-feedback differential amplifier as transimpedance input stage. Feedback realized through emitter-follower stage. Inductive peaking for bandwidth improvement.

feedback TIA architecture [9] typically features reasonable bandwidth performance and low noise operation when compared to other architectures, such as regulated cascode [10].

The schematic of the differential shunt-feedback TIA used in the receiver is shown in Fig. 4. The TIA core comprises a differential amplifier (Q_{inp}, Q_{inn}, R_{C1}, R_{C2}, Q_{Bias1}), two emitter followers (EF) (Q_{f1}, Q_{f2}, Q_{Bias2}), and the feedback resistors R_{f1} and R_{f2}. The size of the input transistors was selected to have multiplier of 3 emitters to reduce the noise generated by the transistor's base resistance. Further increase of these devices did not improve the noise performance, because their parasitic capacitance started to dominate at the input of the receiver, lowering the bandwidth and requiring reduction of R_{f1}, R_{f2}. The bias conditions and operating points of the amplification stages in this architecture are defined by the current fed through $Q_{Bias1..3}$ transistors.

The EF in the feedback path (Q_{f1}, Q_{f2}) improves the bandwidth of the TIA core. However, it forms a second order feedback, adding another pole to the TIA frequency response, which can make it unstable under certain load conditions caused by the next amplifier's input impedance. To avoid this potential instability, the feedback path (Q_{f1} and Q_{f2}) and the output driver path (Q_{O1} and Q_{O2}) are separated into two parallel EF stages [9]. To further improve the bandwidth of the circuit, while keeping acceptable group delay variation and stability, other peaking techniques were also investigated: cascode stage, inductive peaking, negative Miller Capacitance compensation [11], negative capacitance circuit [12]. Cascode amplifier was not used in the TIA stage to keep the input dynamic voltage range high, so that the input amplifier could accommodate a wide range of input signal powers without the necessity to precisely control the feedback loop. Shunt peaking implemented by L_{C1} and L_{C2} inductors with inductance value of 220 pH was found to be best suited for the proposed circuit. The TIA's feedback resistors R_{f1} and R_{f2} were chosen to 320 Ω as well the collector resistor R_{C1} and R_{C2} to 120 Ω to meet the design targets.

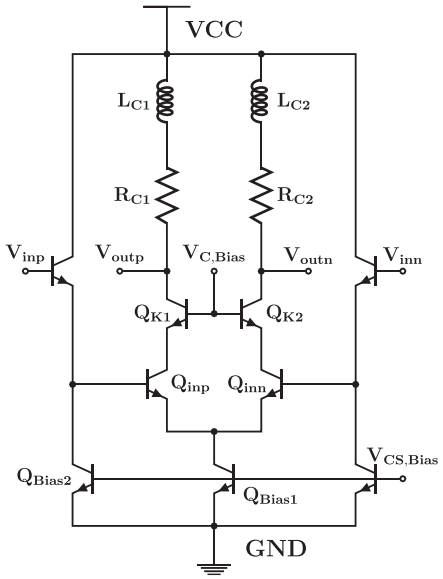


Fig. 5. Cascode amplifier with inductive peaking.

D. Main Amplifier and 50-Ω Output Stage

The MA is implemented with 2 identical differential voltage amplifiers of which one is shown in Fig. 5. The core circuit represents a differential cascode amplifier made from Q_{inp}, Q_{inn}, Q_{K1}, Q_{K2}, R_{C1}, R_{C2}, and Q_{Bias1}. The main advantage of the cascode amplifier is the reduction of the Miller Effect, resulting in higher bandwidth and lower input capacitance. Additional inductors L_{C1} and L_{C2} with inductance value of 220 pH were used to achieve inductive bandwidth peaking in the same way as in the TIA. Input emitter followers between the MA stages improve bandwidth further by reducing capacitive loading between the MA stages. Each stage of the MA has its own external bias control $V_{CS,bias}$ for currents. $V_{CS,bias}$ is generated on chip.

The 50 Ω output stage is also implemented as a differential cascode amplifier with 50 Ω load without any additional bandwidth peaking technique. In the output stage gain is reduced to 1 by means of emitter degeneration in order to achieve sufficient bandwidth.

E. DC Photocurrent and Offset Compensation

As a result of quadrature demodulation there is always a significant portion of DC photocurrent present at the input of the TIAs. This photocurrent can saturate the input transistors and result in the desensitization of the TIA and thus has to be compensated. To handle this issue, a feedback loop is employed that senses the output of the receiver and introduces the reaction at the input of the TIA.

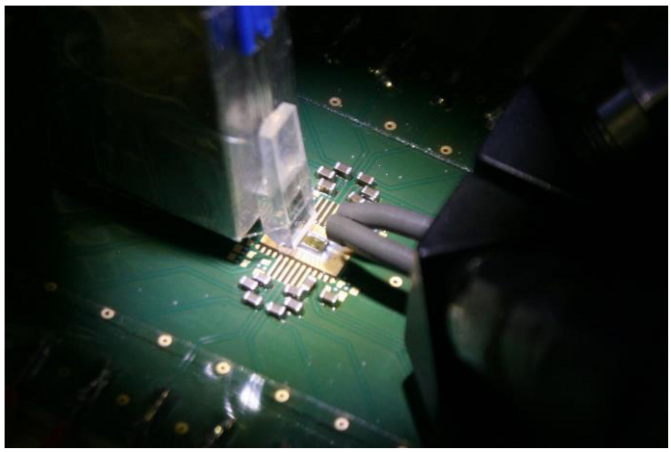
Assuming there is no offset present in the system and it is fully-balanced in its operation, the compensation current is split evenly between both input terminals of the TIA. By default, this current is set to 1 mA and can only be redistributed between two inputs. There is no DC photocurrent sensing present on the chip, so compensation current has to be modified externally via pad when the expected DC photocurrent exceeds the default value. The feedback still can cope with significant input power variation below the compensation threshold due to wide dynamic input range of the input stage. If there is an offset present at any stage of the receiver due to the process variation, temperature gradient or mismatch, the DC voltages of the outputs will drift apart. This situation will be tracked by the FA through the low-pass filters and will be compensated by the redistribution of the current between the inputs of the TIA in the opposite direction.

Because of this feedback, the transfer function of the receiver becomes bandpass with low cut-off frequency defined by the parameters of the low-pass filter and difference between the forward path gain (TIA + MA + 50 Ω) and the gain of the feedback amplifier (FA) [13]. The requirement for proper compensation operation is that the gain of the FA has to be higher than combined gain of the forward amplification path, otherwise low-frequency signals will not be suppressed, resulting in the offset seen at the output of the receiver. The offset of the FA itself should also be low as it will limit maximum precision of the compensation. As a consequence of resulting transfer function, low-frequency noise that could come from flicker noise of electronic components or temperature-related variations of both electronic and optic components will also be suppressed from the output.

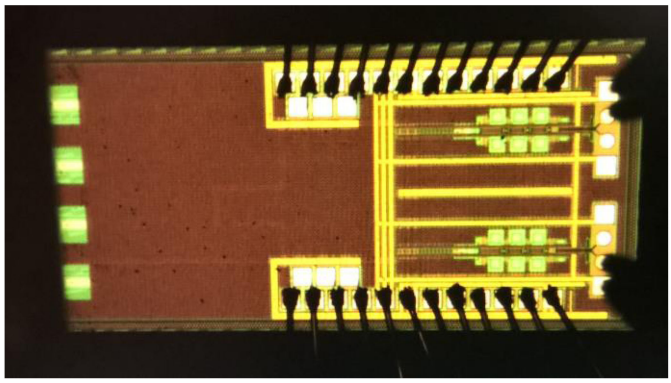
A folded cascode amplifier architecture was used to implement the feedback loop. The resulting low cut-off frequency of the receiver is below 1 MHz. A bypass option was also implemented that allows to break the feedback loop and externally provide the compensation currents to the inputs of TIA, thus fully avoiding the low cut-off frequency, but also losing the flexibility of automatic compensation.

III. Measurement Setup and Results

Measurements were performed on the test chips glued to PCBs with DC pads bonded, allowing to control the biasing currents of the individual amplifier stages with external sources. The optical inputs - the data signal (SI) and the unmodulated carrier (LO) - were fed to the grating couplers (GC) by means of a 4-channel angled fiber array. The fiber array was aligned in position and angle by maximizing the power transmission through the waveguide connecting the outer alignment grating couplers [see Fig. 1(a)]. However, the coupling loss per GCs was measured to be as large as 13.5 dB for e ach coupler. This unexpected high loss can be attributed to the remaining distance between the fiber array and the surface of the chip, as further reduction of this distance during the measurements could result in a collision between the fiber array and bondwires. Nevertheless, the coupled intensity was still sufficient for proper receiver operation due to the high transimpedance of the circuit. Better performance could be achieved by the modification of the fiber array or different bonding approach in a future redesign of the chip. On the opposite side of the chip RF probes were used to measure the electrical output signal [see Fig. 6(a)] Although both in-phase and quadrature channels were designed with differential outputs in a PSSP configuration, the outputs of each channel were probed in a single-ended fashion due to measurement equipment limitation, since both channels have to be



(a)



(b)

Fig. 6. (a) Measurement setup photograph with fiber array (left) and RF probe (right) above the measured chip on the PCB. (b) Chip microphotograph with grating coupler openings in filler structure (left), bondwire connections of DC biases (top and bottom) and two GS and SG single-ended RF probes for simultaneous measurement of in-phase and quadrature channels.

measured simultaneously for signal processing [see Fig. 6(b)]. Multiple chip samples were evaluated showing no significant performance variation.

A. Bandwidth

The opto-electrical bandwidth was measured using two tunable lasers (TLS, Novoptel LU-1000) instead of using a signal modulator [see Fig. 7(a)]. By fine-tuning the TLS wavelength, a precise beating frequency can be generated and controlled in 100 MHz steps. The beating frequency was swept towards high frequency and the outputs evaluated using a 110 GHz electrical spectrum analyzer (ESA, Anritsu MS2760 A). From Fig. 7(b) it can be seen that the 3 dB optical-electrical bandwidth of the receiver is around 34 GHz which is somewhat lower than simulated (42 GHz) which was obtained by the post-layout simulation including electrical interconnect parasitics. In two bandwidth measurement iterations laser center wavelengths were set to 1555 nm and 1565 nm respectively to ensure sufficiently broadband optical frontend performance. The difference between measured and simulated bandwidth was observed for all samples of the receiver. It could be caused by imprecise models of on-chip electrical interconnects or electronic devices. Due to the complexity of the overall circuit the exact cause could not be determined unambiguously.

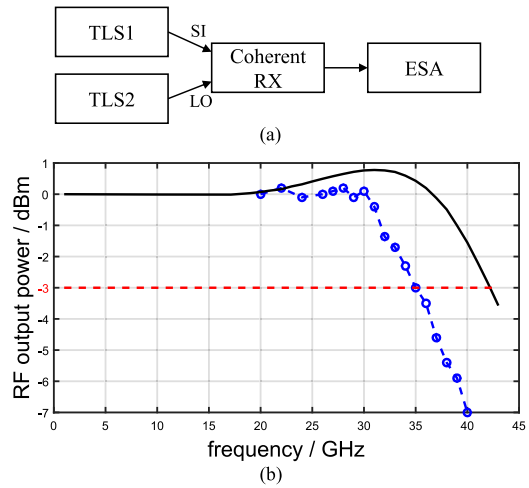


Fig. 7. (a) Bandwidth measurement setup. (b) Comparison of measured and simulated whole chip bandwidth.

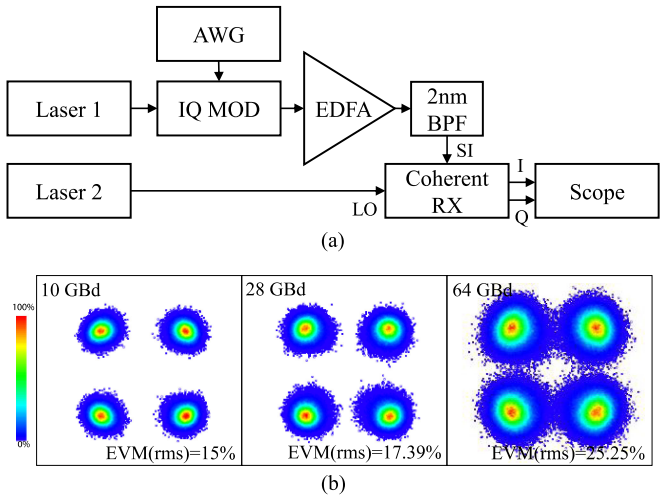


Fig. 8. (a) Transmission experiment setup. (b) Constellation diagram results for differing baud rates: 10 GBd (left), 28 GBd (middle), 64 GBd (right).

B. Constellation Diagrams, EVM, and BER

The data transmission setup is shown Fig. 8(a). A LiNbO3 modulator (EOSpace) was utilized for IQ modulation. The modulator exhibits a nominal bandwidth of around 35 GHz. An arbitrary waveform generator (AWG, Keysight M8196A) generated PRBS 11 signals for the modulator, which were amplified by external drivers (SHF S807). The losses introduced by the modulator were compensated by means of an erbium doped fiber amplifier (EDFA). The EDFA was utilized for flexible adjustment of the optical power during the measurement. However due to high transimpedance of the receiver the actual data transmission experiment could be even performed without

TABLE I
COMPARISON OF COHERENT RECEIVERS IN EITHER SAME TECHNOLOGY OR COMPARABLE HYBRID

Metric	[17]	[12]	[2]	This work
Technology	IMEC SiPh PIC + 0.13 µm SiGe BiCMOS IC	HHI InP PIC + 0.13 µm SiGe BiCMOS IC	EPIC feat. 0.25 µm SiGe BiCMOS	EPIC feat. 0.25 µm SiGe BiCMOS
Baudrate [GBd]	28	64	28	64
Modulation	QPSK, 16-QAM	QPSK	QPSK	QPSK
3dB-OE Bandwidth [GHz]	-	29 -36	-	34
Total Power Consumption [mW]	310	554	514	416
Demonstrated Bitrate [Gb/s]	112	128	56	128
Chip size [mm x mm]	3 x 0.9 (TIA) + 0.3 x 0.5 (PIC)	1.5 x 1.3 (TIA) + not available	3.5 x 2.7	2.5 x 1.1
Power/Bitrate [mW/Gb/s]	5.8 (QPSK), 2.9 (16-QAM)	4.33	9.2	3.25

optical amplification. The optical data signal was filtered with a 2 nm bandpass filter (BPF) removing the out-of-band amplified spontaneous emission (ASE) noise. Polarization controllers were used to effectively couple light into one-dimensional GCs. The electrical outputs of the chip were recorded by means of a 32 GHz real-time oscilloscope (Keysight DSA-X 93204A) and post-processed using vector signal analysis software (Keysight 89600 VSA). The LO power was set to 8.5 dBm and the modulated SI power to 0 dBm by means of the EDFA. Considering the already discussed GC losses this results into -5 dBm LO and -13.5 dBm SI at the 90° hybrid input. Assuming a photodiode responsivity of 0.7 A/W [14] these powers relate to DC currents of 63.5 μA and signal currents of 41.8 μA for each photodiode [15]. A total harmonic distortion (THD) of 6% to 9% for this operating mode was measured by means of a spectrum analyzer. Fig. 8(b) shows the measured and reconstructed constellation diagrams for 10 GBd, 28 GBd and 64 GBd after equalization with time-averaged error vector magnitudes (EVM rms) of 15%, 17.39% and 25.25% respectively. These EVM(rms) values relate to bit error ratios (BER) of $1.31{\cdot}10^{-11}$ for 10 GBd, $4.44{\cdot}10^{-9}$ for 28 GBd, and $3.74{\cdot}10^{-5}$ for 64 GBd according to [16] and are well below the FEC limit of $3.74{\cdot}10^{-3}$ with 7% overhead. To our knowledge this is the fastest single chip coherent ePIC receiver so far, suitable for future low-cost, high bitrate data links.

Table I compares coherent receivers in similar technologies. The receivers from [17] and [12] represent hybrid-integrated PICs with SiGe BiCMOS electronic ICs. In [2] a photonic SiGe BiCMOS ePIC chip is reported which achieves 28 GBd, showing QPSK data transmission. Our coherent receiver outperforms solutions in the same technology and competes well with the best hybrid solutions in comparable technologies considering bandwidth, power consumption and efficiency, demonstrated bitrate, and chip-size.

IV. CONCLUSION

We have demonstrated the first monolithically integrated coherent receiver, fabricated in photonic SiGe BiCMOS technology, performing at bitrates up to 128 Gb/s for a single polarization. To the best of our knowledge this is the fastest monolithically integrated coherent EPIC receiver in any silicon photonic technology, suitable for future high bitrate coherent links.

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