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Si photonic-electronic monolithically integrated optical receiver with a built-in temperature-controlled wavelength filter

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Abstract: We present a Si photonic-electronic integrated ring-resonator based optical receiver that contains a temperature-controlled ring-resonator filter (RRF), a Ge photodetector, and receiver circuits in a single chip. The temperature controller automatically determines the RRF temperature at which the maximum transmission of the desired WDM signal is achieved and maintains this condition against any temperature or input wavelength fluctuation. This Si photonic-electronic integrated circuit is realized with 0.25-μm photonic BiCMOS technology, and its operation is successfully confirmed with measurement.

1. Introduction

As mobile and cloud services become more and more widely deployed, the amount of data processed within data centers is continuously increasing. Consequently, demands for higher-performance interconnect solutions within data centers are getting stronger [1]. Many data centers are replacing electrical interconnects with optical interconnects for rack-to-rack and server-to-server interfaces, and there are many on-going research efforts to further enhance data center performance by applying more extensive optical interconnect and switching solutions [2–4]. In particular, application of WDM technology based on Si photonics is expected to provide higher performance [5,6].

For WDM interconnect and switching solutions, mitigating the temperature-dependent characteristics of wavelength filters is a very important technical issue. Although wavelength filters can be implemented so that their performance is intrinsically temperature independent [7,8], such implementation is not easily achieved in Si photonics technology and the approach based on the filter temperature control is often used [9–11]. Look-up tables can be used for setting the filter temperature at the desired value [12], but this approach can require considerable amounts of indexing time and data storage, and may not provide sufficient temperature control precision especially when the environmental factors vary in a unpredictable manner. Another approach is using the feedback control of the built-in heater with monitoring signals [13–15]. The average filter output power, or the DC output of the transimpedance amplifier (TIA) can be used as the monitoring signal, but this approach requires precise offset calibration for TIA [13,14], which can limit the optical receiver bandwidth. Furthermore, monitoring accuracy is reduced by the signal droop depending on the data pattern. In [15], the amplitude of the received optical data is used as the monitoring signal but a pre-determined reference signal is required. An approach in which the temperature controller can automatically determine the filter temperature providing the maximum received data amplitude is desirable, and dithering filter temperature can be used for achieving

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this [16,17]. In [18,19], such a technique is used for temperature control of ring-resonator filters (RRFs).

However, all of the previously reported filter temperature control techniques rely on control hardware that are located outside the filter and the optical receiver. This can be a problem if many WDM channels are needed since the number of input/output pins needed for temperature control can greatly increase especially when the photonics platform does not provide any electronics with which temperature control signals can be multiplexed.

In this paper, we demonstrate a single-chip Si ring-resonator based optical receiver containing all the temperature-control hardware. The temperature controller in our optical receiver automatically determines the condition at which the RRF output signal has the maximum amplitude in the calibration mode, and maintains this condition against any external temperature variation or input wavelength fluctuation in the lock mode. Although we demonstrate the integrated temperature control technique for the ring-resonator based optical receiver having only one simple RRF in this paper, our approach can be easily extended to WDM receivers having more channels with more sophisticated filters, in which the advantage of the photonic-electronic integration can be even more pronounced.

The remaining part of this paper is organized as follows. In Section 2, detailed explanations are given for the structure and the temperature control method of our optical receiver. In Section 3, the measurement results of performance verification of our optical receiver are presented. Section 4 concludes the paper.

2. Optical receiver with a built-in temperature-controlled ring-resonator filter

Figure 1(a) shows the block diagram of our integrated ring-resonator based optical receiver, and Fig. 1(b) shows the microphotograph of the fabricated chip. The optical receiver contains a RRF having on-chip heater, Ge-photodetector, receiver circuits, and RRF temperature controller, all of which are monolithically integrated on IHP's 0.25-μm Photonic BiCMOS technology [20,21]. The total size for the electronic blocks is 0.337 mm^2 that includes 0.131 mm^2 optical receiver and 0.206 mm^2 temperature controller. In the case of a WDM receiver having multiple channels, it is possible to implement the temperature controller so that one controller can control several channels preventing linear increase of the total size for the electronic blocks with the WDM channel number. Furthermore, using more advanced Si technology than used for the present study, the size for the electronic part can be significantly reduced

The RRF is realized with 450-nm wide Si waveguides fabricated on 220 nm thick SOI. A portion (33%) of the ring waveguide is N-doped for realizing an on-chip heater, which can tune the RRF resonance wavelength to 54% of its FSR. This type of Si heater is used in order to realize the sufficient temperature tuning range, even though it induces a fair amount of loss. However, a metal heater can be used that does not provide as much loss if a dedicated heater fabrication step can be employed [22] and the thermal isolation techniques [23,24] can further improve the efficiency of the heater.

Figure 2(a) shows the measured normalized RRF transmission characteristics for the through port at room temperature, and Fig. 2(b) shows the measured transmission spectrum RRF for drop port at several different voltages applied to the on-chip heater. The temperature values shown in the figure are estimated from the amount of peak wavelength shift using the known temperature dependence of Si refractive index. The measured insertion loss is about 4.5 dB for the drop port excluding the grating coupler without the heater operation. This insertion loss has two components: about 3 dB loss for the ring resonator corresponding to the Q-factor of about 3570 without the N-doped Si heater determined from the simulation, and about 1.5 dB loss due to the free-carrier absorption within the N-doped heater whose propagation loss corresponds to about 120 dB/cm. The propagation loss of N-doped heater reduces the Q-factor to about 2590, determined from the measured transmission spectrum. The 3 dB loss of the ring resonator is

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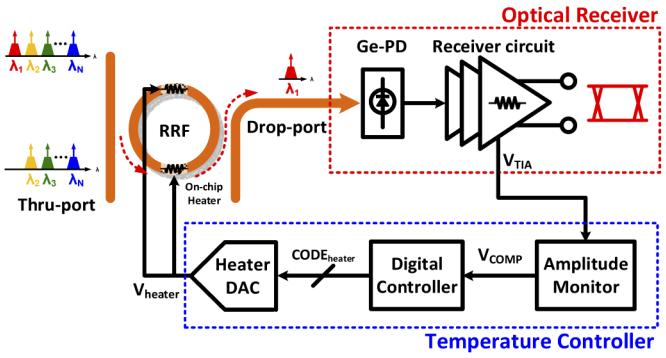
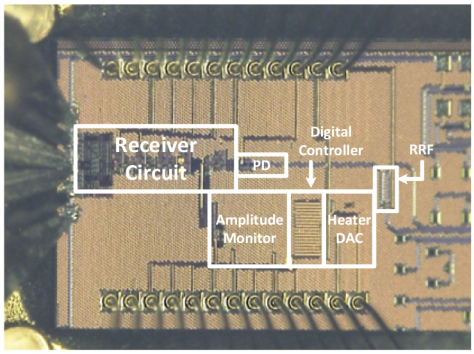


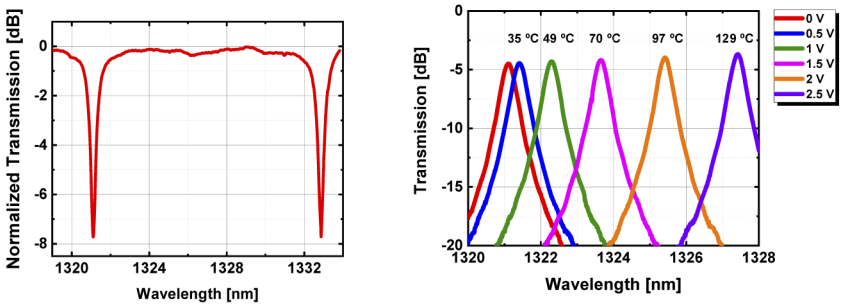
(a)



(b)

Fig. 1. (a) Block diagram and (b) chip microphotograph of monolithically integrated Si ring-resonator based optical receiver with built-in wavelength filter.

mostly due to the bending loss in the ring waveguide as the ring has a relatively small radius of 6 µm. At higher temperature, this bending loss becomes smaller as the ring waveguide has tighter confinement, resulting in smaller insertion loss as can be observed in Fig. 2(b).



(a) (b)

Fig. 2. Measured normalized transmission of RRF for thru-port and (b) measured transmission spectrum of RRF for drop-port and its temperature dependence

Figure 3 shows the structure of the optical receiver and the amplitude monitor within the temperature controller. The optical receiver consists of Ge-PD, TIA, single-to-differential

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buffer, 2-stage post amplifiers, and output buffer. A regulated cascode structure is used for the TIA for achieving the high gain-bandwidth product. The TIA output is delivered to the amplitude monitor, which is composed of peak detector, track and hold circuit, and sense-amplifier-based comparator. The amplitude monitor periodically samples the amplitude of the received optical signal, compares it with the previously sampled value, and produces VCOMP indicating whether the present value is larger than the previously sampled value (VCOMP = 1) or is smaller (VCOMP = 0). This information is delivered to the on-chip digital controller, as shown in Fig. 1(a), realized by automatic CMOS circuit synthesis based on libraries available in Photonic BiCMOS technology. This temperature controller architecture is similar to that used in [25]. However, the entire temperature controller in the present work is monolithically integrated with photonic devices, whereas in [25] the temperature controller and the photonic devices are designed and fabricated separately, and connected with wire-bonding. Our approach based on monolithic electronic-photonic integration can provide a much reduced I/O count, which is of great advantage especially for applications requiring many WDM channels.

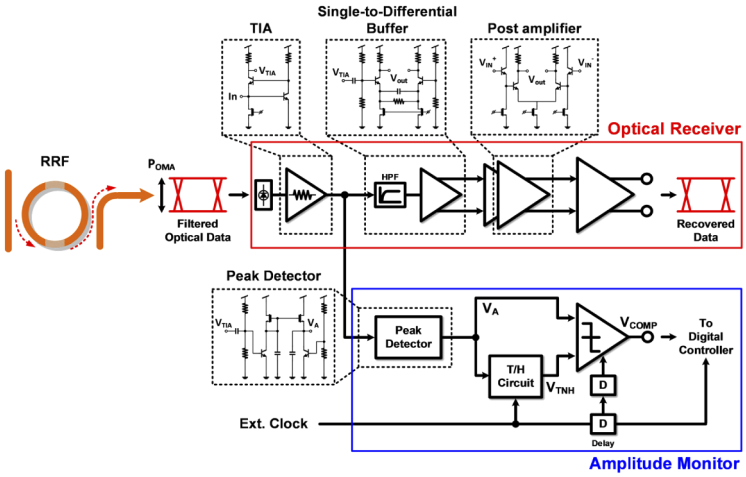

Fig. 3. Detailed structure of the optical receiver circuit and amplitude monitor.

In the calibration mode, the digital controller generates the control bit ($CODE_{heater}$) which produces the heater voltage (V_{heater}) through the heater DAC. The digital controller scans RRF temperature within the pre-determined temperature range, and stores the control bit that produces the largest amplitude, corresponds to the RRF temperature producing the maximum RRF transmission. Figure 4(a) schematically shows the timing diagrams for on-chip heater voltage (V_{heater}), presently-sampled amplitude value (V_A), previously-sampled amplitude value (V_{TNH}), and the result of comparison (V_{COMP}), during the calibration mode. As shown in the figure, V_{heater} goes up in the calibration mode, V_A initially increases since the RRF peak transmission wavelength is smaller than the WDM signal wavelength (Region A), reaches the peak value (Region B), and then decreases (Region C) since the RRF peak wavelength increases with temperature. Since V_{TNH} is the delayed version of V_A, when V_A crosses the peak, V_{TNH} is larger than V_A, at which point V_{COMP} becomes low. From this, the digital controller can determine $CODE_{heater}$ that provides V_{heater} required for the optimal condition, and stores it. The sampling period can be determined by the external clock signal provided to the digital controller, which is designed to be operational up to 5 MHz clock signal. The clock entering each circuit is based on an external clock source. All clocks required by the temperature controller circuit uses an external clock source and a delay based on the inverter chain. A clock without delay is input

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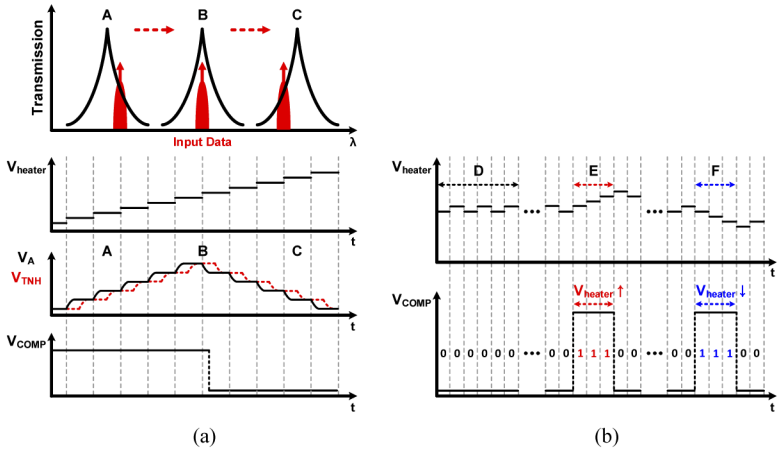
to track and hold, and the clock is input through one delay to the digital controller and two delays to the comparator.



(a) (b)

Fig. 4. (a) Timing diagram during the operation of temperature controller in calibration mode and (b) in lock mode.

Once the calibration step is over, the digital controller goes to the lock mode in which the digital controller maintains the heater voltage required for the maximum received amplitude. Figure 4(b) shows the timing diagrams during the lock mode. The temperature controller dithers $CODE_{heater}$ by one bit from the optimal value, while continuously monitoring V_{COMP}. If no change of V_{heater} is needed, then V_{COMP} remains LOW and the optimal V_{heater} is maintained as it is Region D in the Fig. 4(b). If V_{COMP} becomes HIGH when $CODE_{heater}$ increases by one bit or increase in V_{heater} is needed, then the digital controller increases $CODE_{heater}$ until V_{COMP} becomes LOW and resumes one-bit dithering (Region E). If V_{COMP} becomes HIGH when $CODE_{heater}$ decreases by one bit or decrease in V_{heater} is needed, then the digital controller decreases $CODE_{heater}$ until V_{COMP} becomes LOW and resumes one-bit dithering (Region F).

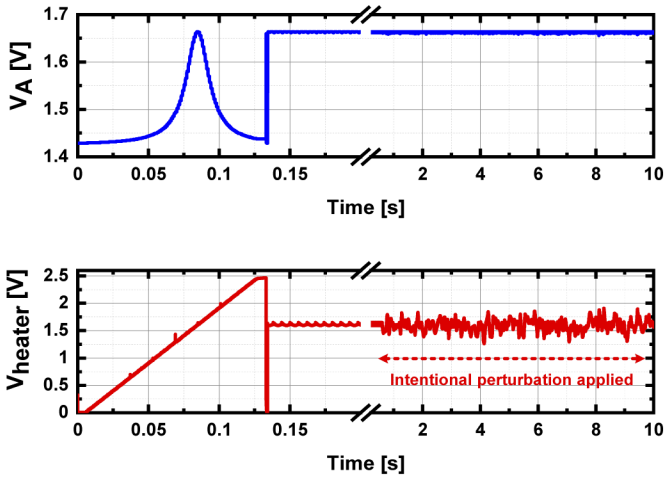


Fig. 5. Simulation result of temperature controller with RRF behavioral model.

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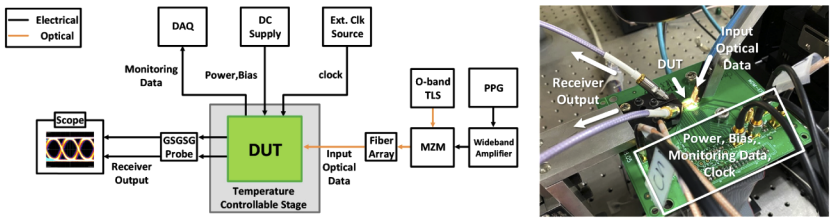
In this way, the temperature controller can maintain the optimal RRF temperature even if the ambient temperature changes or the input wavelength fluctuates.

Figure 5 shows the behavior-level simulation results of the entire temperature controller operation using 1 kHz clock. For this, the temperature-dependent RRF characteristics are modeled with Verilog codes and co-simulated with other circuit elements in Verilog-A, the standard EDA tool which allows co-simulation of Verilog and SPICE. As can be seen in the Fig. 5, the peak amplitude is correctly determined in the calibration mode and maintained in the lock mode. For the demonstration purpose, white noises having peak-to-peak value of 618 mV and RMS value of 80 mV, which corresponds to 30 degrees and 5.3 degrees, respectively, of temperature variation are intentionally introduced to V_{heater}. As shown in the figure, the temperature controller in the lock mode well maintains the optimal V_A value by changing V_{heater} so that the influence of the perturbation can be mitigated.

3. Measurement

Figure 6(a) shows the schematic diagram of the measurement setup, and Fig. 6(b) shows the photograph of the test board. The fabricated chip is mounted on a FR4 PCB, and DC supply/bias voltages for the circuits are provided through bonding wires. The entire board is placed on a temperature-controlled stage. Two grating couplers are used for optical I/O. 2.6 V is used for the circuit supply voltage. The power consumption is 48 mW for the receiver circuit, 11.7 mW for the temperature controller in the lock mode, and up to about 21 mW for the on-chip heater. The power breakdown of RRF temperature controller is shown in Fig. 6(c). For PRBS31 12.5 Gb/s optical data generation, a commercial Mach-Zehnder modulator along with an O-band light source is used. An external 1 kHz clock signal generated by arbitrary function generator is used for the temperature controller operation.



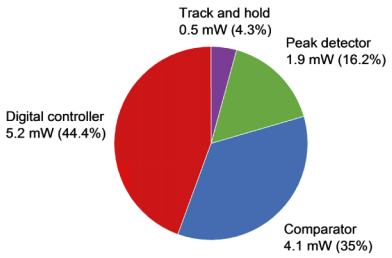


Fig. 6. (a) Block diagram of measurement setup and (b) its photograph. (c) Power breakdown of the RRF temperature controller.

Since the post-amplifier of the receiver circuit is not sufficiently optimized and has a bandwidth of 13 GHz, we are not able to demonstrate higher data rate operation. However, simulation

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results show that the peak detector can work for data up to 40 Gb/s. For controlling the RRF having the higher Q-factor, the only change needed is the heater DAC so that it can have a higher resolution. In order to make the temperature controller operational for controlling RRF with faster temperature variation, the controller has to operate with a faster clock and heater has to operate with smaller thermal time constant. Although 1 kHz clock is used for the present investigation, simulation results show that our temperature controller can operate with up to 5 MHz clock without any stability issues as long as the heater thermal time constant is smaller than the clock period.

Figure 7(a) shows the measured V_A and V_{heater} in both calibration and lock modes, and Fig. 7(b) shows the eye diagrams for the received optical data at four different conditions during the calibration mode marked as A, B, C, or D in Fig. 7(a). As the V_A approaches the peak, the RRF resonance frequency approaches the input data wavelength, providing larger eye opening. Figure 7(a) also shows that the maximum V_A value is well maintained in the lock mode. Figure 7(c) shows the eye diagram in the lock mode. The glitch in V_{heater} at the moment when the lock mode starts is due to the unnecessary step of setting V_{heater} to the minimum value. This does not influence the overall performance of the temperature controller and can be easily fixed by a minor modification in the digital controller.

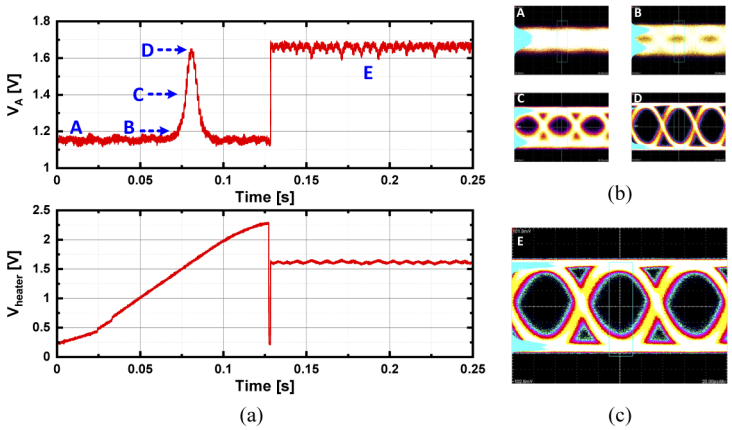

Fig. 7. (a) Measured V_A and V_{heater} in calibration and lock modes. (b) Measured eye diagrams at four different RRF temperatures. (c) Measured eye diagrams during lock mode operation.

Figure 8(a) shows the measured transient response of V_{heater} when the temperature of the stage changes during the lock mode. The stage temperature sinusoidally changes ±10 °C around 30 °C with 0.5 mHz frequency. The temperature change frequency is limited by the stage, not by our temperature controller. Figure 8(b) and (c) show the 12.5 Gb/s eye diagrams for 500 seconds without and with the temperature controller, respectively. Without temperature control, the eyes are all closed, but with our temperature controller, clean eyes can be maintained, clearly verifying the successful operation of our on-chip temperature controller.

Figure 9(a) shows the measurement results when the input data wavelength shifts slightly in the lock-mode operation. The input wavelength is shifted by 1 nm in every 10 seconds. 10 seconds are needed for this measurement as our optical source does not allow rapid frequency shift. Our temperature controller operates successfully up to 6 nm input wavelength shift, which corresponds to temperature change of about 90 degrees for the RRF. Figure 9(b) shows the accumulated eye diagram during this measurement.

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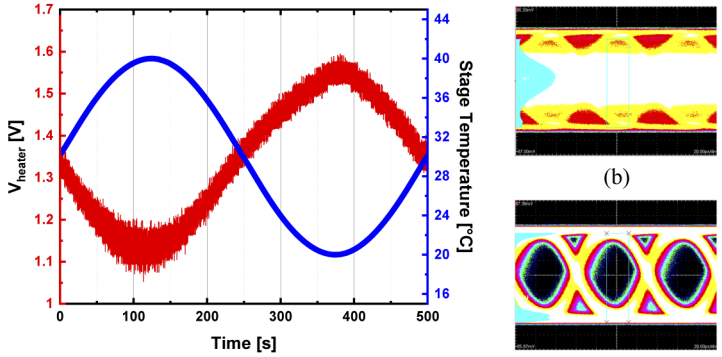

Fig. 8. (a) Measured V_{heater} (red) when stage temperature changes sinusoidally (blue) for 500 seconds. (b) Measured eye diagrams during this without temperature control, (c) with temperature control.

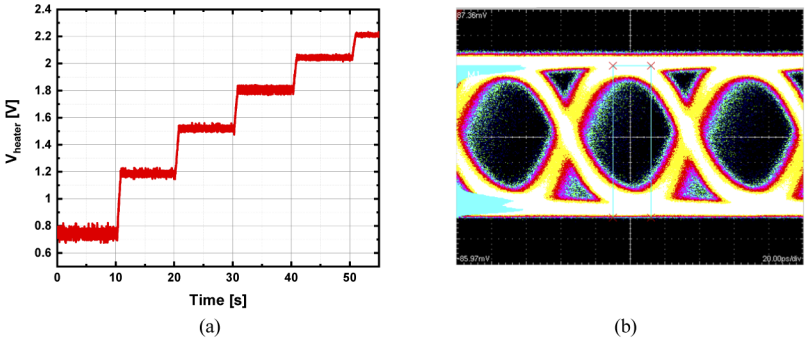

Fig. 9. (a) Measured V_{heater} during the lock mode when input wavelength changes in 1 nm steps and (b) its accumulated eye diagram.

4. Conclusion

A single-chip Si photonic-electronic integrated ring-resonator based optical receiver with a built-in temperature-controlled wavelength filter is realized based on IHP's 0.25-μm Photonic BiCMOS technology. The optical receiver contains all the necessary optical components and electrical circuits, that are needed for filtering out only desired wavelength optical data even if environment temperature or input wavelength changes. The photonic-electronic integration approach demonstrated in this paper demonstrates a great amount of applicability for various Si photonic interconnect and switching applications.

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