Advancing Graphene Integration in Si CMOS Technology: Challenges, Solutions, and Modulator Exploration

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Abstract

The potential of graphene-based devices in enhancing Si CMOS technology functionalities has been widely recognized [1,2]. Nevertheless, the successful integration of graphene into novel microelectronic devices encounters significant challenges. These include: i) The attainment of wafer-scale, high-quality graphene on CMOS-compatible materials (e.g., dielectrics or semiconductors) and subsequent transfer. ii) Developing reliable methods for applying a passivation layer on the graphene surface. iii) Ensuring the entire wafer processing with graphene can adhere to the standard Si CMOS pilot line protocols. This study is dedicated to addressing these challenges comprehensively within a 200mm pilot line at IHP. We have devised several conceptual frameworks aimed at overcoming these obstacles, exemplified by the fabrication of test proof-of-concept devices such as TLMs, Hall bars, or Kelvin bridge structures. The electrical properties of the transferred graphene layers (were determined to be Rs ~1500 $\pm 100 \Omega/sq$ and μ ~800 $\pm 20 \text{ cm}2/V$ •s. The extracted contact resistances at graphene/metal interface were measured at 60 Ω .

Moreover, recent years have seen a surge in interest in graphene-based modulators due to their potential for high-speed and low-power operation, rendering them promising for optical communication and computing systems. These modulators leverage graphene as the active material to modulate light intensity or phase. With their outstanding characteristics encompassing high speed, low power consumption, and compatibility with silicon-based technology, graphene modulators possess the capability to transform optical communication and computing landscapes. Therefore, simulations and fabrication of the graphene ring modulators have been conducted at both the component and device levels, incorporating realistic graphene properties. These results indicate a modulation depth of 1.6 dB/ μ m and a 3dB bandwidth of 7 GHz, showcasing the potential of graphenebased photonic devices for high-speed communication applications. In addition, this study describes the development of silicon nitride photonic integrated circuits (Grating couplers and waveguides) on a 200mm wafer scale as a basis for the graphene-based optical modulators. It's crucial to highlight that the experiments conducted herein occurred within a standard BiCMOS pilot line, rendering this research particularly distinctive. The insights gleaned from this study hold the potential to significantly expedite the integration of graphene and the prototyping of graphene-based devices within mainstream Si technologies.

[1] L. Kim et.al., Science 479 (2011) 338.

[2] W. Mehr et.al., Electr. Dev. Lett., 33, (2012) 691.

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