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Towards a CMOS compatible refractive index sensor: cointegration of TiN nanohole arrays and Ge photodetectors in a 200 mm wafer silicon technology

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Abstract: In this work, we present the monolithic integration of a TiN nanohole array and a Ge photodetector towards a CMOS compatible fabrication of a refractive index sensor in a 200 mm wafer silicon technology. We developed a technology process that enables fabrication with high yields of around 90%. Ge photodetectors with a Ge layer thickness of 450 nm and an area of 1600 µm^2 (40 µm x 40 µm) show dark current densities of around 129 mA/cm^2 and responsivities of 0.114 A/W measured by top illumination (TE polarization; $\lambda = 1310$ nm; angle of incidence = 14 °) at a reverse bias of 1 V. Nanohole arrays were structured in a 150 nm thick TiN layer. They were integrated into the back end of line and placed spatially close to the Ge photodetectors. After the metallization, passivation, and pad opening, the nanohole arrays were released with the help of an amorphous silicon stop layer. A significant impact of the TiN nanohole arrays on the optical behavior of the photodetector could be proven on the wafer level. Photocurrent measurements by top illumination confirm a strong dependence of optical properties on the polarization of the incident light and the nanohole array design. We demonstrate very stable photocurrents on the wafer level with a standard deviation of $\sigma < 6\%$.

1. Introduction

In the last decade, the broadening range of applications of integrated circuits has driven research on the integration of diverse device functionality such as sensors on chip. Optical sensors based on plasmonic excitations utilize the optical properties of either propagating surface plasmon polaritons (SPP) at a metal dielectric interface or localized plasmons in metallic nanostructures for the detection of bulk refractive index changes or near-surface refractive index (RI) changes as induced by ligand-analyte binding events on the sensor surface [1,2]. In this context, metallic nanohole arrays (NHAs) have been investigated. In these structures, extraordinary optical transmission (EOT) can be observed as pronounced transmission peaks at certain wavelengths related to resonant excitations of propagating surface plasmon polaritons at the top and bottom metal dielectric interfaces [3]. The spectral position of those peaks is determined by the geometry parameters of the NHA and can be shifted by changing the refractive index of the dielectric material adjacent to the NHA [4]. This enables the detection of RI changes. Furthermore, the EOT spectra are dependent on the angle of the incident light and its polarization [5]. A combination with a photodetector below the NHA enables a direct conversion of the optical signal to an electrical signal, with possible applications in sensing. Several works have already investigated plasmonic RI sensors comprising metallic NHAs cointegrated with germanium (Ge) photodetectors [6–9]. In those devices, responsivities of R_{opt} (0 V) = 0.08 A/W were obtained for 500 nm thick Ge photodetectors and sensitivities of S = 1200 nm/RIU in bulk RI sensing.

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However, the layer stack of the Ge photodetector was deposited by a molecular beam epitaxy (MBE) step and the NHAs were realized in an aluminum (Al) layer, which was deposited via e-beam evaporation and which was also used as the metallization layer. Thus, their sensor fabrication comprises CMOS incompatible procedures. For the integration in a CMOS compatible 200 mm wafer Si technology, a substantial device and process re-design is required and subject of our research. One particular challenge regarding device realization based on the fact that Ge photodetectors are fabricated in the Front End of Line (FEOL), while the metallization is realized in the Back End of Line (BEOL). The BEOL comprises several metal layers separated by interlayer dielectric (ILD) stacks. Usually, the vertical distance between the FEOL components and the first metal layer of the BEOL is around 1.5 µm. Hence, the realization of an RI sensor in a CMOS compatible 200 mm wafer Si technology is very challenging because it requires the integration of a metallic NHA close to the Ge photodetector without an encapsulation by the ILD stack in order to enable a direct contact with materials to be analyzed.

In this work we present the technological realization of a Ge photodetector combined with a TiN NHA fully integrated in CMOS compatible 200 mm wafer Si technology. The fabrication of Ge photodetectors is mainly based on the IHP ePIC Technology [10] and involves the utilization of a modern design concept [11]. The NHAs were realized in a titanium nitride (TiN) layer. This material was chosen due to its CMOS compatibility and due to its good potential for plasmonic applications [12–16]. In previous works we developed separate process modules only for the fabrication of the TiN NHA [11] and its exposure after finishing the metallization [17]. Here, we combine all developed modules to a full technology process. For our investigations in this work, the metallization comprised only a single metal layer. Hence, the exposure of the TiN NHA comprises the removal of an ILD stack with only a thickness of around 650 nm. However, our release concept also allows to remove thicker ILD stacks of several micrometers in regard to a full BEOL. This is a prerequisite for future integration of the device with signal-processing circuits on-chip.

In order to achieve good device performance and high yield, we investigated various process variations. We were able to achieve a dark current density of 129 mA/cm^2 at a reversed bias of 1 V for photodetectors with a 450 nm thick Ge layer. For the responsivity we obtained a value of 0.114 A/W measured by top illumination at a wavelength of 1310 nm, with reverse bias of 1 V, with a laser power at fiber end of 1 mW and with an incident angle of 14 °. From wafer measurements of the dark current, we obtained yields of around 90% for the devices combining TiN NHAs and Ge photodetectors. Moreover, we demonstrate very stable photo currents over the entire wafer with a standard deviation of $\sigma < 6\%$. While our optical measurement setup is designed for fast on-wafer characterization, it is unable to verify refractive index sensing properties. Nonetheless, certain dependencies of optical properties on the polarization of the incident light and on the NHA design could be observed, which confirms a significant impact of the TiN NHA to optical behavior.

Our cost-effective, high-volume fabrication process for the cointegration of TiN NHAs and Ge photodetectors paves the way for the monolithic integration of RI sensor devices in a 200 mm wafer BiCMOS Si technology with high yields.

2. Design and device fabrication

All devices were fabricated on 200 mm Si wafers with a low boron background concentration of around 1E15 atoms/cm^3. A detailed description of the Ge photodetector fabrication and a discussion of the impact of detector design choices on responsivity and dark current is given in Ref. [11]. The Ge photodetector is based on a stripe configuration design and consists of several lateral PIN Ge diodes with a length of 40 µm connected in parallel by a finger contact scheme. Here, we report results on detectors consisting of nine Ge diodes with a stripe width and distance of 3.2 µm and 1.6 µm, respectively.

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Aiming for to a further reduction of the dark current, we adjusted the detector design at the substrate level. In our previous work [11], all detectors were realized on a planar Si plate. The electrical isolation by shallow trenches (shallow trench isolation – STI) was done only between complete detector devices. In this work, we designed also detectors consisting of Ge diodes, which were additionally isolated from each other on the Si substrate level (Fig. 1).

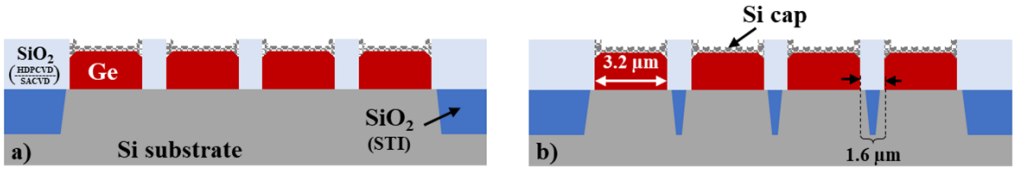

Fig. 1. Schematic of Ge photodetector stripes (a) without and (b) with additional isolation at Si substrate level

We investigated the influence of various process adaptions on performance and yield. Figure 2 shows a brief description of the realization of the Ge stripes to get a better understanding of the adapted process steps. The first process variation was a thermal oxidation of the Si surface. In Ref. [11] we demonstrated a significant improvement in the electrical properties of the detector by performing this oxidation procedure directly before the Ge epitaxy. Due to the CMOS compatibility, this step is permitted at this point of the technology process. Hence, the thermal oxidation was done after the STI module at the beginning of the process flow (Fig. 2(a)). Afterwards, the silicon dioxide (SiO_2) on the Si surface was removed by a chemical wet etching with hydrofluoric (HF) acid.

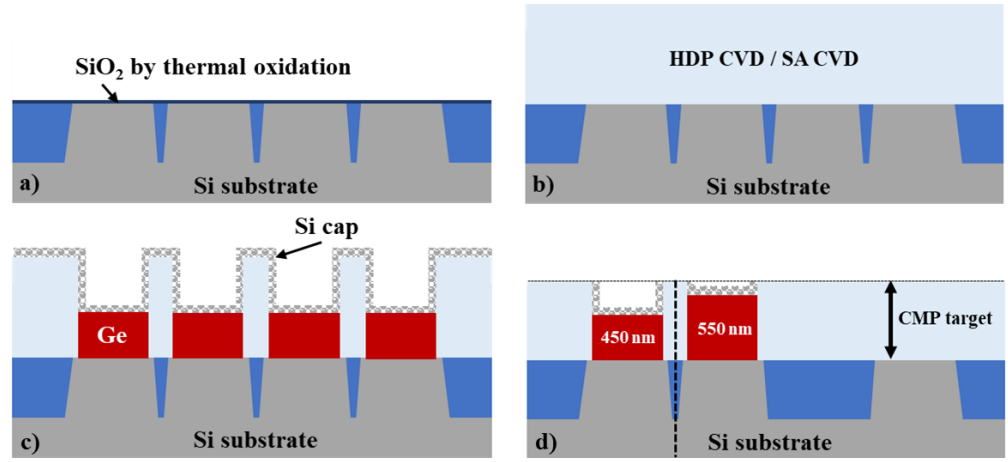

Fig. 2. Schematic description of the realization of the Ge stripes for the photodetector: (a) Thermal oxidation after the STI module; (b) SiO_2 deposition by various CVD procedure; (c) Ge epitaxy selective to SiO_2 followed by a differential epitaxy of a Si cap; (d) Removal of the Si cap on the SiO_2 surface by CMP

Another main process investigation concerned the chemical vapor deposition (CVD) of SiO_2 before the window opening of the Si regions for the Ge epitaxy. This SiO_2 deposition was done either by a high-density plasma (HDP) CVD or a sub-atmospheric pressure (SA) CVD (Fig. 2(b)).

After the window opening, germanium was deposited on Si by an epitaxy procedure selective to SiO_2. We realized process variations with different thicknesses of the Ge layer (450 nm, 500 nm and 550 nm). The next step was a differential epitaxy of a Si cap. Hence, this layer was also deposited on the SiO_2 next to the Ge regions (Fig. 2(c)).

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By a chemical mechanical polishing (CMP) the Si cap on SiO_2 surface was removed. This procedure was controlled by measuring the thickness of the SiO_2 above the Si substrate level (Fig. 2(d)). Due to the compatibility with our IHP ePIC technology [10], we are not allowed to vary this SiO_2 target for CMP. Therewith, it was identical for each Ge thickness variation. The probability of damaging the Ge stripes by CMP increases with a thicker Ge layer. Therefore, we are able to determine a kind of critical germanium thickness and a process limit for the detector fabrication. In Table 1, all process variations are summarized.

Table 1. Process variations for the fabrication of the Ge photodetector

Process	Thermal oxidation	SiO_2 deposition before Ge window opening	Ge thickness
Ox_SA_450	Yes	SA CVD	450 nm
NoOx_SA_450	No	SA CVD	450 nm
Ox_HDP_450	Yes	HDP CVD	450 nm
Ox_HDP_450	No	HDP CVD	450nm
Ox_HDP_500	No	HDP CVD	500 nm
Ox_HDP_550	No	HDP CVD	550 nm

The fabrication of the TiN NHAs was realized by the concept presented in Ref. [11], where we focused only on the structural analysis of the TiN NHA. Separately, we developed a process module for the NHA release [17]. In Fig. 3 the implementation of these modules into the technology process is described schematically. Furthermore, a schematic cross-section and a longitudinal section of a complete device with a photodetector and an integrated TiN NHA is also presented. A more detailed discussion of the Ge photodetector design can also be found in Ref. [11].

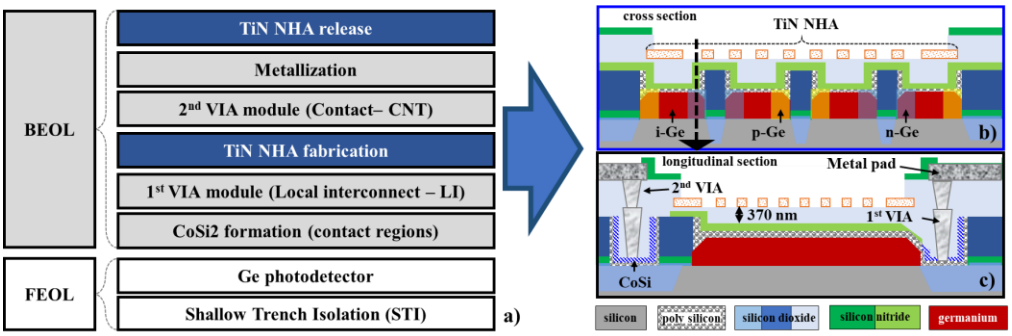

Fig. 3. (a) Schematic description of the technology process for the cointegration of Ge photodetectors and TiN NHAs as well as (b) a schematic cross section and (c) longitudinal section (at marked point in Fig. 3(b)) of the device

The NHA was fabricated in the BEOL with a vertical distance of around 370 nm to the Ge photodetectors. In the IHP photonic BiCMOS technology two vertical interconnect accesses (VIA) are implemented before the first metallization layer. The first VIA module allows a local interconnect (LI) between device components of the FEOL. LI plugs and bars structured by an anisotropic RIE step are filled by a tungsten deposition. Finally, a CMP process is used to remove the tungsten on SiO_2 surface. These process steps pave the way for the TiN NHA integration.

The NHAs were processed in a 150 nm thick TiN layer deposited by a sputtering process. Various designs were patterned via a 248 nm deep ultraviolet (DUV) lithography in a 325 nm thick photo resist. We realized TiN NHAs with pitches of 800 nm and 1330 nm and hole diameters of 600 nm and 900 nm, respectively. In Table 2 all fabricated design variations are summarized.

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Table 2. Design variations of fabricated devices

	NHA	
Design	Pitch	Hole diameter
PD-TST	— photodetector without NHA —	
P0800	800 nm	600 nm
P1330	1330 nm	900 nm

3. Results and discussion

As a first analysis in relation to the process reliability, we determined the yield of the P0800 devices in dependence on the process variations by full-wafer measurements of the dark current at a bias of −1 V (Fig. 4(a)). As a yield criterion, a maximum allowed dark current of 10 µA was set as the limit. In general, we obtained a yield of around 90% (Fig. 4(b)) for devices with an additional isolation of the Ge diodes at the silicon substrate level (Fig. 1(b)) and a Ge thickness of 450 nm.

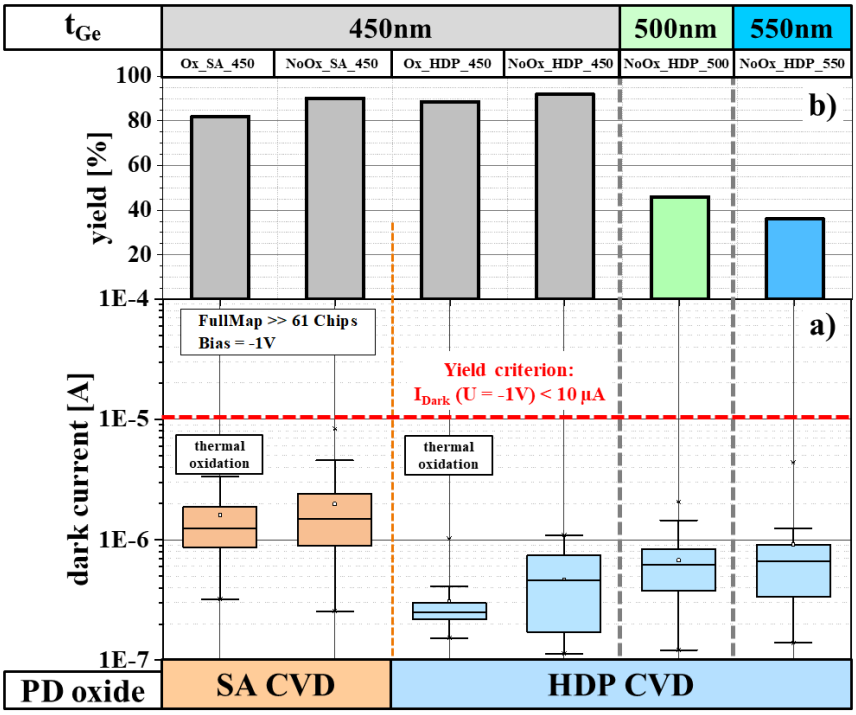

Fig. 4. (a) Full wafer measurement of dark current at a bias of −1 V and (b) analysis of the yield for various process variations of P0800; yield criterion: IDark (U = −1 V) < 10 µA

In regard to the different types of SiO_2 deposited before the window opening for the Ge epitaxy, we observed a much higher dark current for the process using an SA CVD oxide. We assume that this behavior is a consequence of an impacted Ge growth. Due to the identical pre-epitaxy clean steps for each process variation, the presence of residues on the silicon surface before starting the Ge epitaxy, which could impact the growth process, can be excluded. The epitaxy procedure itself consists of a specific step sequence comprising cyclic Ge depositions at 550 °C and cyclic anneals at 800 °C to reduce the defect density of the Ge layer [18]. We suspect that the reason for the disturbed Ge growth is the presence of SA CVD oxide. The lack of quality in

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SA CVD oxides is well known [19,20] and can be influenced by post-annealing steps. The high temperature required for the deposition of the Ge layer can result in an outgassing of atoms or molecules from the SACVD oxide, which can then be adsorbed on the silicon surface during the Ge epitaxy. This can negatively impact the defect density in the Ge, resulting in reduced layer quality and higher dark currents when the SA CVD oxide is used.

An improvement of the dark current could be achieved by the implementation of the thermal oxidation after the STI module. This process step was done to reduce defects at the silicon surface to enable the growth of high quality Ge layers. Figure 5(a) shows the IV characteristics of the PD-TST device with a Ge thickness of 450 nm with respect to different process variations. Obviously, two phenomena determine the behavior of the dark current under reverse bias. For $-0.7\,\mathrm{V} \leq \mathrm{U} \leq 0\,\mathrm{V}$, the IV characteristics for each process variation without the thermal oxidation are almost identical (red plots in Fig. 5(a)). We attribute the leakage current in this voltage range to an increased defect density at the SiGe interface. For an applied voltage lower than −0r.7 V, defects provoked by the utilization of SA CVD oxide dominate the IV characteristics. Therefore, the dark currents of the process variations with SA CVD oxide behave similarly regardless of the implementation of a thermal oxidation (solid lines in Fig. 5(a)). Overall, the lowest dark currents were obtained for the detectors fabricated with HDP CVD oxide and thermal oxidation (Ox_HDP_450). In the measured reverse voltage range, dark currents remain below 0.6 µA in that case.

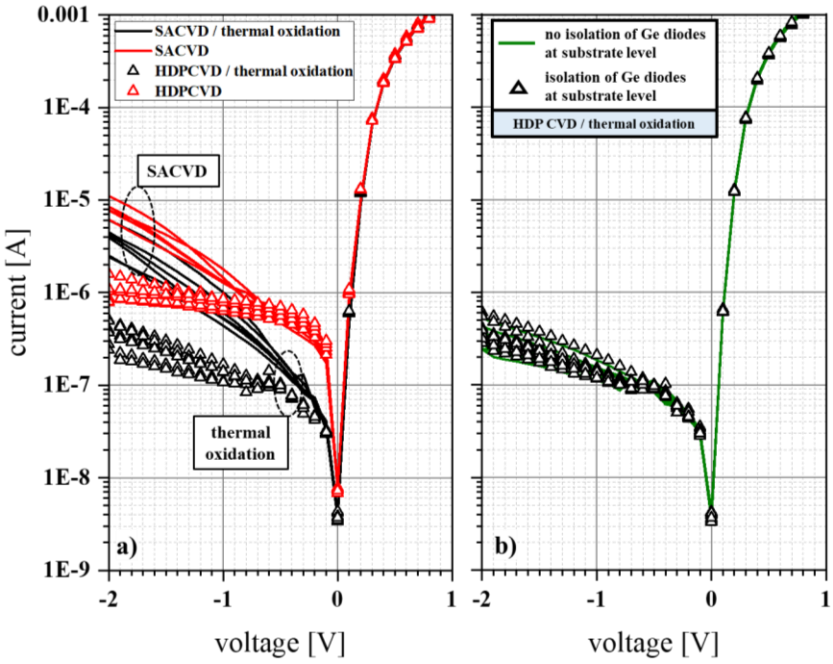

Fig. 5. IV characteristics of several PD-TST devices (a) for different process variations and (b) different design concepts ($t_{Ge} = 450$ nm)

As the IV characteristics demonstrate in Fig. 5(b) demonstrate, no impact of the isolation of the Ge diodes at substrate level can be seen on the device performance. Hence, a leakage component within the regions between neighboring Ge diodes can be excluded and the dark current is mainly determined by generation-recombination centers for carriers at the silicon germanium interface [11].

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By using HDP CVD oxide in combination with the thermal oxidation, we obtained dark currents with a median value of 249 nA and a very low standard deviation at a reverse bias of 1 V for P0800 devices with a Ge thickness of 450 nm (Fig. 4(a)). For the calculation of the dark current density we inspected the cross section of one Ge stripe with the transmission electron microscope (TEM) to determine its actual thickness (Fig. 6). We measured a maximum Ge thickness of 445 nm and a Si cap thickness of 92 nm at the center of the Ge stripe. Due to the facet formation during the Ge epitaxy on Si, the thickness is decreased at the sides of the stripe. We designed the Ge photodetector with an intrinsic zone of 2.4 µm. Hence, the main part of the facet region was doped by a corresponding high-dose implant. We used the measured thicknesses to calculate the dark current density and determined a value of 129 mA/cm^2 at a reverse bias of 1 V. Berkmann et al. [8] achieved lower dark current density for the detectors of their RI sensors of around 39 mA/cm^2 at a reverse bias of 1 V. This corresponds to a difference of less than half an order of magnitude. In contrast to our detectors, their Ge layers were deposited by molecular beam epitaxy (MBE). This expensive process enables the deposition of very high-quality layers but it is unsuitable for a high-volume fabrication.

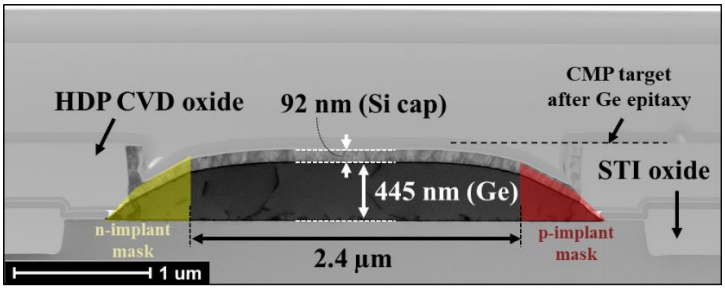

Fig. 6. TEM inspection of the cross section of one stripe of PD-TST

Figure 4(b) shows the yield of the P0800 devices for different process variations. By considering the wafer distribution in Fig. 7, we observe a growing density of defective detectors at the wafer edge. This behavior originates from the CMP process after the Ge epitaxy for the removal of the Si cap on the SiO_2 surface (Fig. 2(d)). It is well known that CMP procedures can affect the chip yield at the wafer edge [21,22]. With increasing Ge layer thickness, the conditions for CMP becomes more critical, resulting in a further decrease of the yield. In Fig. 6 the level of the CMP target height is marked, which was identical for each Ge thickness variation. Therefore, we obtain a decreasing yield for thicker detectors. For further analysis, we will only consider devices with a Ge thickness of 450 nm for the photo detector.

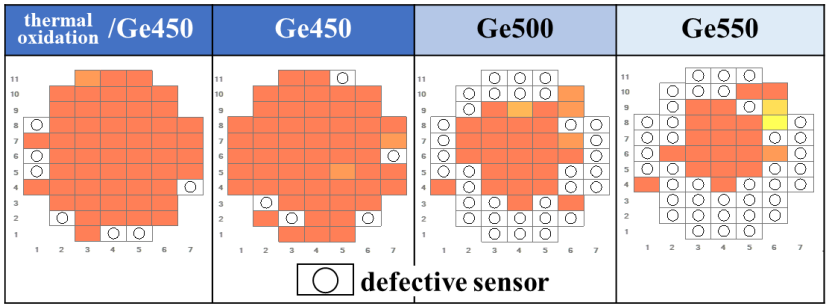

Fig. 7. Wafer distribution of defective P0800 devices for various process variations

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The TiN NHAs were fabricated after the LI module (Fig. 3). Scanning electron microscope (SEM) images show the NHAs after structuring by an RIE step (Fig. 8). The LI plugs for contacting the photodetector below the NHA are clearly visible.

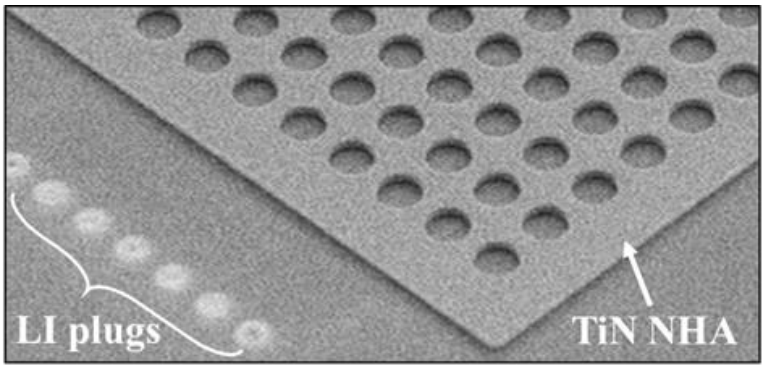

Fig. 8. SEM inspection after the fabrication of the TiN NHA in the BEOL

To verify that no impact on the contact behavior is provoked by the NHA fabrication, we carried out full wafer measurements of contact chains with more than 5000 contacts. Figure 9 shows histograms of the contact resistance RCC for different fabrication processes. We obtained similar resistances for p- and n-contacts of around 15.5 Ω, which corresponds to the target contact resistance for the Ge photodiodes of our IHP ePIC technology [10]. Hence, it could be proven that no contact degradation occurred by the NHA integration.

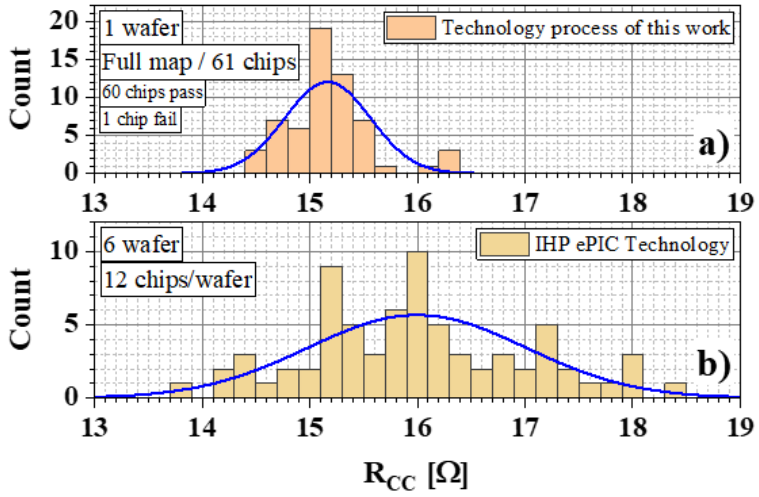

Fig. 9. Histograms of the contact resistance (a) for the technology process of this work and (b) for the IHP ePIC technology

Figure 10(a) shows a SEM image of the released TiN NHA. Moreover, the cross section of P1330 was inspected with TEM (Fig. 10(b)). An energy-dispersive x-ray spectroscopy (EDX) of the TiN NHA above the Ge photodetector demonstrates the reliability of this fabrication (Fig. 10(c)). TiN NHAs and Ge photodetectors were successfully cointegrated with a controlled release until the bottom level of the NHA.

The electro-optical characterization of the devices was performed on a 300 mm fully-automated probe system (Cascade CM300xi-SiPh) from FormFactor with Autonomous Silicon Photonics

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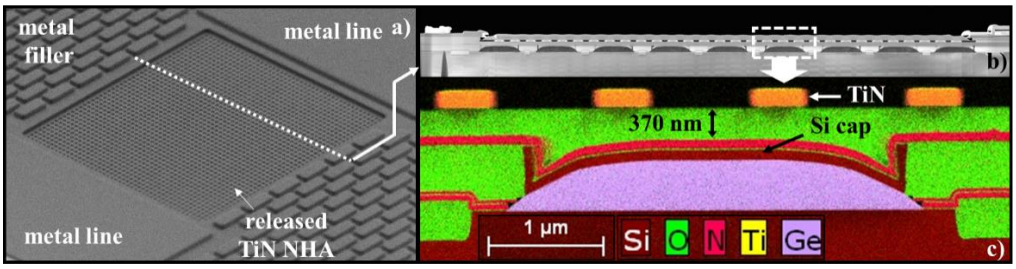

Fig. 10. a) SEM inspection of the released TiN NHA; b) TEM images of the cross section of P1330; c) EDX analysis of one Ge stripe of P1330

Measurement Assistant. This integrated SiPh solution allows sub-micron manipulation of optical fibers positioned above the wafer, automatically optimizing fiber coupling position. The dedicated algorithm uses motorized nano-positioning system for fiber alignment in X and Y axis and keeps a constant distance of 15 µm between fiber tip and sensor surface at the same time. The incident angle was set to 14 ° by using special fiber holders. All measurements were performed on wafer level at 27 °C.

The photo current of the fabricated devices was measured via top illumination. The measurements were performed with TE and TM polarized light at $\lambda = 1310$ nm and a laser power at fiber end of 1 mW (Fig. 11). On a few chips, we compared the photo current and the dark current of PD-TST and P1330 (Fig. 12). For this first analysis, all test structures were illuminated by TE polarized light.

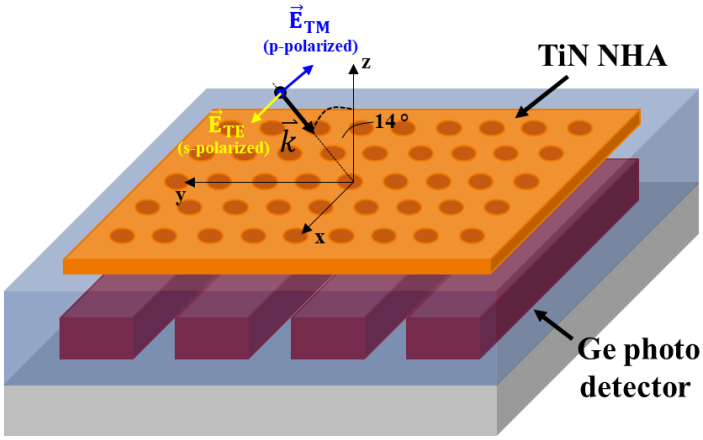

Fig. 11. Schematic of the device top illuminated with TE/TM polarized light under an incident angle of 14 °

We obtained a photo current of 114 µA for the PD-TST device. This corresponds to a responsivity of 0.114 A/W and is higher than results reported previously, where responsivities of around 0.08 A/W were achieved in photodetectors with a Ge thickness of 500 nm [9]. For our PD-TST devices with a Ge thickness of 450 nm, we attained a signal-to-noise ratio of 3 orders of magnitude. Similar results were obtained for P1330.

The stability of the photo current was characterized by full wafer measurements at a bias of −1 V for the illumination with TE and TM polarized light. For this analysis the P0800 device was also considered. In Fig. 13 the full wafer measurements are summarized via a box plot. For each device we obtained a very low standard deviation of $\sigma < 6\%$. Thus, our technology process allows

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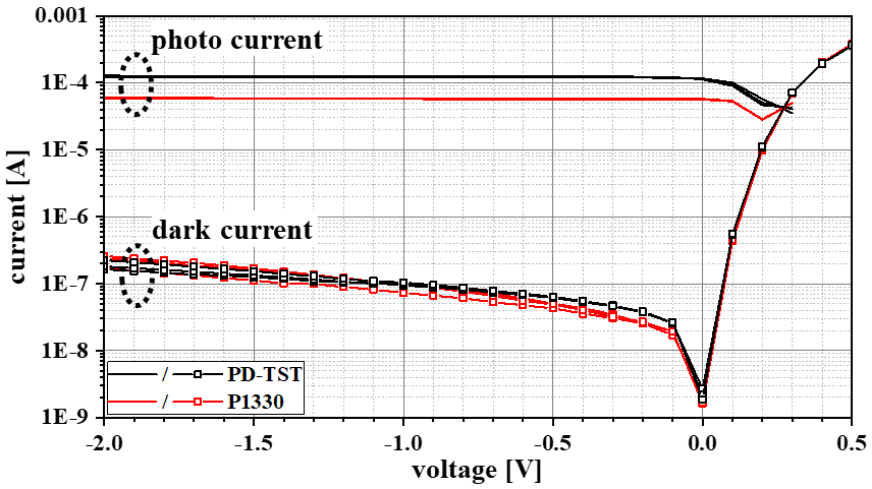

Fig. 12. Dark current and photo current of PD-TST and P1330 measured via top illumination with TE polarized light at λ = 1310 nm using an incident angle of 14 ° and an optical power at fiber end of 1 mW

a device fabrication with very stable photo currents over the entire wafer. P0800 and PD-TST exhibit slightly higher photo currents for the illumination with TE polarized light. This low difference between the polarization could be attributed to the orientation of the Ge photodetector with its stripe geometry [23]. In contrast, for P1330 we attained a larger difference between the photo currents of both polarization, which cannot be related to the stripe geometry. Moreover, the photo current measured with TE polarized light is much lower as for the TM polarization.

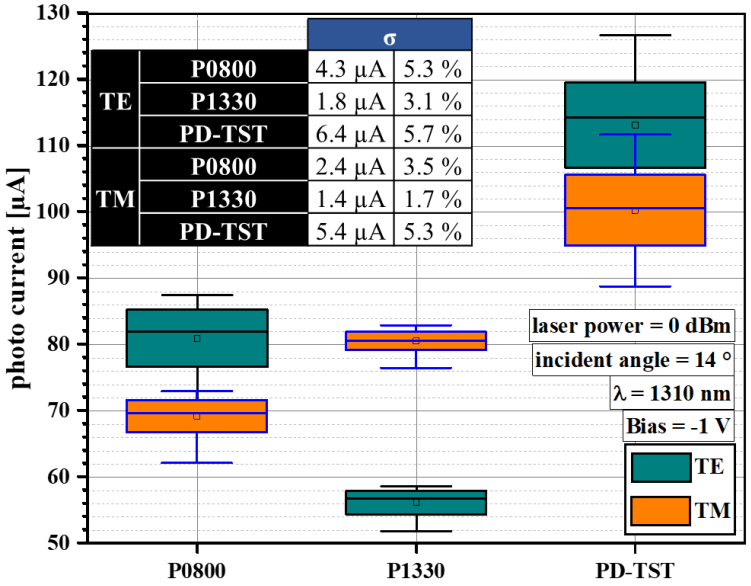

Fig. 13. Full wafer measurement of the photo current at a bias of −1 V measured via top illumination with TE/TM polarized light at λ = 1310 nm using an incident angle of 14 ° and a laser power at fiber end of 1 mW. For P1330 our results show not only a marked polarization dependence of photocurrents compared to P0800 and PD-TST but also an excellent homogeneity over the full area of the wafer.

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We analyzed the responsivity spectra at incident wavelengths between 1250 nm and 1650 nm on wafer level (Fig. 14.). Incident light was provided by three tunable laser sources (Keysight, N7776C series) via single mode fiber. The electrical signal was applied and measured with Keysight B2912A. The probing was done via two DC probes (Cascade DCP-150). We obtained different behaviors of the responsivity for each device. In addition, P1330 shows a strong polarization dependence. This behavior originates from the optical properties of the TiN NHA, which are affected by the NHA geometry (pitch and hole diameter), the refractive index of the dielectrics above and below the NHA as well as the polarization of the incident light [3–5,24,25]. Our devices are characterized in air. Their responsivity spectra do not show asymmetric Fano peaks as signs of EOT in a narrow wavelength range. Due to the measurement tolerances, there is a certain probability that the polarization settings did not match exactly the TE or TM polarization. Furthermore, the angle of incidence can deviate in a range of +/- 0.5 °. This affects the responsivity spectra. Indeed, Fano peaks are only expected for our devices when operated in liquids with a larger refractive index than that of the air and illuminated with TM polarized light in the case of oblique incidence [24]. The limited illumination wavelength range, furthermore, precludes us from detecting a pronounced impact of polarization on the responsivity spectra of P0800 – this is expected to occur at lower wavelengths, corresponding roughly to the array pitch. However, the presence of the NHA leads to a noticeable dependence of optical device properties on the polarization of the incident light in P1330. These measurement results confirm the strong influence of the TiN NHA on the photo current.

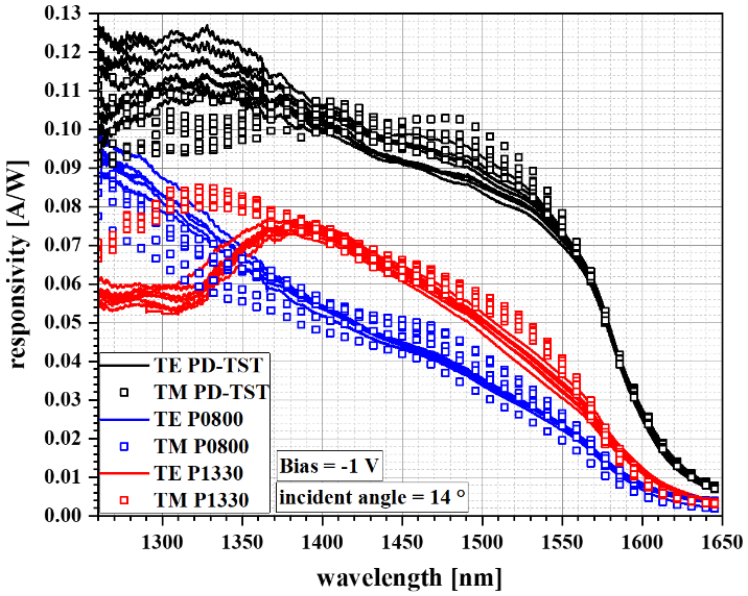

Fig. 14. Responsivity measurement in dependence on the wavelength of PD-TST, P0800 and P1330 under illumination with TE and TM polarized using an incident angle of 14 ° and a bias of −1 V

Our setup is not suitable for measurements with devices submerged in various liquids. Hence, we are not able to determine a sensitivity of our devices in dependence on a change in the refractive index. Such an analysis is subject of future work. Reiter et al. [24] already investigated the sensitivity of TiN NHAs, which were fabricated with the same process. They analyzed an NHA design with a pitch of 700 nm and hole diameter of 455 nm for different TiN layer thicknesses. A sensitivity of 765.4 nm/RIU could be achieved for 150 nm thick TiN NHAs under 15° incidence of TM polarized light. Similar sensitivities can be expected for our devices.

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Furthermore, the good quality of our TiN NHAs is also proven by reflectivity measurements, which show excellent agreement with finite-difference-time domain-simulations [24,25].

4. Conclusion

A CMOS compatible cointegration of TiN NHAs and Ge photodetectors has been demonstrated. We achieved high yields of around 90% for devices with a Ge photodetector thickness of 450 nm. The dark current density and the optical responsivity of the photodetector at a reverse bias of 1 V is 129 mA/cm^2 and 0.114 A/W ($\lambda = 1310$ nm; P = 1 mW; incident angle = 14 °; TE polarization; top illumination), respectively. The integration of the TiN NHA in the BEOL has no impact on yield or the electrical contact behavior. Photo current measurements on wafer level demonstrate the reliable fabrication of the devices. We obtained a standard deviation of $\sigma < 6\%$ in the photo current for each sensor. Furthermore, the impact of the TiN NHA on the photo current was proven by showing strong dependencies on the polarization of the incident light and on the NHA design.

This work, thus, presents a technology process for a low-cost fabrication of sensor devices with high yields. Moreover, this approach could enable the monolithic integration of RI sensors in a 200 mm wafer BiCMOS Si technology. Future device optimization could target increasing device responsivities, which would be beneficial for operating the devices as refractive index sensors. An improvement of the responsivity could, e.g., be achieved by increasing the angle of incidence for the incident light or by the realization of thicker Ge layers for the photo detector. Both strategies result in an increase in absorption length in the Ge. Concerning the Ge layer thickness, we identified an upper bound of 450 nm as a result of a CMP processing step. While the fabrication process presented here, thus, shows a significant reduction in yield upon further increasing the Ge layer thickness, it could be adapted. One possibility to fabricate photodetectors with thicker Ge layers comprises the implementation of a local back etching of the Si substrate before the Ge deposition. This approach would relax the conditions for the CMP procedures and thicker Ge layers would be feasible, provided the increase of the thermal budget required by the deposition of thicker Ge layers can be managed. Moreover, the interface roughness could be affected which could also impact dark current densities.

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