200 mm Wafer Level Characterization at 2 K of Si/SiGe Field-Effect Transistors

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Abstract

The development of a fault tolerant quantum computer necessitates an expansion to millions of physical qubits while maintaining high coherence and minimal error rates. Gated Si/SiGe spin qubits are one of the main contenders to achieve this goal, thanks to the compatibility with existing industrial CMOS processes, which heralds vast capacities and elevated quality benchmarks. Elegant architectural approaches towards scalability of qubits include the electron shuttling over long distances, which promise a reduction of peripherals and opens up space for control electronics.

The concept of Si/SiGe spin qubits and shuttling structures is based on the z-direction confinement of 2D electron gas in a Si quantum well, which is additionally tailored in the x-y-plane by potentials that arise from multiple gate layers. To trace the viability of these complex devices, it is advisable to first check basic functionality of the gate layers with teststructures, like field effect transistors (FETs). It is particularly relevant to characterize at temperatures comparable to the target operating temperature of Gated Si/SiGe spin qubits.

Recently, Fraunhofer IAF has installed a 300 mm wafer prober that can perform device characterization at temperatures as low as 2K. In the related research project, the wafer prober is implemented in a fully industry compatible feedbackloop within heterostructure growth at IHP and device fabrication at Infineon. We present in this paper the viability of this approach by comparing and discussing the current-voltage characteristics and the resulting threshold voltage measured at room temperature and at 2K of 213 FETs on a 200mm wafer. We show the significance of characterizing devices at cryogenic temperatures rather than at room temperature. At 2K, observations were made regarding the presence or absence of off-current, resulting in the clustering of I-V curves and variations in threshold voltage. The origin of these phenomena is scrutinized, examining whether they stem from the cryogenic wafer prober system or are inherent to the FET design. Possible causes are discussed and explored.

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