# *(Invited)* Advancing Si Spin Qubit Research: Process Integration of Hall Bar FETs on Si/SiGe in a 200mm BiCMOS Pilot Line

Felix Reichmann, Alberto Mistroni, Yuji Yamamoto, Philipp Kulse, Steffen Marschmeyer, Dirk Wolansky, Oksana Fursenko, Marvin Hartwig Zöllner, Giovanni Capellini, Laura Diebel, Dominique Bougeard and Marco Lisker


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## Abstract

A fault-tolerant universal quantum computer will require millions of physical qubits, necessitating a highly scalable qubit platform. Si-based spin qubits emerged as a leading candidate, boasting high fidelities, straightforward tunability, and compatibility with the CMOS fabrication process. The progress in this qubit platform in the last two years was remarkable: a 6-qubit quantum processor [1], qubits manufactured in a 300 mm foundry [2] and electron shuttling over long distances [3,4] have been demonstrated.

The technological basis of Si spin qubits are electrostatically defined quantum dots. Accumulation gates generate free carriers, typically forming a 2DEG via z-confinement, while depletion gates delineate areas in the x-y plane for hosting single electrons. In the Si/SiGe material platform, the 2DEG is formed in a strained Si quantum well (Si-QW), situated between two SiGe-Barriers. While this separates the active region from the noisy oxide interface, the 2DEG properties are heavily reliant on the heterostructure quality and consequently device fabrication processes. To refine Si/SiGe heterostructures for optimal spin qubit functionality, a meticulous feedback loop encompassing structural, chemical, and electrical analyses is indispensable. Hall bar-shaped field-effect transistors (HB-FETs) prove to be invaluable tools for comprehensive, large-scale testing of heterostructures regarding their electronic properties [5]. Through magnetotransport experiments, crucial insights into the quality of the 2DEG can be gained, including its time-dependent stability, carrier mobility, density, and tunneling mechanisms [6].

In this paper, we outline the process integration of high-quality HB-FETs onto Si/SiGe heterostructures within the IHP 200 mm BiCMOS pilot line. Our focus lies in addressing pivotal challenges encountered during device integration. Notably, the management of thermal budget emerges as crucial to prevent interface smearing of the Si-QW caused by Ge diffusion within the heterostructure. In the process of establishing ohmic contacts for HB-FETs, we utilize ion implantation, assessing the appropriate fluences and energies for optimal performance. Furthermore, we delve into the optimization of annealing parameters to ensure the optimal activation of dopants without compromising the integrity of the heterostructure. Ensuring high-quality gate dielectrics is essential for a low-disorder 2DEG. Consequently, we undertake a comparative examination of various oxides within our fabrication line to evaluate their defect densities. While $Al_2O_3$ enjoys widespread usage in literature, our findings indicate superior performance with high-density plasma $SiO_2$. Finally, we demonstrate the performance of our HB-FETs and Heterostructures. Our internal feedback loop of structural, chemical and electrical analysis, the latter using HB-FETs, allowed us to achieve 2DEGs of extremely high mobility (above 300.000 $cm^2/Vs$) and low percolation density (below 1E11 $cm^{-2}$).

Our research provides a pathway to the fabrication of critical components for Si spin qubits, which can help to advance the research in this field and may unlock the full potential of this platform.

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