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Efficiency and time resolution of monolithic silicon pixel detectors in SiGe BiCMOS technology

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Abstract: A monolithic silicon pixel detector prototype has been produced in the SiGe BiCMOS SG13G2 130 nm node technology by IHP. The ASIC contains a matrix of hexagonal pixels with pitch of approximately 100 µm. Three analog pixels were calibrated in laboratory with radioactive sources and tested in a 180 GeV/c pion beamline at the CERN SPS. A detection efficiency of $(99.9^{+0.1}_{-0.2})\%$ was measured together with a time resolution of (36.4 ± 0.8) ps at the highest preamplifier bias current working point of 150 µA and at a sensor bias voltage of 160 V. The ASIC was also characterized at lower bias voltage and preamplifier current.

Keywords: Instrumentation and methods for time-of-flight (TOF) spectroscopy; Particle tracking detectors; Particle tracking detectors (Solid-state detectors); Timing detectors

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1 Introduction

Since several years the particle-physics community has devoted an increasing interest to the timing performance of silicon [1, 2] for the detection of ionising radiation. In a pixelated hybrid detector, the NA62 GigaTracker [3] achieved time resolution down to 150 ps. The ATLAS and CMS Collaborations are upgrading their detectors for the High Luminosity LHC program with planes of Low Gain Avalanche Detectors (LGAD) [4, 5]. LGADs are planar silicon sensors that exploit the increase of the signal-to-noise ratio given by an internal gain of 10–50 to provide time resolutions of approximately 30 ps. Those employed in the ATLAS and CMS timing layer have an area of about 1.6 mm^2.

An alternative approach to obtain the signal-to-noise ratio necessary to achieve such time resolution comes from the exploitation of the unparalleled analog performance of Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBT) to produce a fast signal amplification with low noise at low amplifier current density [6, 7]. An R&D effort started in recent years to exploit commercial SiGe BiCMOS — a mainstream microelectronic technology with Very Large Scale Integration (VLSI) capability - to produce monolithic pixel detectors with small pixel size and time resolution comparable with that of LGAD, without recurring to an avalanche gain mechanism [8, 9].

Laboratory measurements with radioactive sources of the first monolithic silicon pixel detector prototype in the 130 nm SG13G2 IHP process [10] with 100 µm pixel pitch demonstrated that time resolutions at the level of 50 ps can be achieved [11, 12]. Such remarkable timing performance for a silicon sensor without an internal gain layer was obtained at rather high discrimination threshold,

which was possibly affecting the sensor detection efficiency. Furthermore, there were indications that the resolution on the signal time-over-threshold (TOT), which was used to correct for signal time-walk, was limiting the timing performance of the detector. These considerations suggested that a study of the analog signals and an improved time-walk correction method would be necessary to fully exploit the timing capability of this type of silicon detector maintaining at the same time very high efficiency.

For this purpose a second monolithic silicon pixel ASIC prototype was produced in the same 130 nm IHP process. The ASIC contains four sub-matrices of pixels with digital readout as well as four analog pixels with the preamplification stage followed by an analog driver with dedicated output pads. Although a full description of the ASIC is given in section 2, the measurements presented in this paper focus on the analog pixels, since the possibility to measure the full output waveform allows for a better insight on the circuit performance, decoupling the front-end characteristics from the digital logic, therefore permitting a detailed study of the efficiency and timing response. The analog channels were characterized in laboratory tests with radioactive sources at the University of Geneva and with minimum ionizing particles (MIPs) at the CERN SPS testbeam facility.

2 Description of the ASIC

2.1 Architecture and floorplan

The ASIC prototype was produced in the IHP SG13G2 130 nm BiCMOS technology with a wafer resistivity of 50 Ω cm. It features a matrix of 12×12 monolithic hexagonal pixels of 65 µm side with a pixel capacitance of 80 fF.[1] The ASIC floorplan is shown in figure 1. Each pixel includes an HBT-based frontend, a fast discriminator and an 8-bit threshold-tuning DAC. A common digital logic placed beside the matrix (from now on called "periphery") contains the readout logic, a dedicated timing digitization circuit, a number of DACs to provide the bias voltages, and currents to the pixels and an SPI slow-control interface to program them.

The pixels are built using the n-well as sensor cathode, biased at a positive bias voltage that can be changed via an external power supply, and the p-doped substrate as the anode. The anode is biased at a negative high voltage (≤ -80 V in the data presented here). The presence of this high-voltage bias forces all the electronics to be insulated by the substrate it in order to avoid breakdown. Hence, every nMOS is placed in insulated p-wells, divided in three power domains. A series of 18 guard-rings are placed around the edge of the chip to insulate the substrate.

The output of the discriminator is sent to a Time-to-Digital Converter (TDC) positioned in the periphery to calculate a timestamp for the hit and measure the TOT of the signal. The ASIC integrates three separate TDCs, each wired to a fast-or line connected to different pixels. The fast-or lines are interleaved so that two adjacent pixels are always connected to separate TDCs: this ensures that in the event of a particle hitting multiple adjacent pixels, the timing information can be measured from all of them independently. The TDC architecture is described in [13]. A 9-stage pseudo-nMOS feed-forward ring oscillator is used with a set of latches to sample the oscillator state. The TDC resolution is about 30 ps. Each TDC features three measurement channels: one for the event timestamp, one for ToT and one for calibration purposes.

[1] The sensor implemented in the pixel is essentially the same sensor of [12].

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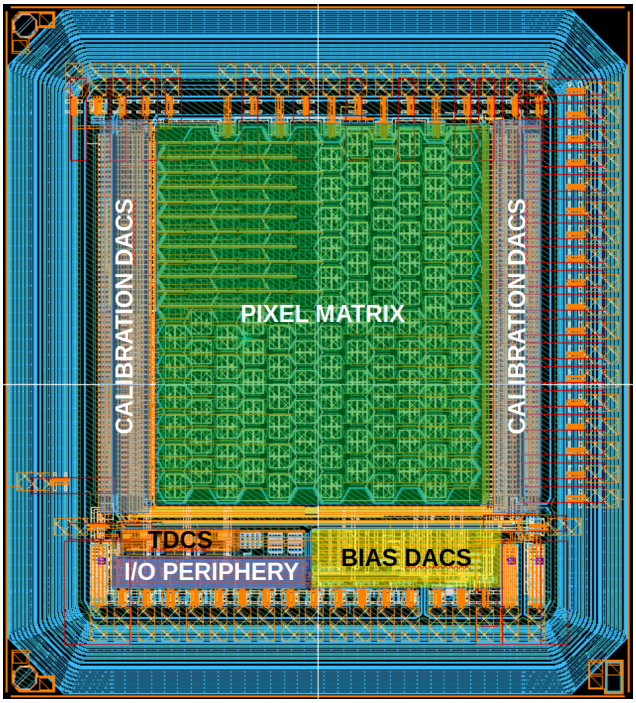

Figure 1. Floorplan of the monolithic pixel detector prototype. The ASIC size is $2.3 \times 2.5\,\mathrm{mm}^2$. It contains four sub-matrices of 6×6 hexagonal pixels with a pitch of approximately 100 µm.

2.2 Front-end flavors

The pixel matrix is divided into four 6×6 sub-matrices, each with a different amplifier design. The discriminator, calibration DACs and readout interface are the same. The basic schematic of the preamplifier can be seen in figure 2. It consists of a SiGe HBT used as a charge sensitive amplifier, with a pMOS load and an MOS-based floating resistor used as a feedback. The architecture is similar to the one the authors developed for [11], which yielded to excellent timing performance. This circuit is followed by a MOS discriminator that compares the output of the preamplifier to a fixed threshold to determine if the pixel was hit by a particle. The four sub-matrices contain different variations of this circuit:

- The circuit in figure 2, with the preamplifier, discriminator and calibration DAC placed outside of the active pixel area;
- The same circuit, with the preamplifier integrated in the pixel n-well;
- The same amplifier, but with an added HBT common collector driving stage placed before the discriminator;
- A version of the circuit with two discriminators with different thresholds, to calculate the rising slope of the input signal directly and perform a more accurate time-walk correction.

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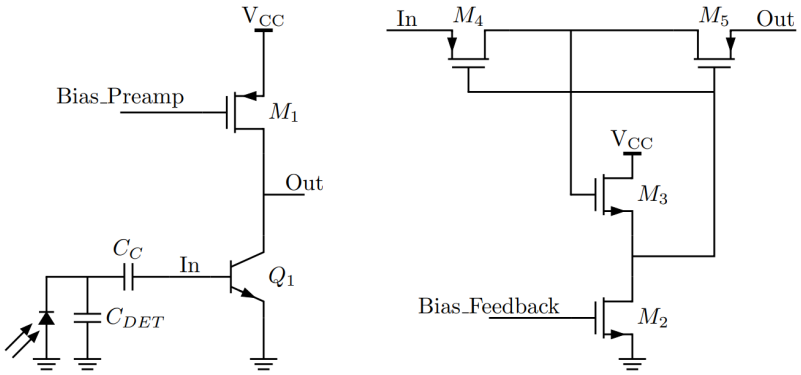

Figure 2. Schematic layout of the BJT-based preamplifier of the prototype ASIC. The left block is a common-emitter configuration capacitively coupled to the sensor, while the right one implements a floating MOS-based feedback resistor.

2.3 Analog pixels

One of the sub-matrices hosts four analog pixels (figure 3). They contain the same HBT amplifier represented in figure 2, followed by an analog driver directly connected to output pads to be measured with an oscilloscope. The driver is composed by two consecutive HBTs in common collector configuration, with the first stage AC coupled to the output of the amplifier. The first stage of the driver has a configurable output impedance, while the second stage is terminated on a 500 Ω resistor in chip. The entire front-end is placed outside of the pixel area, in proximity of the output pads, as shown in figure 3. The short routing from the pixel to the amplifier input is estimated to contribute a capacitance of less than 10 fF.

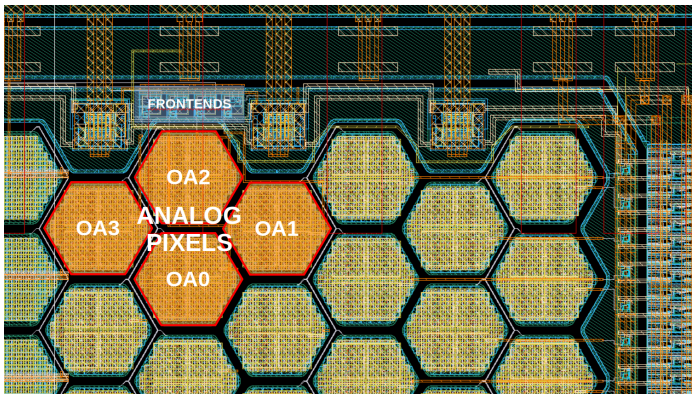

Figure 3. Detail of the ASIC layout that shows the four pixels directly connected to output pads. During the CERN SPS testbeam, pixels OA0, OA1 and OA2 were read by an oscilloscope. This study is based on the data acquired with these three analog pixels.

2.4 Slow-control and readout interface

The periphery of the chip contains, in addition to the I/O pads, thirteen 8-bit DACs to tune all the bias voltages and currents used by the analog blocks in the pixels. Each DAC is programmable via a

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standard SPI interface using 16-bit commands (8 to address a specific DAC, 8 for the DAC value). The same SPI interface can be used to program a "mask" bit for individual pixels (i.e. force their output to be ignored by the readout logic). This is useful in case of malfunctioning pixels, or to test only some parts of the chip at a time. A special SPI command is also used to initiate a frame readout. As soon as this command is sent, the content of the TDCs and the address of the pixel hit is read out via a low-voltage differential line. The state of the pixel is then reset, to be able to acquire a new frame.

3 Amplifier response calibrations

Laboratory measurements with X-ray sources were performed to characterize the analog response of the front-end electronics of two ASICs, that will be called here Detector Under Study 0 (DUT0) and 1 (DUT1). For these measurements and those described in section 4, the outputs of the analog drivers were connected to a 50 Ω coaxial cable and AC coupled via a 100 nF capacitor to a Lecroy WaveMaster 820zi oscilloscope. The oscilloscope has a sampling rate of 40 Gs/s and analog bandwidth limited to 4 GHz. A ^{109}Cd source was used to measure the gain of the electronic chain, which comprises the pixel, the preamplifier and the driver. To study the response of the electronics as a function of the power consumption, four different working points were adopted, with amplifier bias current I_{preamp} = 7 µA, 20 µA, 50 µA and 150 µA.

The two main photons from the ^{109}Cd source derive from the ^{109}Ag X-ray K lines of energy E_1 = 22.16 keV and E_2 = 24.94 keV. The spectrum of ^{109}Cd was fitted with a double Gaussian function. Figure 4 shows one example of the spectra from DUT0, while figure 5 shows the amplitude values obtained from the fit of the same spectrum as a function of the deposited charge, assuming an energy of 3.6 eV to generate and electron-hole pair in silicon. A linear fit of the data was used to estimate the charge gain (A_q) of the front-end electronics.

The Equivalent Noise Charge (ENC) of the front-end was then calculated as

$$\mathrm{ENC} = \frac{\sqrt{\sigma_V^2 - \sigma_{\mathrm{scope}}^2}}{A_q}$$

where σ_V is the standard deviation of the electronics-noise distribution measured on the oscilloscope when the front-end is connected, and σ_{scope} = 420 µV is the voltage noise of the oscilloscope with the open input connector. The results of the gain and ENC measurements are summarized in table 1. The two DUTs show the same trend within approximately 10%. At I_{preamp} = 50 µA the ENC is as low as 50 electrons. As expected, it increases significantly for smaller I_{preamp} values, which could produce a degradation of the detection efficiency. The increase of the ENC at I_{preamp} = 150 µA is due to the configuration of the amplifier used for this working point.

4 Efficiency and time resolution measurement

4.1 Testbeam experiment setup and data set

The detection efficiency and time resolution of the prototypes were measured at the CERN SPS testbeam facility with a pion beam with 180 GeV/c momentum. The experimental setup consisted of the UniGe FEI4 telescope for particle tracking [14], with the two devices under test (DUT0

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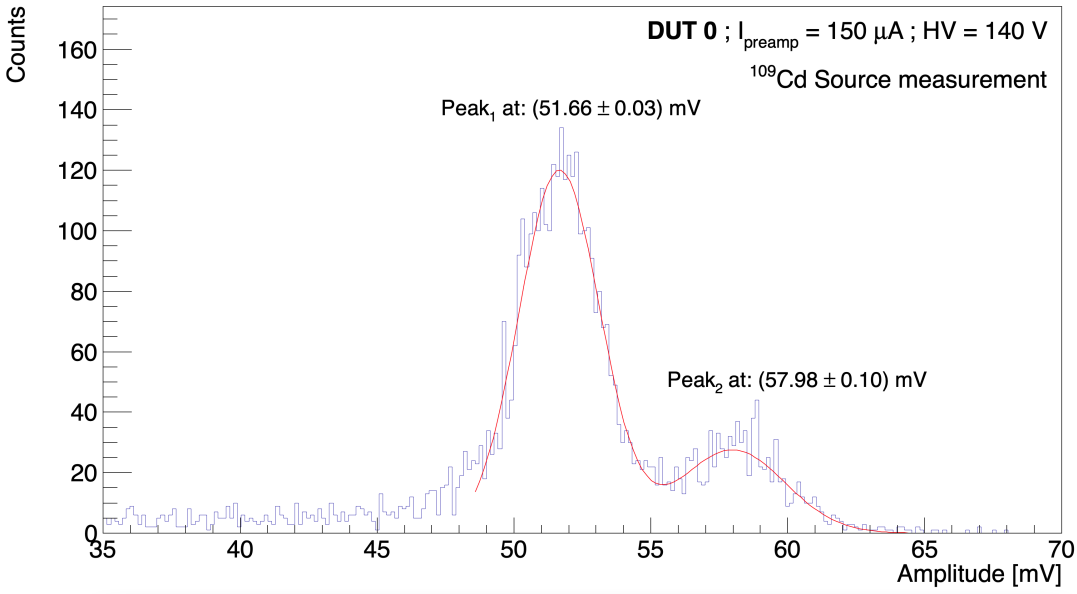

Figure 4. Spectrum of the ^{109}Cd source measured at the working point I_{preamp} =150 µA and HV = 140 V. The two peaks, corresponding to the X-ray emission of ^{109}Ag, were fitted with a double Gaussian function.

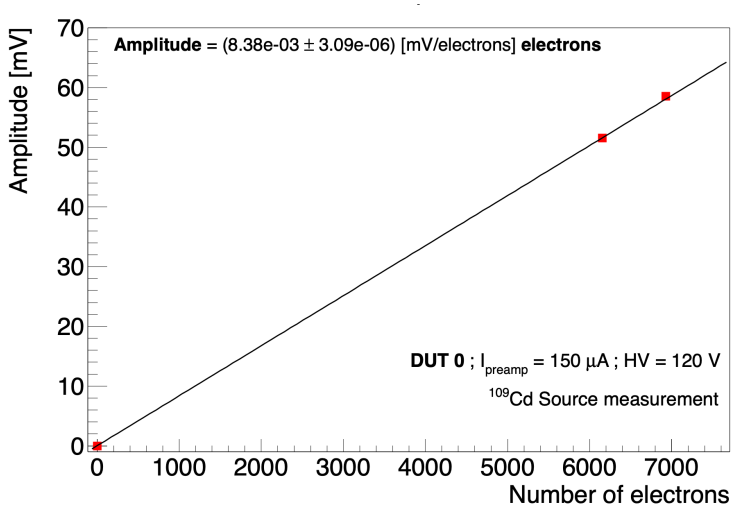

Figure 5. Example of the amplitude measurement as a function of the number of electrons obtained with the ^{109}Cd source for one of the working points for DUT0. The superimposed linear fit is used to parameterise the response of the front-end at this working point.

upstream with respect to the beam, DUT1 downstream) placed after three detection planes of the telescope as shown in figure 6. The DUTs were operated at room temperature. The DUTs were read by two oscilloscopes with analog bandwidth of 4 GHz and a sampling rate of 40 GS/s and 20 GS/s, respectively. The DUTs were positioned specularly to each other and pixels OA0 (shown in figure 3) from the two chips were aligned and sent to the oscilloscope with the largest sampling rate to make Time-Of-Flight (TOF) measurements. The data from pixels OA1 and OA2 of the two DUTs, which were not aligned among the two DUTs, were also acquired.

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Table 1. Power density, voltage noise, charge gain and ENC of the analog front-end electronics at the four I_{preamp} working points for HV = 120 V. The power density is calculated for a matrix of pixels with 100 µm pitch. The lower ENC value measured at I_{preamp} = 50 µA is due to a different configuration of the amplifier and driver working point that acts as a filter for noise, thus reducing the bandwidth.

		DUT0			DUT1		
I_{preamp} [µA]	Power density [mW/cm^2]	σ_V [mV]	A_q [mV/fC]	ENC [electrons]	σ_V [mV]	A_q [mV/fC]	ENC [electrons]
7	84	1.35	42.3	194 ± 1	1.41	49.2	171 ± 2
20	240	0.82	43.4	102 ± 1	0.83	46.0	97 ± 1
50	600	0.70	55.0	54 ± 1	0.58	50.5	50 ± 1
150	1800	0.81	52.4	76 ± 1	0.72	44.4	82 ± 1

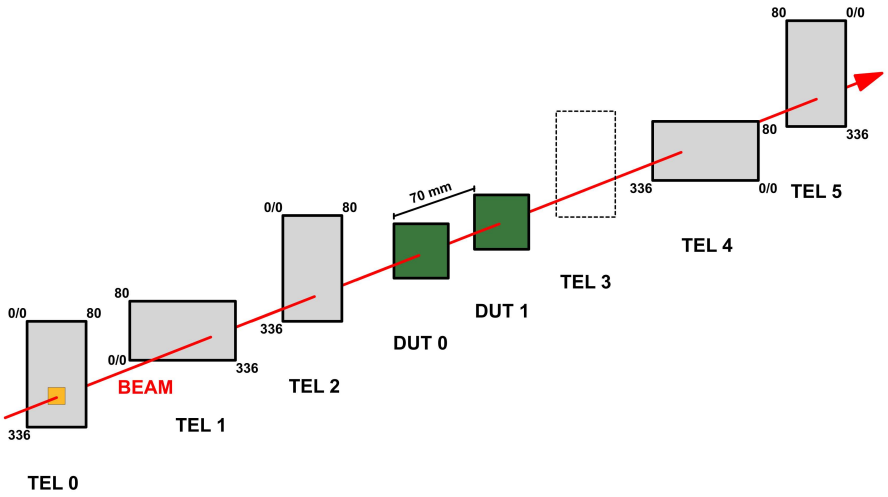

Figure 6. Schematic view of the experimental setup, showing the five FEI4 telescope [14] planes that were operated and the two DUTs in green. Plane TEL3 was not operational during this testbeam measurement. The FEI4 readout chip has a matrix of 80 × 336 pixels with a pixel size of 250 × 50 µm^2. The telescope planes are alternatively rotated by 90° to optimise the space resolution on the two transversal directions. A region of interest, shown by the yellow area, was imposed to the first plane of the telescope, and was put in coincidence with the last telescope plane to generate the trigger.

The analysis of the data was performed using the full waveform information acquired by the oscilloscopes. The signals from the DUTs were delayed to guarantee that they were always in the second half of the waveform time window acquired by the oscilloscope. This configuration allowed using the first half of the waveform to determine the voltage noise σ_V at the output of the analog front-end and set a discrimination threshold V_{th} as a multiple of the voltage noise, independently for the two DUTs. Figure 7 shows a typical waveform with a signal pulse from a MIP at the working point with I_{preamp} = 150 µA. The dashed line represents the discrimination threshold at $V_{th} = 6\ \sigma_V$.

The FEI4 telescope provided the trigger to the oscilloscopes. A Region Of Interest (ROI) of 250 × 600 µm^2 was set on one of the trigger planes of the telescope, centered around the pixels OA0 of the two DUTs that were aligned with respect to the beamline and used for the TOF measurement.

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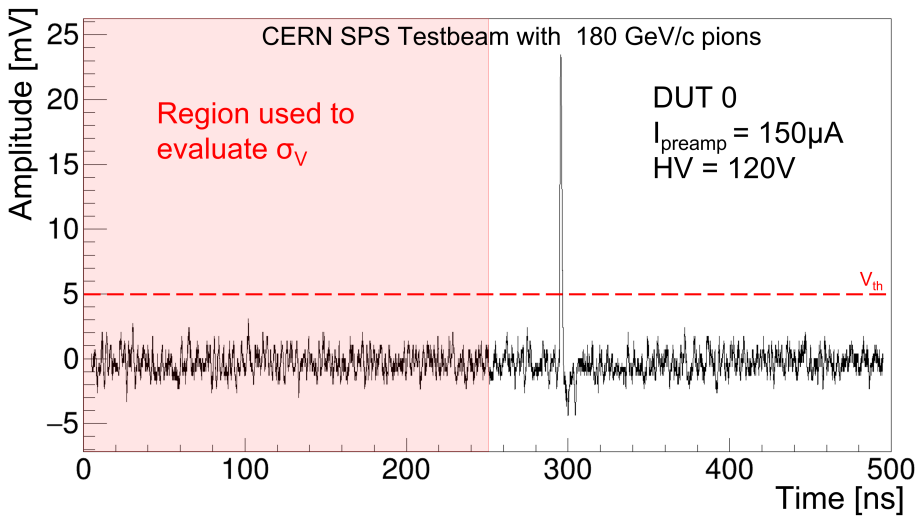

Figure 7. Example of a waveform from working point $I_{\text{preamp}} = 150\,\mu\text{A}$. The shaded region below 250 ns is the portion of the waveform used to extract σ_V. The dashed line shows the discrimination threshold used for this working point.

Data were acquired with DUT0 and DUT1 at the same four front-end working points used for the characterization of the DUTs with radioactive sources (section 3) for a bias voltage of 120 V. At this potential the substrate is not fully depleted. The depletion depth is estimated to be 23 µm, which corresponds to a most probable charge $Q_{\text{MPV}} \approx 1300$ electrons for a MIP.

A high voltage scan was also performed only for the working point $I_{\text{preamp}} = 150\,\mu\text{A}$.

To evaluate the efficiency and time resolution of our DUTs in the cleanest possible way, a selection was applied on the quality of the tracks reconstructed by the FEI4 telescope. The selection consisted in discarding events in which more than one track was reconstructed by the telescope, and in accepting only those events with the reconstructed track having an associated hit in each of the five telescope planes and a $\chi^2/\text{NDF} \leq 1$. About 30% of the triggered events survived this stringent selection on the tracks from the telescope. For this final sample the telescope pointing resolution on the DUT planes was estimated to be approximately 10 µm [15].

4.2 Cross talk and robustness to induced noise

During laboratory and testbeam measurements, cross talk between the channels was observed for events with large charge deposition, corresponding to approximately five times the MIP most probable charge. The analysis of these events showed that this cross talk was not influenced by the relative position of the pixels within the matrix or the routing of the signal before and after the amplification. Therefore the observed cross talk could be ascribed to two possible causes. The first is a feedback path passing through the ground of the board, which is then injected to the backside of the chip through the HV decoupling capacitors and finally in the amplifier input. This hypothesis is supported by the fact that the system becomes less stable at bias voltages below 50 V, when the pixel capacitance is significantly larger. The second cause is noise induced by the driver pulse propagating in the power supply, since in this prototype the analog and driver electronics share the same supply lines.

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As a consequence of this cross talk, only events in which the pixel under test had the largest signal among the three acquired pixels were selected for the time resolution measurement. No selection was applied for cross talk in the efficiency measurement, since cross talk appears only for efficient events.

4.3 Efficiency measurement

For the calculation of the efficiency, all the selected pion tracks reconstructed by the FEI4 telescope were extrapolated to the surface of each of the two DUTs. Only the tracks crossing a DUT within the area of the three pixels under study, or outside the external edges of the pixels by at most one standard deviation of the telescope resolution, were retained. An event was considered efficient if the signal in at least one of the pixels crossed the discrimination threshold.

Figure 8 shows the efficiency map for the two DUTs at the $I_{\text{preamp}} = 150\,\mu\text{A}$ working point, for a threshold of $6\sigma_V$ and a sensor bias HV = 120 V. The panels show the efficiency map for the entire surface of the three pixels (the pixel edges are represented by the black lines). The degraded efficiency measured nearby the twelve external sides of the hexagonal pixels is produced by the FEI4 telescope resolution, as attested by the fact that such degradation of the efficiency is not observed in the region of the three internal hexagon sides between the pixels. To avoid biases stemming from the pointing resolution of the FEI4 telescope, the measurement of the detection efficiency was restricted to events with tracks extrapolated inside the triangular area[2] in between the three pixels that is delimited by the red lines in figure 8.

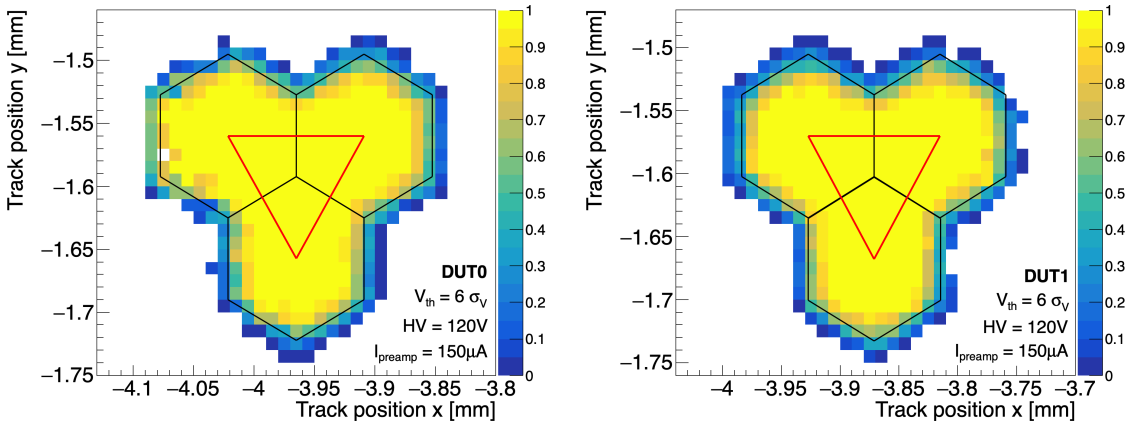

Figure 8. Efficiency map measured for DUT0 (left) and DUT1 (right) at $I_{\text{preamp}} = 150\,\mu\text{A}$, threshold $V_{th} = 6\ \sigma_V$ and HV = 120 V. The pixel edges are shown by the black lines. The efficiency degradation around the external edges of the three pixels is due to the FEI4 telescope resolution. The efficiency measured inside the triangular area delimited by the red lines is unaffected by the telescope pointing resolution and is used throughout this study.

Figure 9 and table 2 show the efficiency obtained within the triangular area for the four preamplifier working points at a discrimination threshold of 6 σ_V and at a sensor bias voltage of

[2]It should be noted that this triangular area constitutes exactly one sixth of the total area of the three pixels, which is representative of all the zones of a pixel (central-pixel zone; zone in between two pixels; zone in between three pixels) in the right geometrical proportions. Therefore, the efficiency measured inside it provides a reliable estimation of the efficiency over the entire hexagonal pixel area, unbiased by the telescope resolution.

120 V. The efficiency follows the trend expected from the ENC measurement of table 1. All the preamplifier working points show an efficiency well above 99% except for the one at 7 µA. At this current a larger depletion depth would be required to operate the front-end at even higher efficiency. It is also noted that DUT0 shows a lower efficiency, compatibly with the larger ENC measured with the ^{109}Cd source (section 3). At higher currents DUT0 is slightly more efficient than DUT1. To investigate this difference, the efficiency as a function of the discrimination threshold was inspected. The results are reported in figure 10 for HV = 120 V. The threshold scan indicates a clear difference in performance, in spite of the fact that both DUTs reach the efficiency plateau at a threshold of six standard deviations of the noise.

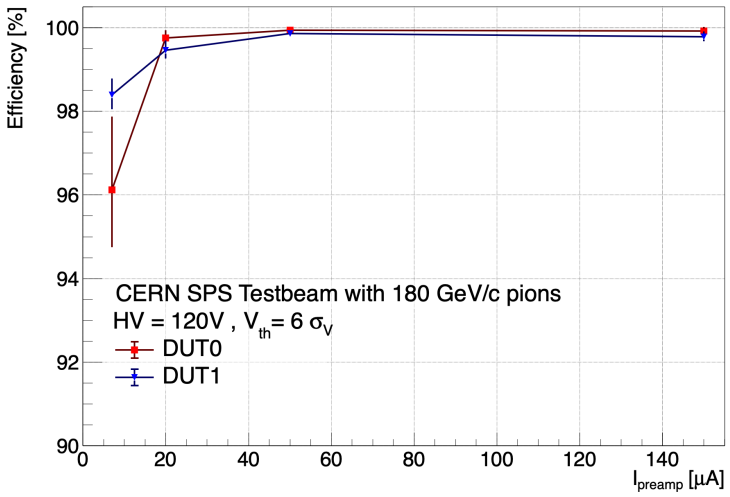

Figure 9. Efficiency vs. I_{preamp} for HV = 120 V, evaluated in the triangular inter-pixel zone for DUT0 (in red) and DUT1 (in blue).

Table 2. Efficiency of the two DUTs at different I_{preamp} for HV = 120 V. The efficiency is measured according to the definition given in the text. The uncertainties are statistical only.

Efficiency measured at HV = 120 V				
I_{preamp} [µA]	7	20	50	150
Efficiency DUT0 [%]	$96.1^{+1.4}_{-1.7}$	$99.75^{+0.12}_{-0.17}$	$99.94^{+0.03}_{-0.05}$	$99.91^{+0.05}_{-0.08}$
Efficiency DUT1 [%]	$98.4^{+0.3}_{-0.4}$	$99.45^{+0.2}_{-0.2}$	$99.86^{+0.05}_{-0.07}$	$99.78^{+0.08}_{-0.11}$

The efficiency measurement of a sensor HV scan carried out for the working point I_{preamp} = 150 µA is reported in figure 11 and table 3. The scan shows that the two DUTs are in the efficiency plateau at 120 V. At the 50 Ω cm substrate resistivity of this prototype, increasing the HV from 120 V to 160 V increases the depletion depth by 15%, which has little or no contribution for the working point at the highest power consumption, but could have been beneficial for the front-end operation at 7 µA for which a small drop in efficiency was observed (figure 9).

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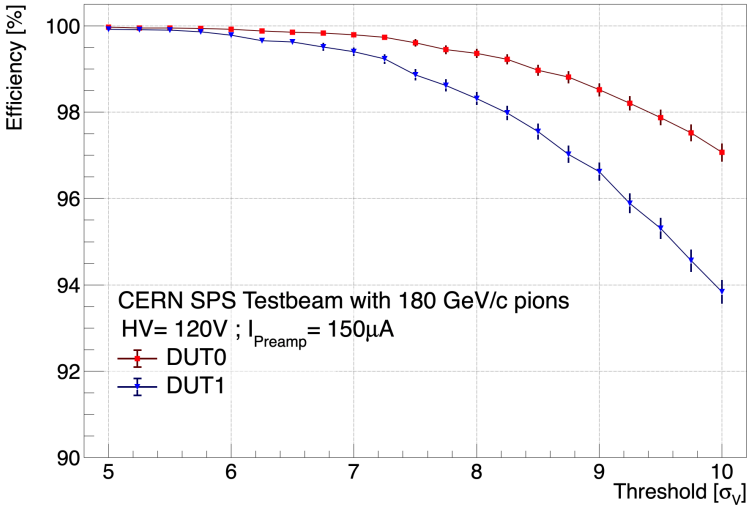

Figure 10. Efficiency vs. discrimination threshold measured within the triangular inter-pixel zone for DUT0 (in red) and DUT1 (in blue).

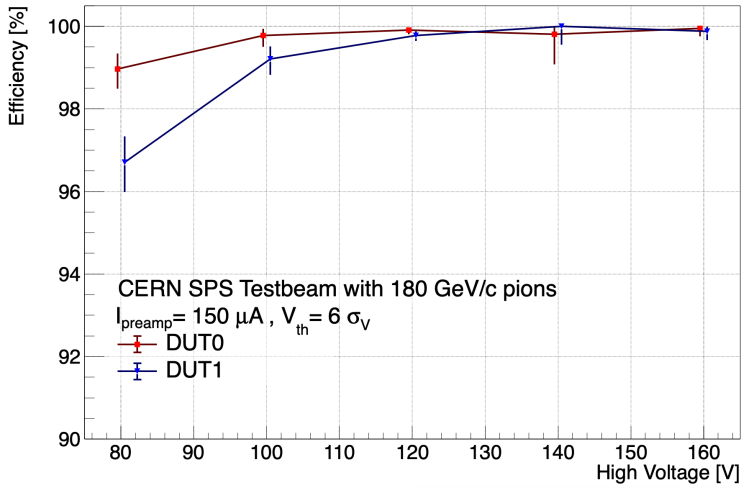

Figure 11. Efficiency vs.sensor bias voltage for the two DUTs at $I_{\mathrm{preamp}} = 150\,\mu\mathrm{A}$ and voltage threshold of $6\,\sigma_V$. The vertical error bars show the statistical uncertainties.

Table 3. Efficiency at different HV values for the two DUTs for $I_{\mathrm{preamp}} = 150\,\mu\mathrm{A}$. The efficiency is measured according to the definition given in the text. The uncertainties are statistical only.

Efficiency measured at $I_{\mathrm{preamp}} = 150\mu\mathrm{A}$					
HV [V]	80	100	120	140	160
Efficiency DUT0 [%]	$98.97^{+0.35}_{-0.46}$	$99.78^{+0.14}_{-0.26}$	$99.91^{+0.05}_{-0.08}$	$99.81^{+0.18}_{-0.71}$	$99.95^{+0.04}_{-0.18}$
Efficiency DUT1 [%]	$96.70^{+0.61}_{-0.70}$	$99.21^{+0.28}_{-0.37}$	$99.78^{+0.08}_{-0.11}$	$100.^{+0.00}_{-0.42}$	$99.88^{+0.09}_{-0.20}$

4.4 Time resolution measurement

For the time resolution measurement, the pixels OA0 of the two DUTs were carefully aligned with respect to the beamline and events in which the two pixels registered signals with amplitudes above a discrimination threshold of 6 σ_V in coincidence were selected. Furthermore, the telescope-track quality selection described in section 4.1 and the cross-talk selection described in section 4.2 were applied. To avoid biasing the sample with a geometrical selection, no requirement on the telescope-track position was imposed.

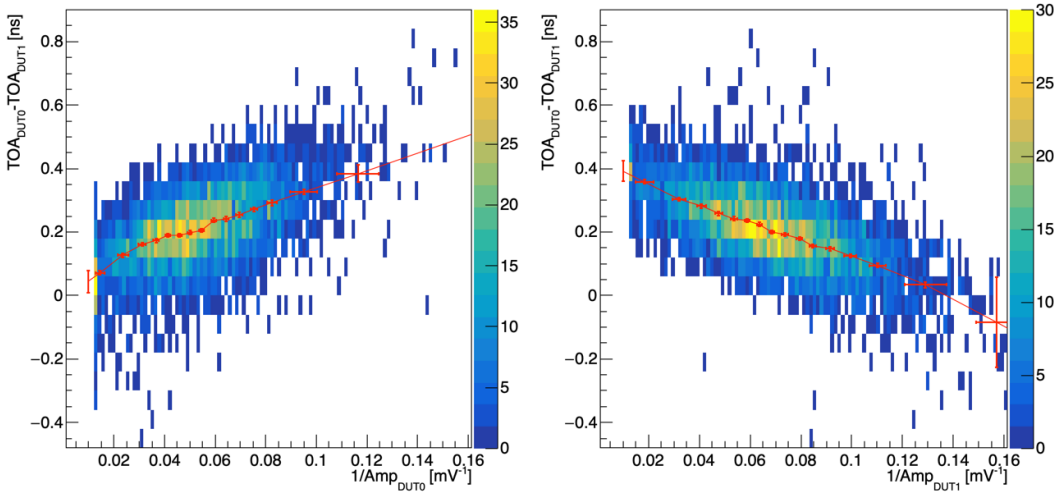

Figure 12. Distributions of the difference in TOA between the two DUTs vs. the inverse of the amplitude that was used for the time-walk correction of DUT0 (left) and DUT1 (right). Both DUTs were operated at I_{preamp} = 150 µA and HV = 160 V. The time-walk correction points (in red) were obtained by a Gaussian fit on each bin of the inverse of the amplitude. The red segments show the linear interpolation between the time-walk correction points used to correct the data. The TOA difference contains an arbitrary offset that is irrelevant for the measurement of the time resolution.

Time-walk correction. Figure 12 shows the difference in the Time-Of-Arrival (TOA) measured in pixels OA0 of DUT0 (TOA0) and DUT1 (TOA1) as a function of the inverse of the signal amplitude in DUT0 (left) and DUT1 (right) for the working point at 150 µA and HV = 160 V. The data show a large variation of the average of the difference TOA0−TOA1 as a function of the signal amplitudes, of the order of a few hundreds ps, that was corrected in the following way.

The data were divided in variable-size bins of the inverse of the amplitude containing at least 200 entries. For each of these bins for DUT0 in figure 12 left, the most probable value of TOA0-TOA1 was obtained by a Gaussian fit (red points in the figure). That value was associated to the average value of the inverse of the DUT0 amplitude distribution within that bin (instead than to the center of the bin). An event-by-event correction was then applied to the inverse of the amplitude of the signal in DUT0, using the value provided by the linear interpolation (red segments in the figure) of the two adjacent time-walk correction points. Once DUT0 was time-walk corrected in this way, the entire

procedure was repeated for DUT1 (shown in figure 12 right) to complete the time-walk correction.[3]

Extraction of the time resolution. Once data were corrected for time walk, Gaussian fits were performed to the TOA0-TOA1 distributions, including only bins containing more than 25% of the entries at the maximum of the distribution. It was then assumed that the two DUTs have the same resolution, so that the time resolution of each DUT can be estimated as $\sigma_t = \sigma_{\text{TOA0-TOA1}}/\sqrt{2}$.

As an example, figure 13 shows the resulting TOA difference distribution after time-walk correction for the data acquired at the working points 150 µA and HV = 160 V (left) and 7 µA and 120 V (right). In the case of the former, that is the best working point for time resolution, the standard deviation obtained by the Gaussian fit is measured to be $\sigma_{\text{TOA0-TOA1}} = (51.4 \pm 1.1)$ ps. Therefore the time resolution of each DUT is estimated to be

$$\sigma_t = \frac{\sigma_{\text{TOA0-TOA1}}}{\sqrt{2}} = (36.4 \pm 0.8)\ \text{ps}. \tag{4.1}$$

The fraction of events exceeding the Gaussian fit in the tails of the distribution of figure 13 is approximately 5%. This fraction of events represents the typical non-Gaussian component found in the tails of the time-resolution distribution for all the data sets acquired at the testbeam at different sensor and preamplifier bias. As a consequence the resolutions quoted in the following refer to 95% of the signals acquired by the DUTs.

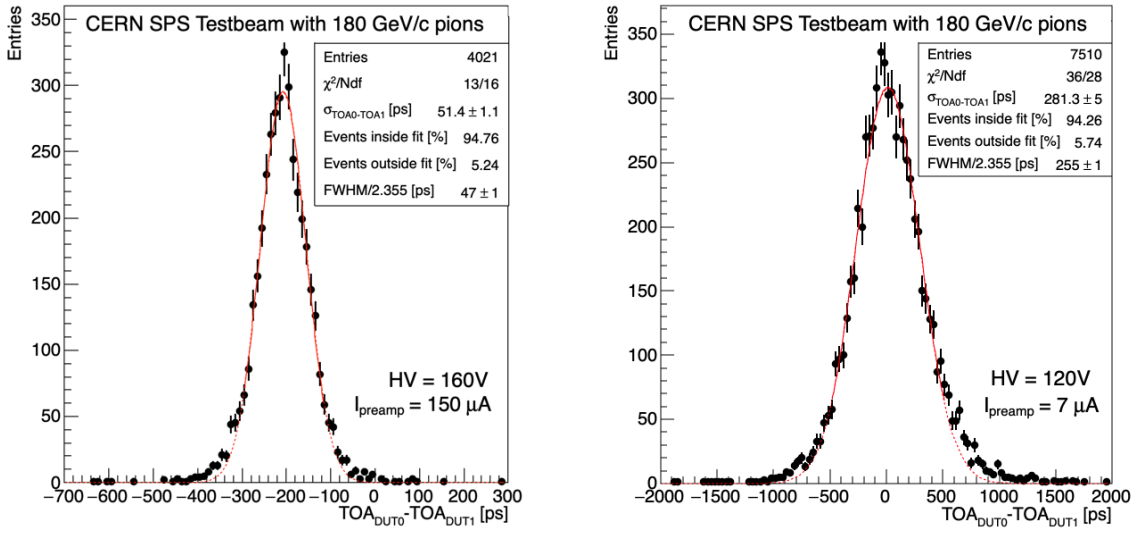

Figure 13. TOA difference between pixels OA0 of DUT0 and DUT1 after time-walk correction for the two working points reported in the panels. A constant arbitrary offset is present, which is irrelevant for the time-resolution calculation. The red lines show the results of the Gaussian fit using only the bins with more than 25% of the entries in the maximum of the distribution. The full red lines show the ranges used for the fits, while the dashed red lines allow the estimation of the non-Gaussian components in the tails.

[3]Given its importance for this measurement, the time-walk correction was performed also with an unbinned maximum-likelihood fit. This second method was used for a simultaneous extraction of the resolution parameter $\sigma_{\text{TOA0-TOA1}}$ and of the two time-walk correction functions for DUT0 and DUT1. For all the data samples analysed, the results were within few percent from those obtained by the method described in the text.

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Figure 14 top shows the time resolution as a function of the HV for the highest power consumption working point $I_{\text{preamp}} = 150\,\mu\text{A}$. The time resolution varies between 60 and 36 ps with the HV between 80 and 160 V. At HV = 120 V the timing performance is approximately 20% worse than the one measured at 160 V.

Figure 14 bottom shows the time resolution measured at $HV = 120\,\text{V}$ for the four I_{preamp} working points. As expected, the time resolution depends on the preamplifier current. A significant degradation of the performance is observed for the lowest power-consumption working point studied $I_{\text{preamp}} = 7\,\mu\text{A}$, for which the time resolution still remains at the level of 200 ps.

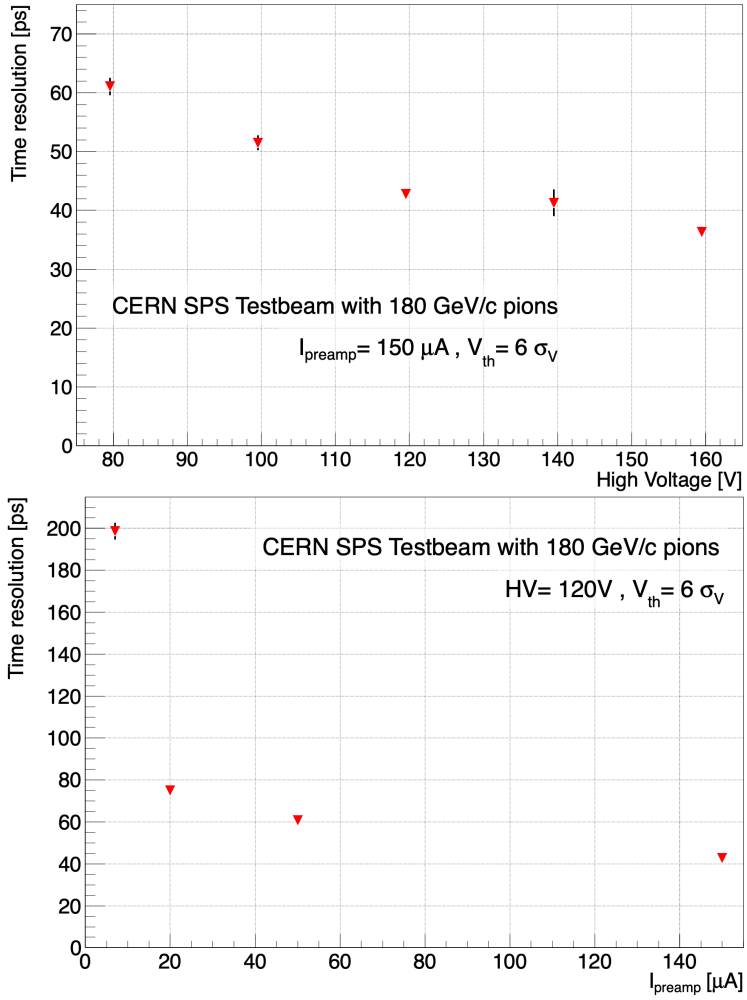

Figure 14. Top: time resolution as a function of sensor bias voltage at $I_{\text{preamp}} = 150\,\mu\text{A}$. Bottom: time resolution as a function of I_{preamp} for sensor bias voltage $HV = 120\,V$. The time resolution is defined as $(\sigma_{\text{TOA0-TOA1}})/\sqrt{2}$. It refers to the Gaussian component of the data, which is approximately 95% of the total.

5 Conclusions

A monolithic silicon detector prototype with 100 µm pixel pitch was produced in 130 nm SiGe BiCMOS technology on 50 Ω cm wafers and tested at a beamline with minimum-ionizing particles.

The analysis of the data acquired with analog channels using a threshold of 6 σ_V shows that this detector technology can achieve efficiencies up to 99.9%. This result proves that the low ENC reachable with SiGe HBTs allows operating at very high efficiency even with a thin depletion layer of approximately 20 µm. The small drop in efficiency observed at the lowest amplifier current studied, caused by an increase of the ENC, could be compensated by increasing the sensor depletion depth. Therefore, further optimization of this detector technology is possible by adopting higher resistivity substrates to obtain full depletion of the sensitive volume.

Results with a previous prototype [12] that provided uniquely the TOT measurement to perform the time-walk correction, showed that a remarkable timing performance at the level of 50 ps was possible only at large discrimination threshold, therefore compromising the detection efficiency. The data presented here demonstrate that a time-walk correction that uses the signal amplitude instead of the TOT can provide an even better timing performance at the lowest discrimination threshold permitted by the ENC of the amplifier: when operated at a preamplifier current as low as 20 µA the SiGe HBT amplifier implemented in the ASIC provides a time resolution better than 100 ps and an efficiency of 99.6%; at a preamplifier current of 150 µA a time resolution of 36 ps and an efficiency of 99.9% are measured, even without the support of an avalanche gain layer to boost the signal-to-noise ratio. These results prove that this technology is suitable for applications that require the combination of tracking capabilities with excellent time resolution.

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