A 206–220-GHz Compact Fundamental Oscillator With up to 7-dBm Output Power and 7.4% Peak DC-to-RF Efficiency in a 130-nm SiGe Technology

Arjith Chandra Prabhu, *Graduate Student Member, IEEE*, Janusz Grzyb, Marcel Andree, *Member, IEEE*, Holger Rücker, and Ullrich R. Pfeiffer, *Fellow, IEEE*

***Abstract*— This letter presents a 206.5–220.5-GHz fundamental differential Colpitts oscillator in a cascode topology implemented in a 130-nm SiGe HBT technology with $f_t/f_{\max}$ of 350/450 GHz. Base inductors at the common-base (CB) stages are used to provide an inductive load at the output of the common-emitter (CE) stage, hence, boosting the output power by 27%. The resonant tank is embedded straight on top of the devices, reducing layout parasitics and resulting in a compact and efficient oscillator core layout. The oscillator provides a peak output power of 7 dBm at 208 GHz, 7.4% peak dc-to-RF efficiency at 220 GHz, and 6.55% tuning range (TR). At peak efficiency, the oscillator delivers an output power of 5.7 dBm with 50-mW dc power consumption and a phase noise (PN) of −90.2/−110 dBc/Hz at 1-/10-MHz offset, respectively. To the best of the authors' knowledge, the presented oscillator has the best PN figure-of-merit (FoM) of −182.1 dBc/Hz at 1-MHz offset in a SiGe/CMOS technology above 200 GHz. It occupies a total area of 0.086 mm^2, including the RF pad, and an ultracompact core size of 0.0049 mm^2.**

***Index Terms*— Colpitts, dc-to-RF efficiency, frequency generators, fundamental oscillator, mm-Wave, output power, phase noise (PN), PN figure-of-merit (FoM), power boosting, SiGe, ultracompact.**

I. Introduction

FREQUENCY generators at mm-Wave frequencies play a crucial role in high data-rate wireless communication [1], [2], [3], radar systems [4], [5], [6], high-resolution terahertz (THz) imaging systems [7], [8], and spectroscopy [9], [10]. In coherent systems applied in laser holography [11] and high-resolution radar imaging [5], [12], not only amplitude but also phase information are extracted, allowing distance measurements with an accuracy in the μm range [13]. Extracting accurate phase information typically requires locked sources based on a phase-locked loop (PLL) feedback system. However, implementing a PLL at frequencies beyond 200-GHz poses a challenge due to the lack of frequency dividers at these frequencies. Another approach for signal locking is based on the injection locking method [14], [15], [16], [17] which tends to be area-consuming or inefficient. An alternative approach for high-resolution 3-D imaging is based on light-field ray-tracing [18] utilizing multipixel focal plane arrays (FPAs) of incoherent sources resulting in a compact and efficient imaging system.

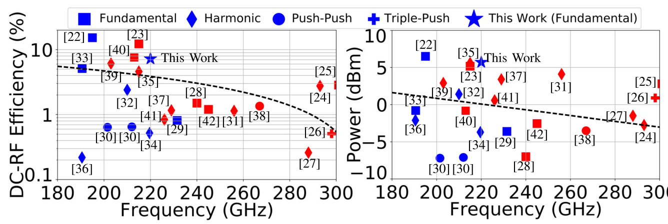

Fig. 1. Comparison of SOTA efficiency and output power of oscillators in SiGe (blue) and CMOS (red) technologies operating from 180 to 300 GHz.

High power frequency sources beyond $f_{\max}/2$ become challenging due to the transistor degraded performance and increased back-end losses. Typically, such sources are implemented using an oscillator at lower frequencies followed by a frequency multiplier chain [19], [20], [21]. Here, peak output powers of 9.6 dBm at 270 GHz occupying an area of 0.92 mm^2 with 1.38% efficiency [19] and 8 dBm at 240 GHz occupying an area of 0.28 mm^2 with 1.47% efficiency [21] are reported. Nevertheless, due to the high area and low efficiency, such multiplier chains are unsuitable as sources in large-scale FPAs for THz light-field applications. A good alternative is different oscillator topologies, subdivided into harmonic, push–push/triple-push, and fundamental oscillators that are generally compact and efficient at the cost of output power. In more detail, an efficiency of up to 15.3% and 6.5-dBm output power at 195 GHz [22] that drops to 12.3% with 5.17-dBm output power at 215 GHz [23], 2.76% with −2.74-dBm output power at 293 GHz [24] are reported, while in [25] a 301-GHz push–push oscillator [26] with an efficiency of 2.8% and 2.85-dBm output power is presented. The corresponding state-of-the-art (SOTA) trend in dc-to-RF efficiency and output power of oscillators in SiGe and CMOS technologies beyond 200 GHz is shown in Fig. 1.

This letter presents an efficient and compact 206–220-GHz fundamental differential Colpitts oscillator in a 130-nm SiGe HBT technology, which utilizes a 10 pH base inductor to boost the output power by 27% by providing an inductive load to the output of the common-emitter (CE) device. The innovative layout reduces the parasitic effects by implementing the resonant inductor and capacitor directly above the transistors resulting in a compact oscillator core. The oscillator delivers the highest

Received 31 January 2025; accepted 19 February 2025. Date of publication 10 March 2025; date of current version 9 May 2025. This work was supported by the European Research Council (ERC) through the European Union's Horizon 2020 Research and Innovation Programme under Grant 101019972. *(Corresponding author: Arjith Chandra Prabhu.)*

Arjith Chandra Prabhu, Janusz Grzyb, Marcel Andree, and Ullrich R. Pfeiffer are with the Institute of High-Frequency and Communication Technology, University of Wuppertal, 42119 Wuppertal, Germany (e-mail: chandra@uni-wuppertal.de).

Holger Rücker is with the IHP—Leibniz-Institut für Innovative Mikroelektronik, 15236 Frankfurt (Oder), Germany.

Digital Object Identifier 10.1109/LMWT.2025.3546162

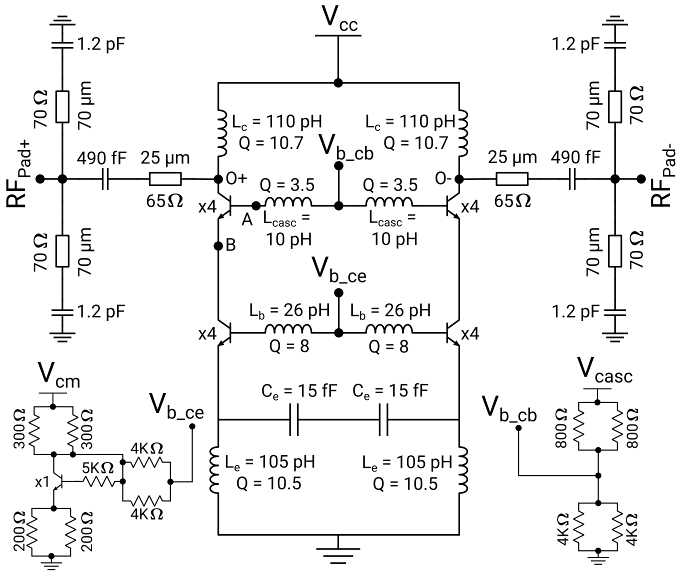

Fig. 2. Schematic of the ×4 ($A_e = 4 \times 0.07\ \mu$m $\times$ 0.9 μm) fundamental differential Colpitts oscillator with output matching and biasing networks.

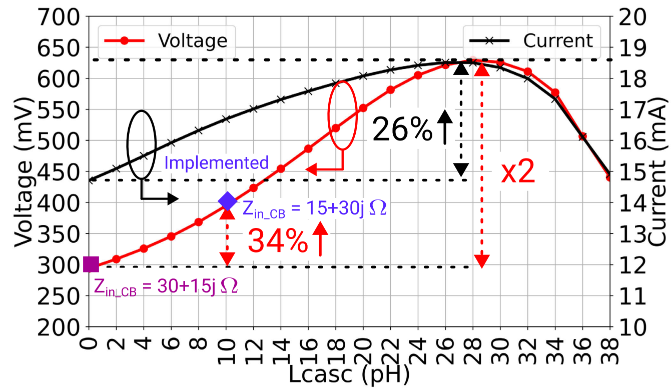

Fig. 3. Ideal core large signal simulation of the magnitude of 220-GHz fundamental voltage (left) and current (right) swing at the input of CB device (across nodes AB) for a varying L_{casc}.

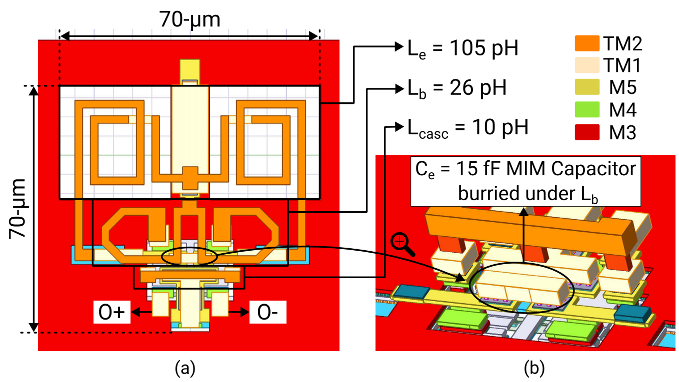

Fig. 4. (a) 3-D EM model of the compact 70 × 70 μm oscillator core with the resonance inductors implemented on TM2. (b) Closed-up highlighting MIM capacitors implemented on Metal5 (M5) and TM1 buried under inductor L_b.

output power compared to the SOTA above 200 GHz with values up to 7 dBm, a maximum peak efficiency of 7.4%, and occupies a total area of 0.086 mm^2. The corresponding efficiency and power are well above the trend line shown in Fig. 1.

II. Circuit Design

The fundamental oscillator is designed in a 130-nm SiGe BiCMOS HBT technology with a f_t/f_{max} of 350/450 GHz offering a 12-μm-thick seven-metal aluminum back-end with two thick top-metal layers [43] and complying to the standard DRC rules of the technology. All inductors and transmission lines (TLs) have been implemented on the 3-μm Top-Metal2 (TM2) layer with Metal3 as the ground plane. The schematic of the fundamental oscillator is shown in Fig. 2 consisting of an x4 ($A_e = 4 \times 0.07\ \mu$m $\times$ 0.9 μm) differential CE Colpitts topology followed by a common-base (CB) stage to provide isolation. The bases of the CE and CB devices are biased using current mirror and voltage divider circuits, respectively. The Colpitts oscillator, including RF pads, is full wave 3-D electromagentic (EM) simulated with parasitic interconnects in Ansys HFSS.

A. Oscillator Core

A load–pull simulation was used to analyze the output of the CE stage, resulting in an impedance of $15 + 30j\ \Omega$ to enhance the fundamental voltage and current swings. To achieve this, the L_{casc} inductor was used to transform the input impedance of the CB stage $Z_{\text{in\_CB}}$ from $30 + 15j\ \Omega$ to $15 + 30j\ \Omega$ thereby maximizing the voltage and current swings as shown in Fig. 3. As the oscillation frequency decreases with increasing L_{casc}, both C_e and L_b are adapted to maintain a constant frequency of 220 GHz. Although an L_{casc} of 28 pH improves the current swing by 26% and doubles the voltage swing, a 10-pH inductor was implemented to ensure a compact oscillator core size of 70 × 70 μm and provide the required load impedance of $15 + 30j\ \Omega$ at the output of the CE device, and improve the voltage and current swing by 34% and 14%, respectively.

The 3-D EM model of the 70 × 70 μm compact oscillator core is shown in Fig. 4 consisting of symmetrical differential inductors L_b, L_e, and L_{casc}. The emitter inductor L_e, extracted from EM simulations, has a differential inductance of 210 pH achieving a self-resonance frequency (SRF) of 338 GHz. The ground under L_e is removed to improve the inductance and quality factor. The differential resonant tank inductor L_b is implemented directly above the differential CE transistors having a value of 26 pH, and an SRF of 447 GHz. A 15-fF resonant tank MIM capacitors C_e are buried under L_b as shown in Fig. 4. The complete EM simulated oscillator core, including output matching and the 10-pH L_{casc}, shows 30% improvement in voltage swing and 27% improvement in output power compared with the core without L_{casc}.

B. Output Matching

An optimal differential impedance Z_{opt} of $50 + 65j\ \Omega$ after modeling the interconnects up to Top-Metal1 (TM1) at the oscillator's output was found through load–pull providing an ideal output power of 7.8 dBm with a shift in oscillation frequency to 217 GHz. The outputs have been separated into two single-ended configurations instead of a balun to reduce further losses, frequency detuning, and maintain compactness. The output matching consists of a differential 220-pH shunt inductor L_c with 318.7-GHz SRF. A 25-μm-long, 65-Ω symmetrical series TLs, and two 70-μm-long, 70-Ω shunt lines along with the RF pads are implemented on each side along with large 490-fF dc blocking series capacitors to realize an impedance of $42 + 66j\ \Omega$ close to Z_{opt}.

TABLE I
PERFORMANCE COMPARISON OF FUNDAMENTAL OSCILLATORS IN SILICON-BASED TECHNOLOGY

Ref	Tech	Type	Freq (GHz)	P_{out} (dBm)	Efficiency (%)	TR (%)	P_{dc} (mW)	PN @ 1 MHz offset (dBc/Hz)	FoM (dBc/Hz)	Area (mm^2)
[22]	55nm SiGe	Fundamental	195	6.5	15.3	1.1	29	-98.6	-177.1	0.1517 (Chip)
[32]	130nm SiGe	Harmonic	210	1.4	2.4	10.6	57.5	-87.5	-178.2	0.08 (Chip) 0.027 (Core)
[33]	130nm SiGe	Fundamental	190.6	-0.8	5.1	6.4	16.2	-67[1]	-155.8	0.231 (Chip)
[34]	55nm SiGe	Fundamental	219.6	-3.7*	0.52	28.3	82.1	-	-161.9	0.31 (Chip)
[29]	SiGe BiCMOS	Fundamental	218-245	-3.6	0.81	11.66	54	-98[2]	-165.65	-
[23]	65nm CMOS	Fundamental	215	5.17	12.3	1.1	26.64	-90	-168.4	0.0806 (Chip)
[40]	65nm CMOS	Fundamental	213	-0.83	7.6	0.98	10.82	-93.7	-169	0.0675 (Chip) 0.0179 (Core)
This Work	**130nm SiGe**	**Fundamental**	**220**	**5.7/7[3]**	**7.4/5[3]**	**6.55**	**50/101[3]**	**-90.2**	**-182.1**	**0.086 (Chip) 0.0049 (Core)**

TR : Tuning Range, * Radiated Power, [1] Estimated from plot, [2] PN @10 MHz offset, [3] Measured @ 208 GHz
$FoM = PN - 20 \cdot log_{10}((f_0/\Delta f) \cdot (TR/10)) + 10 \cdot log_{10}(P_{DC}/1mW) - P_{out}[dBm]$ [32]

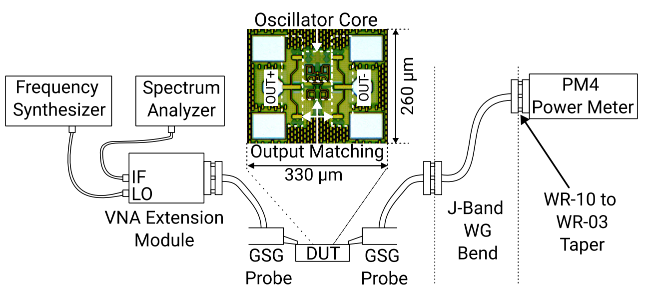

Fig. 5. Measurement setup and chip micrograph of the fundamental differential Colpitts oscillator.

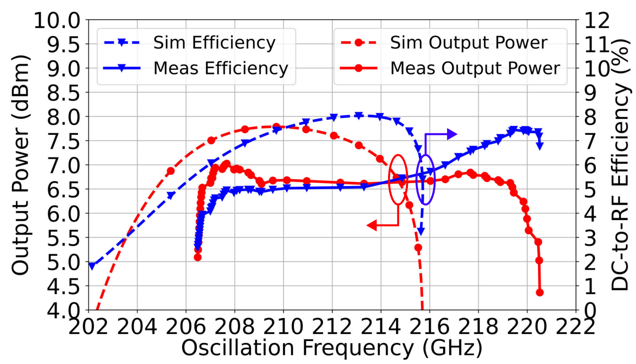

Fig. 6. Measured and simulated differential output power (left) and dc-to-RF efficiency (right) across the TR of 220.5–206.5 GHz and operated at V_{cc}/V_{casc} of 3.5/3.2 V.

III. MEASUREMENT RESULTS

Fig. 5 shows the measurement setup, including the chip micrograph. The two single-ended outputs enable simultaneous frequency and power measurement with 50-Ω termination on each side using a J-band WR-03 vector network analyzer (VNA) extension module connected to an E44404 spectrum analyzer from Agilent and a VDI-Erickson PM4 power meter with WR-03 to WR-10 taper. All relevant losses, such as probe/waveguide losses and conversion gain (CG) of the VNA extension modules, were calibrated and de-embedded. The oscillator is operated at a nominal collector (V_{cc}) and CB base (V_{casc}) bias of 3.5 and 3.2 V, respectively. Fig. 6 presents the measured output power and efficiency across a tuning range (TR) of 206.5–220.5 GHz, demonstrating excellent agreement with the simulated results, with an oscillation frequency variation of <2%. Fig. 7 shows the downconverted output spectrum at 210.7 MHz with a peak of −16.5 dBm and the corresponding PN of −90.2/−110 dBc/Hz and PN

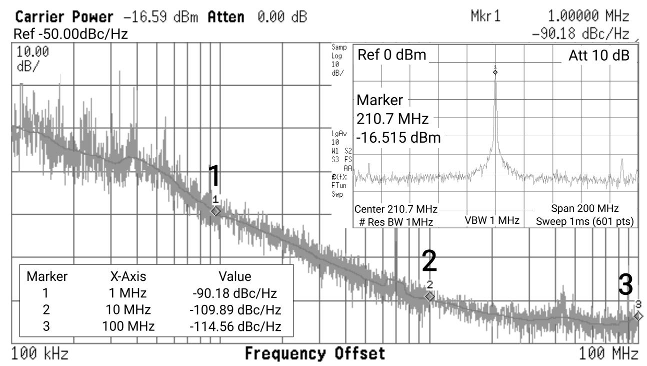

Fig. 7. Measured PN and spectrum of the oscillator operating at 220-GHz biased at $V_{cc}/V_{casc}/V_{cm}$ of 3.5/3.2/1.06 V.

figure-of-merit (FoM) of −182/−181 dBc/Hz at 1-/10-MHz offset, respectively. At 220 GHz, the oscillator has an output power of 5.7 dBm, dc-to-RF efficiency of 7.4%, and dc power consumption of 50 mW.

IV. CONCLUSION

In this work, an efficient 206.5–220.5-GHz fundamental Colpitts oscillator implemented in a 130-nm SiGe HBT technology with a peak output power of 7 dBm around 208 GHz and peak dc-to-RF efficiency of 7.4% at 220 GHz is reported. The implemented 10-pH inductance at the CB device provides an inductive load to the CE device and boosts the output power by 27%. This design has the best PN FoM of −182/−181 dBc/Hz at 1-/10-MHz offset as compared to the SOTA for silicon-based oscillators above 200 GHz presented in Table I. Therefore, based on its ultracompact 0.0049 mm^2 core size, the presented oscillator is suitable for large-scale source arrays for high-resolution THz light-field imaging.

REFERENCES

[1] P. Rodríguez-Vázquez, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "A 16-QAM 100-Gb/s 1-M wireless link with an EVM of 17% at 230 GHz in an SiGe technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 4, pp. 297–299, Apr. 2019.

[2] I. Kallfass et al., "MMIC chipset for 300 GHz indoor wireless communication," in *Proc. IEEE Int. Conf. Microw., Commun., Antennas Electron. Syst. (COMCAS)*, Nov. 2015, pp. 1–4.

[3] J. Park, S. Kang, S. V. Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," in *Proc. Symp. VLSI Circuits (VLSIC)*, Jun. 2012, pp. 48–49.

[4] J. Grzyb, K. Statnikov, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 210–270-GHz circularly polarized FMCW radar with a single-lens-coupled SiGe HBT chip," *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 6, pp. 771–783, Nov. 2016.

[5] A. Mostajeran, A. Cathelin, and E. Afshari, "A 170-GHz fully integrated single-chip FMCW imaging radar with 3-D imaging capability," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2721–2734, Oct. 2017.

[6] S. Hansen, C. Bredendiek, G. Briese, A. Froehly, R. Herschel, and N. Pohl, "A SiGe-chip-based D-band FMCW-radar sensor with 53-GHz tuning range for high resolution measurements in industrial applications," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 1, pp. 719–731, Jan. 2022.

[7] R. Jain, P. Hillger, E. Ashna, J. Grzyb, and U. R. Pfeiffer, "A 64-pixel 0.42-THz source SoC with spatial modulation diversity for computational imaging," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3281–3293, Dec. 2020.

[8] U. R. Pfeiffer and A. Kutaish, "Terahertz light-field imaging with silicon technologies," *IEEE Open J. Solid-State Circuits Soc.*, vol. 4, pp. 1–11, 2024.

[9] M. W. Mansha, T. E. Rice, M. A. Oehlschlaeger, I. Wilke, and M. M. Hella, "A 220–300 GHz twin-FET detector for rotational spectroscopy of gas mixtures," *IEEE Sensors J.*, vol. 21, no. 4, pp. 4553–4562, Oct. 2020.

[10] K. Schmalz et al., "Dual-band transmitter and receiver with bowtie-antenna in 0.13 μm SiGe BiCMOS for gas spectroscopy at 222–270 GHz," *IEEE Access*, vol. 9, pp. 124805–124816, 2021.

[11] R. Collier, *Optical Holography*. Amsterdam, The Netherlands: Elsevier, 2013.

[12] S. Thomas, C. Bredendiek, and N. Pohl, "A SiGe-based 240-GHz FMCW radar system for high-resolution measurements," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 11, pp. 4599–4609, Nov. 2019.

[13] L. Piotrowsky, S. Kueppers, T. Jaeschke, and N. Pohl, "Distance measurement using mmWave radar: Micron accuracy at medium range," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 11, pp. 5259–5270, Nov. 2022.

[14] S. Li, D. Fritsche, C. Carta, and F. Ellinger, "A 200-GHz sub-harmonic injection-locked oscillator with 0-dBm output power and 3.5% DC-to-RF-efficiency," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 212–215.

[15] Z. Peng, J. Chen, H. Wang, L. Zhang, W. Hong, and X. Liu, "A 208-GHz injection locking doubler chain with 3.2% PAE and 2.9-mW output power in CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 4, pp. 351–354, Apr. 2022.

[16] X. Liu and H. C. Luong, "A 170-GHz 23.7% tuning-range CMOS injection-locked LO generator with third-harmonic enhancement," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2668–2678, Jul. 2020.

[17] A. Siligaris et al., "A 270-to-300 GHz sub-harmonic injection locked oscillator for frequency synthesis in sub-mmW systems," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 4, pp. 259–261, Apr. 2015.

[18] P. Hillger et al., "Toward mobile integrated electronic systems at THz frequencies," *J. Infrared, Millimeter, THz Waves*, vol. 41, no. 7, pp. 846–869, Jun. 2020.

[19] A. C. Prabhu, J. Grzyb, P. Hillger, T. Bücher, H. Rücker, and U. Pfeiffer, "A 300 GHz x9 multiplier chain with 9.6 dBm output power in 0.13-μm SiGe technology," in *Proc. IEEE 24th Top. Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, Jan. 2024, pp. 37–40.

[20] Z. Li, J. Chen, D. Tang, R. Zhou, and W. Hong, "A 205–273-GHz frequency multiplier chain ($\times 6$) with 9-dBm output power and 1.92% DC-to-RF efficiency in 0.13-μm SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 7, pp. 2909–2919, Jul. 2023.

[21] E. Turkmen, I. K. Aksoyak, W. Debski, W. Winkler, and A. Ç. Ulusoy, "A 220–261 GHz frequency multiplier chain ($\times$ 18) with 8-dBm peak output power in 130-nm SiGe," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 7, pp. 895–898, Jul. 2022.

[22] H. Khatibi, S. Khiyabani, A. Cathelin, and E. Afshari, "A 195 GHz single-transistor fundamental VCO with 15.3% DC-to-RF efficiency, 4.5 mW output power, phase noise FoM of -197 dBc/Hz and 1.1% tuning range in a 55 nm SiGe process," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 152–155.

[23] H. Wang, J. Chen, L. Zhang, and X. Liu, "High-efficiency millimeter-wave CMOS oscillator design using port voltage/current optimization and T-embedding networks," *IEEE Trans. THz Sci. Technol.*, vol. 12, no. 6, pp. 550–564, Nov. 2022.

[24] S. Jameson and E. Socher, "High efficiency 293 GHz radiating source in 65 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 7, pp. 463–465, Jul. 2014.

[25] Z. Peng, J. Chen, H. Wang, L. Zhang, W. Hong, and X. Liu, "A 300 GHz push-push coupling VCO employing T-embedded network in CMOS technology," *IEEE Trans. THz Sci. Technol.*, vol. 12, no. 4, pp. 426–429, Jul. 2022.

[26] A. H. M. Shirazi, A. Nikpaik, S. Mirabbasi, and S. Shekhar, "A quad-core-coupled triple-push 295-to-301 GHz source with 1.25 mW peak output power in 65nm CMOS using slow-wave effect," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 190–193.

[27] J. Grzyb, Y. Zhao, and U. R. Pfeiffer, "A 288-GHz lens-integrated balanced triple-push source in a 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1751–1761, Jul. 2013.

[28] N. Landsberg and E. Socher, "240 GHz and 272 GHz fundamental VCOs using 32 nm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4461–4471, Dec. 2013.

[29] S. P. Voinigescu et al., "A study of SiGe HBT signal sources in the 220–330-GHz range," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2011–2021, Sep. 2013.

[30] P.-Y. Chiang, O. Momeni, and P. Heydari, "A 200-GHz inductively tuned VCO with -7-dBm output power in 130-nm SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3666–3673, Oct. 2013.

[31] M. Adnan and E. Afshari, "14.8 a 247-to-263.5GHz VCO with 2.6 mW peak output power and 1.14% DC-to-RF efficiency in 65nm bulk CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2014, pp. 262–263.

[32] C. Jiang, A. Cathelin, and E. Afshari, "An efficient 210GHz compact harmonic oscillator with 1.4dBm peak output power and 10.6% tuning range in 130nm BiCMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 194–197.

[33] D. Fritsche, S. Li, N. Joram, C. Carta, and F. Ellinger, "Design and characterization of a 190-GHz voltage-controlled oscillator," in *Proc. 46th Eur. Microw. Conf. (EuMC)*, Oct. 2016, pp. 493–496.

[34] A. Mostajeran and E. Afshari, "An ultra-wideband harmonic radiator with a tuning range of 62GHz (28.3%) at 220GHz," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 164–167.

[35] R. Kananizadeh and O. Momeni, "High-power and high-efficiency millimeter-wave harmonic oscillator design, exploiting harmonic positive feedback in CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 10, pp. 3922–3936, Oct. 2017.

[36] R. Kananizadeh and O. Momeni, "A 190-GHz VCO with 20.7% tuning range employing an active mode switching block in a 130 nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2094–2104, Aug. 2017.

[37] H. Jalili and O. Momeni, "A 230-GHz high-power and wideband coupled standing wave VCO in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 547–556, Mar. 2020.

[38] S. K. Nath, J. Yoo, J.-S. Rieh, and D. Yoon, "A 253–280 GHz wide tuning range VCO with -3.5 dBm peak output power in 40-nm CMOS," in *Proc. IEEE 47th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2021, pp. 299–302.

[39] A. Ghorbani-Nejad, A. Nikpaik, A. Nabavi, A. H. M. Shirazi, S. Mirabbasi, and S. Shekhar, "Optimum conditions for efficient second-harmonic power generation in mm-wave harmonic oscillators," *IEEE J. Solid-State Circuits*, vol. 57, no. 7, pp. 2130–2142, Jul. 2022.

[40] H. Wang, J. Chen, J. T. S. Do, H. Rashtian, and X. Liu, "High-efficiency millimeter-wave single-ended and differential fundamental oscillators in CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2151–2163, Aug. 2018.

[41] Y. Liang, Q. Chen, X. Wu, X. Fan, and L. Li, "A 226 GHz coupled harmonic VCO with 9.34% tuning range utilizing three-coil transformer with switched inductor in 65nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2023, pp. 1–3.

[42] A. Qahir, D. R. Utomo, B. Yun, K. S. Choi, D. W. Park, and S. G. Lee, "High-power 150/245-GHz fundamental oscillators with 12.1/− 2.54-dBm peak output power for phased array transceivers," *IEEE J. Solid-State Circuits*, vol. 59, no. 11, pp. 3683–3693, Nov. 2024.

[43] H. Rücker, B. Heinemann, and A. Fox, "Half-terahertz SiGe BiCMOS technology," in *Proc. 12th Top. Meeting Silicon Monolithic Integr. Circuits RF Syst.*, Jan. 2012, pp. 133–136.