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A Fully Integrated 0.48 THz FMCW Radar Sensor in a SiGe Technology

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ABSTRACT The THz gap has been a significant research objective for photonics and electronics for decades. This work introduces a fully integrated frequency modulated continuous wave (FMCW) radar sensor with a center frequency of 0.48 THz, realized in a silicon-germanium (SiGe) technology. The sensor consists of a THz MMIC integrated onto a front-end printed circuit board (PCB) with FR4 substrate used for frequency synthesis and IF signal amplification. A dielectric polytetrafluoroethylene (PTFE) lens is mounted above the MMIC to act as transmitter (Tx) and receiver (Rx) lens as well as a physical protection for the bond wires of the MMIC. A back-end PCB generates the supply voltages and control signals, and its analog-digital-converter (ADC) samples the IF signal. The whole sensor is just 4.9 cm by 4.3 cm in size and is cost-efficient due to its design with FR4 PCBs. The MMIC reaches an output power of up to −9 dBm. In FMCW operation with the full sensor, a tuning range of 49 GHz is reached along an equivalent isotropic radiated power (EIRP) of up to 22 dBm. Distance measurements were successfully tested for distances of up to 5 m, and a radiation pattern is presented. In summary, this article demonstrates the potential of SiGe technology in the THz range for applications like localization, material characterization, and communication.

INDEX TERMS BiCMOS, dielectric lens, differential, distance measurement, FMCW, frequency divider, frequency doubler, frequency-modulated continuous wave (FMCW), frequency synthesis, MMIC, mixer, power amplifier, radar, receiver, sensor SiGe, system, THz, THz-radar, voltage-controlled oscillator.

I. INTRODUCTION

In recent years, extensive research has been carried out in the THz frequency range, mainly defined as 300 GHz $< f <$ 10 THz. Several technological approaches are used to close the THz gap that forms between state-of-the-art electronic silicon and III/V technologies on the lower end and optical systems on the upper edge of the frequency band. Focussing on the electronic approaches, there have been several demonstrations of first THz systems reaching frequencies as high as 500 GHz using silicon technologies [1], [2], [3], [4] and advanced indium phosphide (InP) resonant tunneling diode (RTD) technology [5]. These systems enable localization, material characterization [6], and also THz communication [7], [8]. Another emerging application is insect and plant monitoring [9], where THz frequencies are expected to be beneficial, e.g., in the radar-cross section (RCS) of a target. A big advantage over optical systems is the possible compactness and mobility of a fully integrated radar transceiver, making operation in a mobile scenario powered by a USB power bank possible and opening various possible application scenarios.

The main drivers in THz systems are newly developed SiGe-technologies with f_T/f_{max} of up to 470/650GHz, which

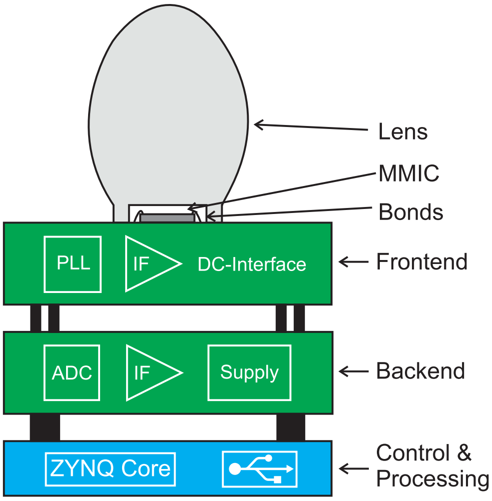

FIGURE 1. Concept diagram of the 0.48 THz sensor stack, consisting of two designed and stacked PCBs, a commercial control board with a Zynq SoC, a MMIC and a PTFE lens.

improves THz output power and efficiency. However, many challenges arise from this very high frequency, like the huge impact of parasitic elements, limited simulation model accuracy, and manufacturing tolerances having a considerable impact.

An advantage of an FMCW system operating at a high frequency is the higher absolute tuning range (TR), as frequency doubling of a fundamental voltage-controlled oscillator (VCO) signal also doubles the TR, resulting in a better range resolution. A drawback of high frequencies is the need for on-chip integrated antennas since off-chip transitions using wire bonds in the THz range become very lossy [10], reducing the THz output power significantly. Therefore, integrated antenna solutions are preferred.

This article presents a fully integrated FMCW radar sensor operating at 0.48 THz. This sensor features a SiGe MMIC, including all the RF components, a low-cost FR4 front-end PCB for phased-locked loop (PLL) components and the first intermediate frequency (IF) amplifier, a back-end PCB with the power supply, additional IF amplifiers, and an ADC, as well as a processing PCB with a Xilinx Zynq core, managing the PLL and ADC as well as the communication with external devices like a PC. To collimate the radiated power, a PTFE lens is directly mounted onto the front-end PCB and 350 μm above the MMIC, which also acts as physical protection of the wire bonds.

This work is based on a transceiver MMIC, developed in IHP's SG13G3 technology with copper back-end of line (BEOL). It uses a similar circuit topology as in [11], which uses the SG13G3 technology with aluminum BEOL. The MMIC is a new design based on the same architecture and system concept. Since the BEOL has been fully changed, all passive structures, including metal contacts, transmission lines, and capacitors, have been newly developed. These components are one of the biggest challenges within a design at 0.48 THz, since the influence of parasitic elements is very

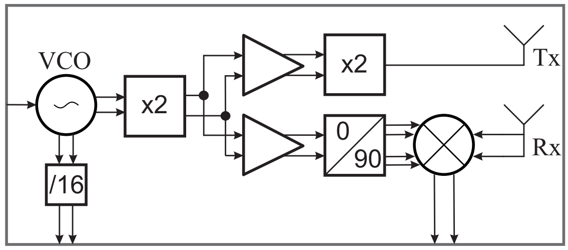

FIGURE 2. Block diagram of the 480 GHz FMCW transceiver MMIC. All RF components are integrated in the MMIC. Therefore, only a dc connection is needed along with the divider output and the Rx mixer output at the MMIC to PCB interface.

high. However, the deliberate redesign and 3D EM simulation of passive elements result in better circuit performance, which ultimately doubles the output power of the sensor itself compared to [11]. A full sensor is developed based on cost-efficient PCBs to present a fully integrated FMCW radar sensor at 0.48 THz. Additionally, sensor verification measurements like FMCW distance, EIRP, and pattern measurements are evaluated. These measurements are a vital part in the verification of the whole system concept including it's packaging and lens integration due to the challenges of the THz frequency range. Further details can be found in the respective sections.

The article is organized as follows: Section II explains the system concept and details the SiGe circuits, which were fabricated using IHP SG13G3Cu technology. The design of the front-end and back-end is detailed in Section III. In Section IV, the experimental results are presented, which are compared to the state-of-the-art in Section V. A summary of the paper is outlined in Section VI.

II. SYSTEM CONCEPT AND THZ MMIC

The sensor uses a modular architecture and consists of a front-end, a back-end, a lens, and the MMIC itself. The goal is to use only a USB connection for both a data connection to a computer and the sensor's entire power supply. A visualization of the sensor concept is given in Fig. 1. A quasi-monostatic transceiver concept is chosen for this work, where both the Tx and Rx antenna are located very close to each other but are still separated despite possible Tx-Rx leakage. For a true monostatic concept, a directional coupler would be necessary, introducing an additional insecurity, which is why we decided against it. Each system component is discussed in a respective section, beginning with the MMIC.

The FMCW radar MMIC contains all RF components needed for operating the FMCW radar system except for parts of the PLL, which are implemented with a commercial product. The design is carried out utilizing the new SiGe-BiCMOS technology SG13G3Cu by IHP [12], [13]. It features HBTs with a f_T/f_{max} of 470/650 GHz, together with 7 copper layers. A block diagram of the MMIC is given in Fig. 2. First, the signal generation in a VCO with a connected divide-by-16 static frequency divider is implemented. A subsequent frequency doubler is introduced to reach a higher center frequency and a larger tuning range. Afterward, the signal is split up into the Tx and Rx paths. The Tx channel further features a power amplifier (PA) to drive the subsequent final frequency doubler, ultimately providing the 0.48 THz transmit signal. The Rx channel also uses PAs identical to the Tx channel. The receiver concept utilizes an IQ-based subharmonic receive mixer, creating the need for an IQ branch-line coupler subsequent to the PA in the Rx path. Since the frequency is way too high to use off-chip antenna solutions connected with bond wires [10], both the transmit and receive antenna are integrated into the MMIC.

A. 120 GHZ VCO AND FREQUENCY DIVIDER

The VCO is based on the well-known Colpitts topology [14], [15], which was also used for the VCO's previous version developed in SG13G3(Al) [11]. Additionally, minor improvements were incorporated within the Cu version. To tune the frequency of the oscillator, tunable MOS-capacitors are used together with transmission lines (TLs) at the base of the oscillating transistors. To account for fabrication tolerances and simulation inaccuracy, laser fuses, which can be cut post-production, are included inside the base inductance, as well as the load and degeneration. The desired center frequency of the oscillator is around 120 GHz, so only two subsequent frequency doublers are needed to reach the final output frequency. The choice of the right VCO is a tradeoff. Lower VCO frequencies result in better phase noise performance but more unwanted harmonics. The desired frequency of 120 GHz results in unwanted harmonics with multiples of 120 GHz so that they are far enough out of the system operating frequency band, so the influence on the radar measurement is assumed to be negligible.

An on-chip frequency divider is introduced to enable frequency synthesis. Since the transistor's speed is very high, a static frequency divider is developed to also benchmark the SiGe Technology. Each divider stage consists of two latches in current mode logic (CML), resulting in a total division factor of 16 using four stages. The latches themselves are coupled with an emitter follower in emitter-coupled logic (ECL). This enhances the overall speed of the divider, resulting in a much higher than-needed maximum input frequency for this VCO, demonstrating the technologies' performance. For more insights into the divider design, refer to [16], where the original design in SG13G3Al, operative up to an input frequency of 163 GHz, was presented. Since the transistor performance remains constant for the copper and aluminum BEOL, no additional breakout MMIC was designed and measured. For this transceiver, the current scaling of the divider stages was further implemented to save energy, utilizing reduced current for each stage.

B. 240 GHZ FREQUENCY DOUBLER AND POWER AMPFLIFIER

Following the fundamental VCO, a frequency doubler is used to increase the center frequency of the generated signal from 120 to 240 GHz. Since the VCO has a differential circuit architecture, a doubler based on a Gilbert cell is chosen to maintain full differential operation in the subsequent Tx and Rx paths. The architecture of the doubler is a bootstrapped Gilbert cell doubler [17], omitting the need for 90° phase-shifted inputs since the inductance between the differential pair and the switching quad is used to shift the phase accordingly. Since the output frequency is as high as 240 GHz, all inductive elements are realized with transmission lines. The biggest limitation of the bandwidth using this architecture is the limited frequency range, where a DC offset at the output is avoided, and the internal phase difference at the two output nodes, which is sufficiently close to 180° for a certain range. For this system, however, this error is negligible within the VCO's tuning range.

Following the doubler, the signal is split into two paths: one for Tx and one for Rx. Since the doubler has a conversion loss in addition to the power divider loss (≥ 3 dB), amplification at 240 GHz is needed. Therefore, a power amplifier is implemented in both the Tx and Rx paths. For this purpose, a two-stage PA with cascaded differential amplifiers is chosen. Since the operating frequency is approx. at half the technologies f_T, reasonable gain (around 15 dB in simulations) can be achieved with this topology with good efficiency. The first stage of the PA is chosen to have a high gain but moderate output power, while the second stage is designed with a high saturated output power of up to 7 dBm and is driven into compression to ensure a minimal power variation across the whole tuning range. Accordingly, the first stage has a core current of around 15.7 mA, while the second stage requires 19 mA. The overall efficiency of up to 5% PAE (simulated) of the PAs is good, helping to balance the overall power consumption of the MMIC, given the fact that this PA design is used both in the Tx and Rx paths. Further details are outlined in [18] for the version of the MMIC in the previous SG13G3Al technology. Compared to this previous version, the load was further optimized together with the subsequent frequency doubler. Additionally, the transmission line between the PA and the doubler was improved, resulting in a higher power level at the doubler's input. The doubler greatly profits from a higher input power.

C. 480 GHZ FREQUENCY DOUBLER

A final frequency doubler is utilized in the transmit path to push the frequency of 240 GHz to the planned output frequency in the THz range. Opposing the first frequency doubler, this one is realized in a push-push topology. The reason is that the output frequency is above the transit frequency of the technology, and therefore, a Gilbert-Cell doubler was evaluated to have insufficient conversion gain, while a push-push topology can still achieve sufficient output power. The drawback of this circuit is that only a single-ended output signal is generated due to its internal architecture. However, the implementation of a single-ended on-chip patch antenna eliminates the disadvantages. Within the design phase, the influence of parasitic elements was closely monitored and evaluated. Compared to the previous version, a 3D-EM simulation of the inductive load was performed down to the lowest metal layer at the HBT contacts. Therefore, the load was optimized, internal matching of the doubler was improved, and together with the increased input power from the PA, the output power of the doubler was increased.

D. 480 GHZ SUB-HARMONIC RX MIXER

In a complete system, the receiver is of high importance since it contributes significantly to the SNR through its conversion gain and noise figure according to the Friis formula [19]. When operating the receiving down-conversion mixer above the transit frequency of a technology, its design becomes even more challenging. When using a typical Gilbert cell as circuit architecture, a high local oscillator (LO)-power is needed to enable acceptable performance, which is very difficult to achieve at THz frequencies in SiGe and requires significant hardware effort. To overcome this problem, a sub-harmonic mixer is utilized in this transceiver design. With this choice, only a 240 GHz LO signal is needed, which can be provided with high power due to its lower frequency compared to the signal at 480 GHz. In this concept, the frequency doubling of the LO signal to the same frequency as the RF signal is done internally by utilizing eight parallel transistors. The drawback of this concept is that differential IQ signals are required at the mixer's LO input. This IQ signal is generated by using branch line couplers that use the amplified 240 GHz signal from a separate PA chain to generate a 240 GHz differential IQ signal at the input of the mixer. While this is a straightforward approach, it may introduce non-ideal operation outside of its center frequency due to phase and amplitude imbalance, which results in a reduced conversion gain, which was measured to be -16 dB near the center frequency. However, since the sensor has a relative tuning range of around 10 %, these errors are small enough across the used frequency range. For more detail on the circuit architecture, see [11].

III. SYSTEM INTEGRATION

This section discusses the developed front-end PCB and the integration of the MMIC onto the PCB. Since most of the high-frequency components are integrated into the MMIC, only divider signals with frequencies of up to 8 GHz are present on the PCB. Therefore, we opted for a fast and cost-efficient solution, deciding to take an FR4 substrate. This section will introduce the components on the front-end, which are the frequency synthesizer with the loop filter, the IF-amplifier, and the dielectric lens. A photograph of the system is shown in Fig. 3, and the front-end PCB is detailed in Fig. 4 additionally.

In order to generate the frequency ramps needed for FMCW operation, the on-chip VCO needs to be stabilized and swept. To achieve this, a phased-locked-loop (PLL) is utilized by implementing the commercially available frequency synthesizer ADF4159 from Analog Devices. This PLL chip features components like the phase-frequency-detector (PFD), a charge pump, a programmable frequency divider with an optional

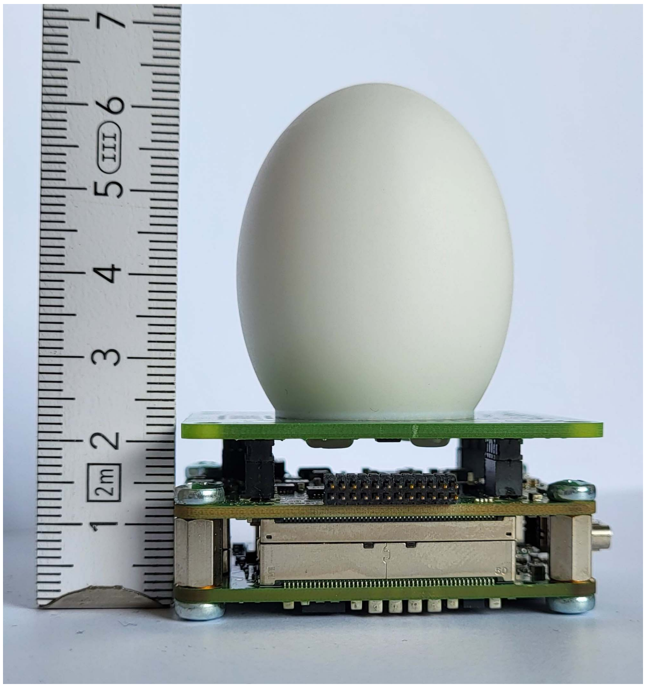

FIGURE 3. Photograph of the developed and fabricated THz FMCW sensor based on FR4 PCBs. The MMIC is hidden below the PTFE lens, which is also used as a cover for the bond wires. The total size of the sensor is $49 \times 43 \times 64$ mm without housing.

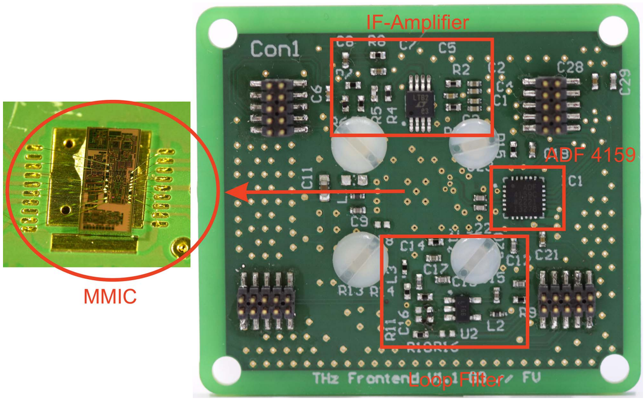

FIGURE 4. Photograph of the front-end PCB with marked IF-amplifier, ADF 4159 PLL chip, the loop filter, and the MMIC on the backside. The lens is mounted onto the PCB with nylon screws.

Delta-Sigma modulator, and the corresponding control and I/O capabilities. There is an on-chip divide-by-16 prescaler, so the input frequencies of the PLL chip are around 7.5 GHz, which the ADF4159 can easily handle. The reference signal, generated by a temperature-stabilized quartz crystal oscillator, is set to 100 MHz, featuring a very low phase noise of $-175\,\frac{\text{dBc}}{\text{Hz}}$ at 1 MHz offset frequency. The ADF4159 is designed to work with a wide range of VCOs, so the loop filter needs to be placed externally on the PCB. Multiple loop filter topologies can be chosen in such a system, including both active and passive filters. Since the charge pump can only

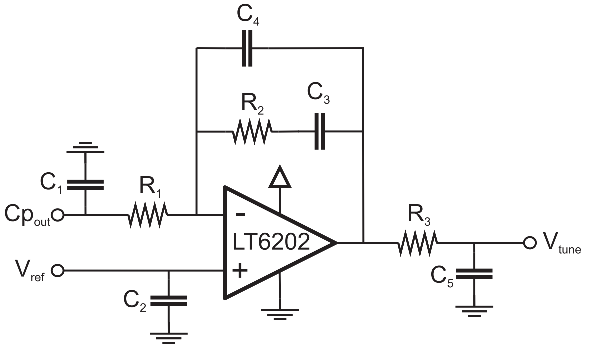

FIGURE 5. Active loop filter topology, featuring four poles for 5th order filter. A low noise operational amplifier (Analog Devices LT6202) is used at a positiv supply voltage of 5 V in this design.

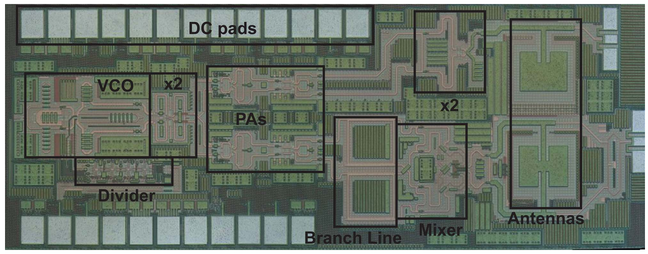

FIGURE 6. Picture of the fabricated MMIC in IHP's SG13G3Cu SiGe technology. The size of the MMIC is 2350 × 890 μm. The VCO-based signal generation is located on the left, while the patch antennas are located on the right side. The top and bottom sides are used for bondwire connections to the PCB for the dc signals as well as the divider output and the IF signal output.

support tuning voltages according to its supply range, which is 3.3 V, an active topology is needed for tuning voltages of up to 5 V. Further analysis led to the topology in Fig. 5 to be chosen in this sensor, featuring a total of 4 poles as a fifth-order active filter. The operational amplifier (OP) is a very low noise, rail-to-rail LT6202 from Analog Devices, operated from GND to 5 V.

The filter was designed with the program ADIsimPLL from Analog Devices, where the tuning and noise characteristics of VCO used on the MMIC was implemented. While the stability of the loop is given for a phase margin of more than 0° above the point of unity gain, typically a value above 30° is desirable to avoid stability problems due to e.g. component variation [20]. In this design, a margin of 49.5° is chosen to spare some margin along a loop bandwidth of 600 kHz. Incorporating all of the noise contributions from the VCO, the external crystal clock oscillator (XCO), as well as the PFD and loop filter, a total PLL noise of −75 dBcHz is simulated at 1 MHz offset frequency.

After the implementation of the PLL on the front-end, the software is configured. For generation of the FMCW ramp, a delta-sigma modulator is operated with frequency-hops of 250 kHz and a ramp duration of 4.8 ms, enabling fast repetition rate measurements in FMCW operation.

Directly integrated on the front-end, close to the MMIC, a first IF-amplifier is positioned. This amplifier is chosen to be an LT6203 low-noise OP-AMP with a fixed gain operating fully differential. The IF signal is then transferred onto the back-end PCB for signal processing. Mounted directly on the PCB, a dielectric lens is used to transmit and receive the THz signal. This lens is made out of PTFE and has an elliptical shape with a straight flange at the bottom for mounting. Simulations have been carried out using CST microwave studio. The simulations show a directivity of 39 dBi at the center frequency of 480 GHz. For more detailed information, cf. [11]. The front-end PCB features four 1.24 mm pin headers for the transfer of needed supply voltages and control signals to the back-end to ensure a compact overall design, durability, and flexibility.

This radar sensor aims to be highly integrated but also modular. A dedicated PCB was designed to manage these functions and meet the requirements for multiple supply voltages for the MMIC, PLL chip, loop filter, and IF amplifier, as well as the necessary control signals for the PLL. Several low-dropout regulators (LDOs) are implemented to generate the required voltages with low voltage ripple and are programmable by a simple resistor. An ADC is chosen to be directly integrated onto the PCB as well, featuring 18-bit with 2 Msps, ensuring a precise quantization of the received IF signal. An additional commercial board with a Zynq SoC provides process control, data acquisition, and signal processing. The sensor is powered via a single USB-C connection and can be operated while connected to a host computer or in stand-alone mode for embedded scenarios.

IV. MEASUREMENT RESULTS

In this section, measurement results using an on-wafer setup, as well as free-space setup results, are presented and discussed. For on-wafer measurements, frequency information was gathered with a Keysight UXA signal analyzer with the corresponding VDI spectrum analyzer extender (SAX), while power was measured using an Erickson PM5B power meter together with WR2.2 waveguide (WG) ground-signal-ground (GSG) probes. Since the back-end of the system is still under final verification IF signals during FMCW measurements were captured utilizing a Keysight Infinium oscilloscope with differential, high-Z input, and a 12-bit ADC. A picture of the manufactured MMIC is given in Fig. 6. The total size of the MMIC is 2350 × 890 μm^2, while the total dc-power consumption is 279 mA @ 3.3 V (921 mW) including the on-chip divide-by-16 prescaler.

A. MMIC RESULTS

First, the MMIC itself is measured with probes on an on-wafer probe station. Therefore, a dc probe is used to supply the MMIC with a voltage of 3.3 V as well as the tuning voltage for the VCO. The first result presented is the tuning curve at the RF output of the MMIC, shown in Fig. 7. The tuning range of the MMIC is from 451.2 GHz to 503.16 GHz, resulting

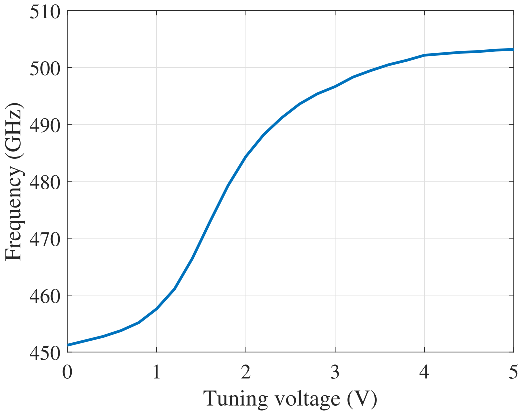

FIGURE 7. Tuning curve of the transmitter path. The VCO is tunable from 0 to 5 V and features a tuning range of 13 GHz, which is then multiplied in frequency to 52 GHz.

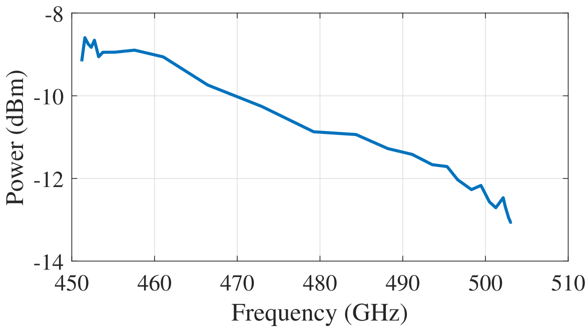

FIGURE 8. Output power of the transmitter, measured on-chip with pads and corrected for the losses of the probe, the waveguide taper and flange at the power meter (PM5B) as well as the on-chip pads.

in a relative tuning range of 10.9 % at a center frequency of 477 GHz. While this relative tuning range is moderate due to the used MOS capacitors in the VCO, the absolute tuning range is still around 52 GHz, ensuring precise target separation in the THz band.

The result presented below is the measured output power at the additional characterization pads added into the Tx path. These pads can be disconnected from the Tx path using a laser, removing the additional capacitance of the output pads, that create a plate capacitor between the probing area and the ground plane beneath, at the last frequency doubler's output. Fig. 8 displays the result, which is corrected for the loss of the used waveguide probe, a WG taper, and flange, as well as the losses of the used pad. The losses of the probe and the WG taper and flange were obtained from manufacturer datasheets, while the losses of the pads were estimated with 3D-EM simulations. As an example, for 480 GHz, the losses of the probe are 3.9 dB; for the WG taper and flange, it is 0.6 dB. The pads had a loss of 4.4 dB in the simulation at 480 GHz.

The measured power ranges from -9 dBm at the lower frequency corner to -13 dBm at just above 500 GHz. The

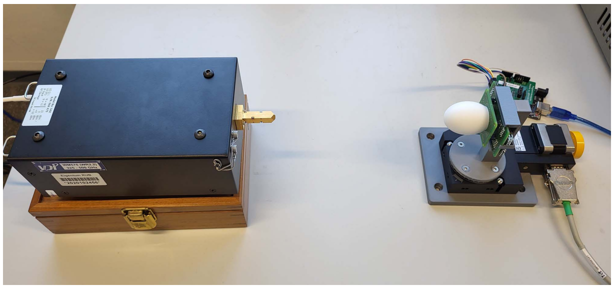

FIGURE 9. Picture of the measurement setup for both the EIRP as well as the transmission radiation pattern. The sensor is placed on a PI rotation stage and pointed at the VDI spectrum analyzer extender with its waveguide antenna. Absorber material is removed and objects are placed closer together for better visibility.

drop towards the higher frequencies is most likely due to the decreasing distance to the technologies' $f_{\max}$, as well as the extremely high influence of parasitic elements at this frequency, acting like a low-pass filter. Nevertheless, the power is relatively high for a SiGe-technology in this frequency range, without techniques like power combining, improving further compared to [11] and other already published work, where powers of -14 dBm to -10 dBm are reported [21] in this frequency range.

B. EIRP MEASUREMENT

Many THz applications suffer from a low dynamic range, which limits the sensor's maximum detection range. To determine the radiated output power, including the lens-based antenna, we measured the EIRP using a free-space setup. A Keysight UXA signal analyzer is equipped with a signal analyzer extension (SAX) module for the WR 2.2 waveguide band. The SAX is connected to a 26 dBi horn antenna from VDI. The measurement setup is depicted in Fig. 9. The first choice for power measurements is typically to use a power meter to ensure accurate results. In this given scenario, the expected received power at the horn antenna is quite low due to the free space loss of around 78 dB. This makes the reading from the PM5B very unstable below 1 μw. Therefore, the setup with the spectrum analyzer is chosen since it offers a much higher dynamic range for this power region. To ensure accurate results, the measured power on the UXA was checked through the use of a VDI WR2.1 VNA extension module (VNA-X) connected through a waveguide attenuator. The readings were then corrected with the manufacturer's datasheet values. The results were within the expected accuracy region for this frequency range and in consideration of the waveguide transitions between all components.

The radar sensor is placed 40 cm apart from the horn antenna, and several CW frequencies were used consecutively. For PLL stability reasons, the upper end of the ramp was set to 495 GHz since the output of the loop filter did not fully reach the upper supply rail.

The signal analyzer's 'max hold' detector was then used on the signal analyzer to capture the transmitted power during measurement. Afterward, the measured power data is

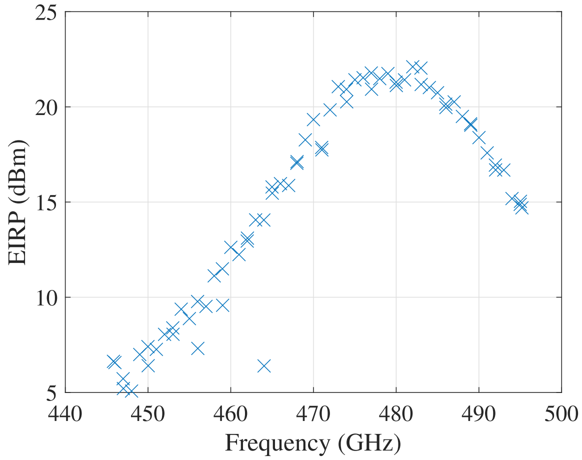

FIGURE 10. EIRP of the MMIC in stepped CW operation, captured with a spectrum analyzer extender at 40 cm distance using the "max hold" detector.

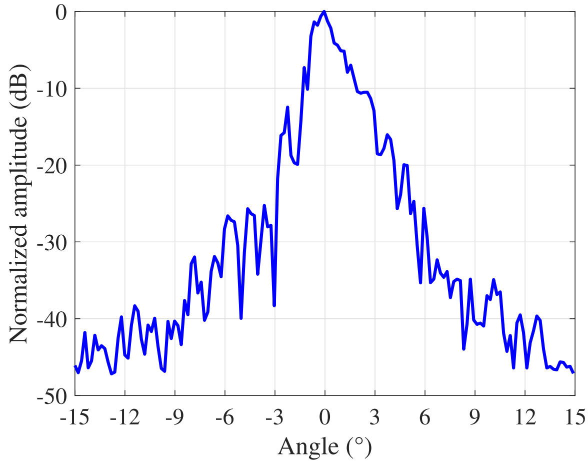

FIGURE 11. Transmission radiation pattern of the sensor in CW mode at 480 GHz as example, captured with a spectrum analyzer at a distance of 40 cm.

corrected with the free-space path loss and the gain of the horn antenna from VDI, according to the Friis transmission equation [22], resulting in the EIRP of the radar sensor. Based on [22], the far-field distance of an antenna with a diameter of 34 mm begins at a distance of 3.7 m. In the far-field calculation of a two-antenna setup, the larger lens-based antenna had to be used, not the horn antenna. This means that the EIRP measurement was performed in the near field rather than in the far field. The result is shown in Fig. 10 and shows EIRP values of 5 to 22 dBm of power over a frequency range of 49 GHz. The highest peak power is located at 479 GHz, while the power decreases towards the lower edge of the frequency range.

Based on a simulated lens antenna gain of around 38 dBi and the power result presented in Fig. 8, one would expect an EIRP of up to 27 dBm at the center frequency, opposing to the measured 22 dBm. There are several possible reasons for this deviation. First of all, there is a possible degradation of the patch antenna's efficiency η due to intense metal filling beneath and around the patch, needed by the Cu BEOL. At the edges of the patch, there is a trench down to the lowest metal. In this area, no metal filling is placed to avoid influencing the field between the signal layer edges and the reference ground plane. Aside from this trench, metal filling had to be included to fulfill design rule check (DRC) requirements, even in metal layers high in the stack and close to the signal layer of the patch antenna. This most likely lowers η to a certain extent. Simulations comparing the patch antenna with and without the metal filling indicate a difference of 1.8 dB in the radiation efficiency at center frequency and even 4.4 dB in the total efficiency.

Moreover, as already calculated, the measurement was performed within the near-field of the antenna since alignment at distances above 3.7 m is even more difficult. This may introduce near-field reflections and effects that have an uncertain influence on the measurement result. Finally, the simulations performed in [11] might not be 100 % accurate since the loss of material in CST is not fully accurate, leading to a possible overestimation of the simulated antenna gain. Together, these factors could explain the lower-than-expected EIRP, although this does not preclude FMCW operation as it only affects the sensor's SNR and maximum range.

C. TRANSMISSION RADIATION PATTERN

The transmission radiation pattern was measured with a simple setup using one rotating axis as a measurement for the radiation of the radar system. For this purpose, the radar was mounted onto a PI DT-80 rotation stage, which enables rotation with a resolution down to 0.2°. The radiated power is then again measured with a VDI SAX and a Keysight UXA, like for the EIRP. The plot, given in Fig. 11, displays the measured pattern with normalized amplitude. The E-field of the waveguide is parallel to the E-field on the patch antenna in this scenario, while the distance between both is 40 cm. The measurement shows a strong peak in the range of $-2°$ to $2°$. Outside of this range, a drop down to the noise floor of the measurement equipment is reached. The beam is very narrow aside from the peak; some fluctuating peaks are present between 20 and 40 dB below the main peak power, which are to be expected from the simulations in [11]. Additional influences are potential standing waves in the measurement setup since the distance from the sensor to the horn antenna was 40 cm only.

D. FMCW EXAMPLE SCENARIO

Several target scenarios have been evaluated to verify the radar sensor in FMCW operation. The simplest scenario is using a single corner reflector as a target at a predefined distance. Therefore, the measurement was performed with this target at 1.2 m. The setup of the FMCW measurement is demonstrated in Fig. 12. For the FMCW measurements, a swept TR of

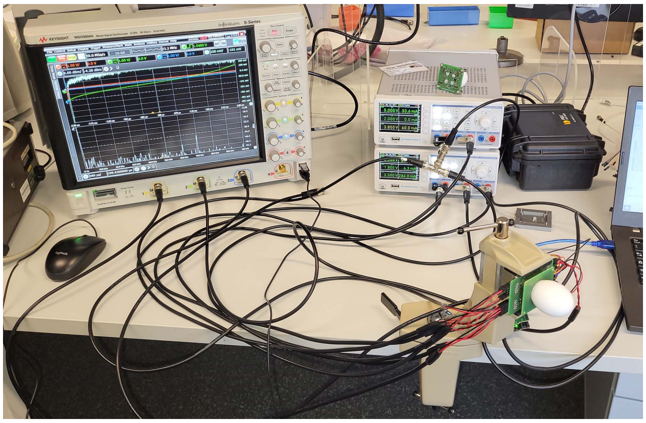

FIGURE 12. Picture of the setup for FMCW test measurements. The target is a corner reflector mounted on a stator, placed at a given distance.

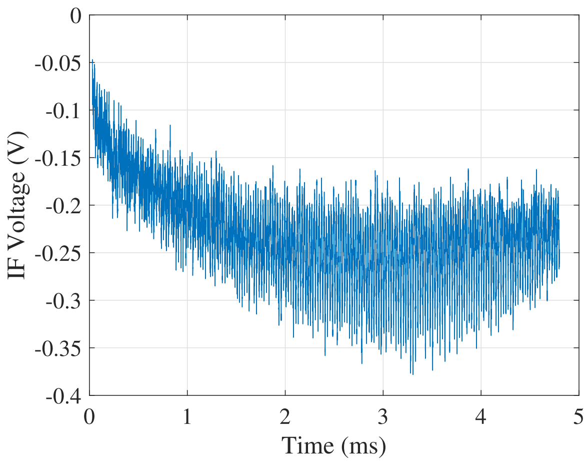

FIGURE 13. Captured differential IF signal within a FMCW ramp sweep of 4.8 ms. A small variation of approx. 180 mV is visible that is caused by the variation of the output power of the MMIC.

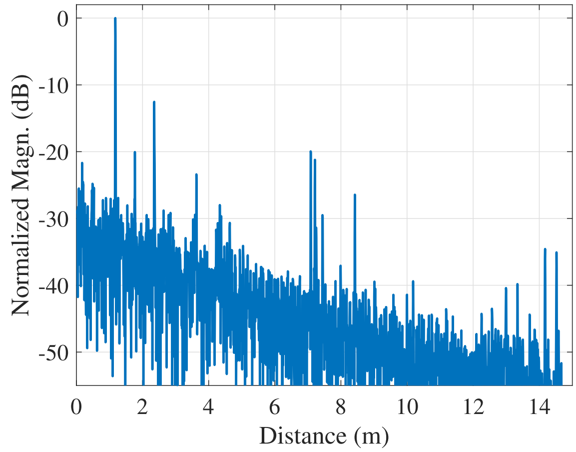

FIGURE 14. FMCW distance plot for a target at 1.2 m with removed dc and a hamming window applied. A strong peak is visible at the according distance, while also the multiple of it are visible. At a distance of around 7 m there are reflections of the room's wall and multipath reflections.

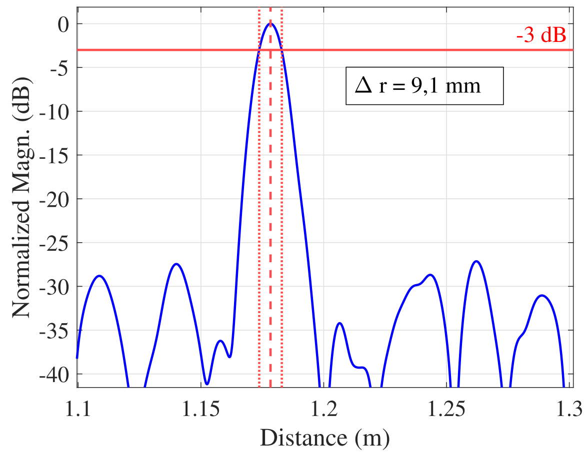

FIGURE 15. FMCW distance zoomed in on peak for determination of the 3-dB peak width. The measured width is 9.1 mm with a hamming window used.

49 GHz was used since there were some PLL-related stability problems at the upper end of the VCOs tuning range.

The PLL was controlled with an Arduino Uno microcontroller with the help of an adapter PCB with an oven-controlled crystal oscillator (OCXO) mounted on it. The differential IF signal was captured with a Keysight DSOS804 A oscilloscope, featuring a 16-bit resolution and 1 MΩ inputs. Fig. 13 displays the captured IF signal for a distance of 1.2 m. The amplitude of the signal is around 75 mV, showing a small envelope gradient across the frequency ramp time of 4.8 ms, while the frequency range of the sample is shifted down a bit compared to the VCO breakout measurements.

A Fast-Fourier Transformation (FFT) is utilized to calculate the distance within the spectrum of the IF signal, while the dc part is removed and a hamming window is applied. The x-axis is then rescaled to represent the distance to the mixer on the MMIC. The resulting distance plot is depicted in Fig. 14. The first and strongest peak is at a distance of 1.2 m, representing the corner reflector with 15 cm long edges. Following the first peak, there are multiple reflections visible, while two times the distance (2.4 m) is the second largest peak in this measurement.

Fig. 15 details the peak in the range spectrum. In this plot, the 3 dB peakwidth can be acquired, and thus, an estimation for the radar's target separation capabilities can be derived. The 3 dB width is 9.1 mm for this scenario with a hamming window applied. The hamming window itself decreases the side lobe levels at the cost of a broader peak. The factor for the hamming window is 1.3, which yields a theoretical minimum resolution of 3.98 mm for 49 GHz of TR. The resoluction is further influenced by the systems amplitude variation over the frequency as can be seen in Figs. 10 and 13 acting as an additional window function. The difference between the measured 9.1 mm resolution and the theoretical minimum is 5.1 mm, due to the above-mentioned reason as well as the

TABLE 1. **State-of-the-Art Wideband Transceivers Above 0.3 THz Tested in Free Space or FMCW Operation**

Ref.	Tech.	Type	f_c (GHz)	Tuning Range (GHz)	P_{dc} (mW)	P_{out} (dBm)	Size (mm^2)
[25]	130 nm SiGe	Ext. LO with multiplier chain	320	43	2944	−5	1.98
[26]	130 nm SiGe	Integrated VCO at 160 GHz	321	38.43	722	3	5.14
[27]	130 nm SiGe	Integrated VCO at 85 GHz	340	52	640	−6.8	1.2
[28]	130 nm SiGe	Integrated VCO at 170 GHz	340	70	1700	0.1	2.85
[29]	130 nm SiGe	Integrated VCO at 93 GHz	380	14.6	380	−11♣	4.18
[30]	35 + 50 nm InAlAs/InGaAs	Ext. LO with multiplier chain	383	80	1100	9	9
[31]	40 nm CMOS	Ext. LO with multiplier chain	420	0	905	−9	4.88
[21]	90 nm SiGe	Ext. LO with multiplier chain	470	55	280	−10	1.42
This	130 nm SiGe	Integrated VCO at 120 GHz	480	49	921	−9	2.1

Note: ♣ : EIRP

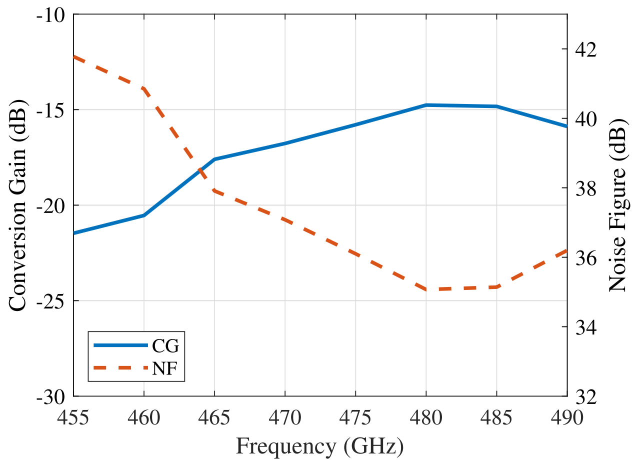

FIGURE 16. **Calculated conversion gain of the Rx mixer only and noise figure of receiver with the mixer and IF-amplifier. Measurement data were taken from the spectrum analyzer noise floor and FMCW measurements.**

influence of signal dispersion at this high frequency. It is possible to perform a calibration by weighting certain frequencies to enhance the resolution to its theoretical minimum at the cost of dynamic range [23]. Further measurements were carried out up to a distance of 5 m in the laboratory but are not shown to avoid redundancy.

E. RECEIVER CHARACTERIZATION

For FMCW measurements, the receiver noise and the conversion gain are also relevant. There are several possible ways to determine the receiver's noise figure (NF). In this work, the gain method is used [24]. For this method, the thermal noise is compared with the added noise measured at the noise floor with a spectrum analyzer. For room temperature, the NF can be calculated using:

$$NF = F_{\text{floor,out}} - \left(-174\frac{\text{dBm}}{\text{Hz}} + 10 \cdot \log(B_{\text{res}}) + G_{\text{IF}}\right)$$

where B_{res} is the resolution bandwidth of the spectrum analyzer, and G_{IF} the IF gain of the receiver path, including the Rx mixer on the MMIC and the IF amplifier on the front-end. The gain of the IF amplifier was simulated with LTspice from Analog Devices, while the conversion gain of the mixer was calculated from the FMCW measurement presented above. The results are presented in Fig. 16. For the frequency of 480 GHz, the gain of the mixer is $CG_{\text{mixer}} = -14.8$ dB. Together with the measured noise floor, the total noise figure of the receiver with mixer and amplifier is approx. 35.2 dB at 480 GHz.

V. COMPARISON

In recent years, transceivers for THz frequencies have become more and more relevant because of their possible bandwidths and application scenarios. Table 1 gives an overview of already published THz transceivers compared to this presented transceiver. There are several transceivers operating above 300 GHz, even reaching output powers as high as 3 dBm. Above 0.4 THz, there are only a few published transceivers, having in common the fact that they rely on an external signal source since they act as a multiplier chain. Nevertheless, they reach powers up to -10 dBm at 0.47 THz with a tuning range of 55 GHz. This work takes the center frequency to 0.48 THz, while reaching 49 GHz of tuning range in FMCW operation with an on-chip VCO, making it, to the author's best knowledge, the only fully integrated FMCW radar sensor operating at nearly 0.5 THz without external signal source. The output power is competitive to other work with up to -9 dBm, while the dc power consumption is a fair bit higher. One of the reasons for this is that this work is a fully integrated sensor without any need for stabilized RF signals being fed in from external sources. This means more power consumption in the VCO and divider circuits, but the benefits of this fully integrated solution in terms of mobility, compactness, and simplicity for various applications predominate.

VI. CONCLUSION

This article presented a fully integrated SiGe-based THz FMCW radar sensor. The sensor reaches a center frequency of 0.48 THz with a tuning range of 49 GHz (10% rel.) in FMCW operation. The introduced MMIC contains all RF components of the radar sensor, including a VCO and transmitter as well as receiver paths with on-chip patch antennas. The MMIC is integrated onto a cost-efficient FR4 PCB for easy production. A PTFE lens is used to collimate the radiated beam and acts as a mechanical cover for the bond wires of the MMIC. A back-end PCB featuring multiple LDOs has been developed to enable control and power supply with a commercial Zynq SoC board. Still, not all features of the software have been implemented yet. Nevertheless, FMCW operation was performed and demonstrated on an external oscilloscope, confirming operation at least up to 5 m in lab conditions, still exhibiting a sufficient dynamic range. The measured EIRP reaches up to 22 dBm at 479 GHz while the beam of the radar is narrow, enhancing angular resolution. These successful measurements validate that the chosen system concept and architecture are suitable for the Terahertz frequency range despite the challenges in the MMIC design and system integration. In summary, this work shows that with the development of new technologies in SiGe, electronics can tackle the THz gap from the mm-wave regime, already demonstrating a fully integrated and compact FMCW sensor at 0.48 THz. This work can be a base for THz communication, SAR-based imaging and material characterization, all in cost-efficient SiGe MMICs.

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